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CoreReset_PF v2.2 Release Notes

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 3.0

Updated for CoreReset_PF v2.2. Refer Table 1.

1.2 Revision 2.0

Updated for CoreReset_PF v2.1. Included core in Peripheral section in Libero.

1.3 Revision 1.0

Revision 1.0 was the first publication of this document. Created for CoreReset_PF v2.0.

Contents

2 CoreReset_PF v2.2 Release Notes

2.1 Overview

These release notes accompany the production release of CoreReset_PF v2.2. This document provides details about the features, enhancements, system requirements, supported families, implementations, and known issues and workarounds.

2.2 Features

- Synchronous negation of resets to ensure recovery time of downstream flip flops is met.

2.3 Delivery Types

No License is required to use CoreReset_PF. Complete RTL source code is provided for the core.

2.4 Supported Families

- PolarFire®

2.5 Supported Tool Flows

Requires Libero® System-on-Chip (SoC) PolarFire software v12.0 or later.

2.6 Installation Instructions

The CoreReset_PF CPZ file must be installed into Libero software. This is done automatically through the Catalog update function in Libero, or the CPZ file can be manually added using the **Add Core** catalog feature. Once the CPZ file is installed in Libero, the core can be configured, generated, and instantiated within SmartDesign for inclusion in the Libero project.

Refer to the *Libero SoC Online Help* for further instructions on core installation, licensing, and general use.

2.7 Documentation

This release contains a copy of the *CoreReset_PF Handbook*. The handbook, describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and also implementation suggestions. Refer to the *Libero SoC Online Help* for instructions on obtaining IP documentation.

For updates and additional information about the software, devices, and hardware, visit the Intellectual Property pages on the Microsemi SoC Products Group website: visit:

http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores.

2.8 Known Limitations and Workarounds

There are no known limitations and workarounds for CoreReset_PF.

2.9 Resolved Issues

The following table lists the resolved issues in v2.2 Release.

Table 1 • **Resolved SARs in CoreReset_PF v2.2 Release**

SAR	Description
105208	Included gating of signals coming from input buffers and pipeline stage of 16 registers for synchronous reset.
106735	Removed support for IGLOO2 Family.
97049	Updated Handbook for v2.2.