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CoreBootStrap v3.0 Release Notes

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 2.0

Updated for CoreBOOTSRAP v3.0. PolarFire support added, Big Endian support removed, SPI source address, and AHB destination address split into upper and lower words to facilitate VHDL support.

1.2 Revision 1.0

Revision 1.0 was the first publication of this document. Created for CoreBOOTSTRAP v2.0.

Contents

2 CoreBootStrap v3.0 Release Notes

2.1 Overview

These release notes accompany the production release of CoreBootStrap v3.0. This document provides details about the features, enhancements, system requirements, supported families, implementations, and known issues and workarounds.

2.2 Features

Following are the key features of CoreBootStrap:

- Provides bootstrap capability to a processor sharing an AHB bus, whereby boot code is extracted from SPI and placed in AHB-based RAM for fast execution after exiting the reset state
- Supports all available SPI Flash chips, via “Motorola Mode 0” signaling, and parameterized software reset command sequences along with various timing parameters to handle differences between SPI chip manufacturers
- Resets extended to parameterized durations:
- Power-on reset length to overcome SPI Flash chips’ widely-varying specifications from power-up to device available, which can range from under 200µs to over 5ms
- Default reset duration parameterized separately to cover the other two reset sources
- Supports three reset sources:
  - Power-on reset
  - External reset
  - Processor reset
- Three and four byte addressing options parameterized to handle SPI flash chips of different sizes
- SPI Flash source and AHB RAM destination addresses are parameterized along with the 32-bit word count for the boot code copy operation
- AHB master-mode compatible, including handling AHB “response” in case of error conditions
- Posted-write protection via read-back of first location in AHB memory at end of copy
- Safe transfer of SPI bus to host after boot via Flash Slave-select (FLASH_SS) glitch avoidance
- Software debug support: bypassing of boot code copying and error signals provided
- SPI clock programmable as any even-number ratio of AHB clock to SPI clock, minimum ratio 4:1
- Support for VHDL and Verilog netlists

2.3 Interfaces

CoreBootStrap supports the following interfaces:

- AHB and AHB-Lite 32-bit Master interface
- SPI serial flash interfaces which handle “Motorola Mode 0” signaling (all available SPI Flash chips support this mode)
- SPI host interfaces, such as that of CoreSPI

2.4 Delivery Types

A License is not required for using CoreBootStrap v3.0. Complete Verilog unobfuscated source code is provided for the core and user test benches.

2.5 Supported Families

- RTG4™
- PolarFire®
- SmartFusion®2
- IGLOO®2

2.6 Supported Tool Flows

- Libero® System-on-Chip (SoC) software v11.7 or later.
- Supports Windows & Linux operating systems

2.7 Supported Test Enviroments

- Verilog user test bench

2.8 Installation Instructions

The CoreBootStrap CPZ must be installed into Libero software. This is done automatically through the Catalog update function in Libero, or the CPZ file can be manually added using the **Add Core** catalog feature. Once the CPZ file is installed in Libero, the core can be configured, generated, and instantiated within SmartDesign for inclusion in the Libero project.

Refer to the *Libero SoC Online Help* for further instructions on core installation, licensing, and general use.

2.9 Documentation

This release contains a copy of the *CoreBootStrap Handbook*. The handbook, describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and also implementation suggestions. Refer to the *Libero SoC Online Help* for instructions on obtaining IP documentation.

For updates and additional information about the software, devices, and hardware, visit the Intellectual Property pages on the Microsemi SoC Products Group website: visit:

http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores.

2.10 Known Limitations and Workarounds

- AHB bus sizes other than 32 bits are not supported
- SPI flash and AHB RAM start addresses must start on 4-byte word boundaries
- Checksum, when supported, must be on a 4-byte word boundary
- Boot code must be a multiple of 4 bytes
- No support for big endian