CoreTimer v2.0 Release Notes

This document accompanies the production release for CoreTimer v2.0. It describes the features and enhancements. It also has information about system requirements, supported families, implementations, known issues and workarounds, and resolved issues from previous versions.

Features

CoreTimer is an APB slave module that provides access to an interrupt-generating, programmable decrementing counter.

Key Features

CoreTimer has the following features:

- Configurable 16-bit or 32-bit Timer
- APB slave interface for register access
- No additional clock required. Runs off the APB clock
- Prescaler provides clock division up to 1,024
- Continuous or one-shot operating modes
- Interrupt generation

Interfaces

CoreTimer supports the following interfaces:

- APB slave interface
- Interrupt request interface

Delivery Types

A License is not required for using CoreTimer v2.0. The complete hardware description language (HDL) source code is provided for the core and testbenches.

Supported Families

All Microsemi® devices and families are supported by CoreTimer v2.0.

Supported Tool Flows

Libero v9.1 or later software supports CoreTimer v2.0.

Note: CoreTimer is compatible with both Libero Integrated Design Environment (IDE) and Libero System on-Chip (SoC). Unless specified otherwise, this document uses the name Libero to identify both Libero IDE and Libero SoC.

Installation Instructions

The CoreTimer CPZ file must be installed in Libero. This is completed automatically through the Catalog update function in Libero, or the CPZ can be manually added using the **Add Core** catalog feature. Once installed in the Libero catalog, the core can be instantiated and configured.

Refer to the Using DirectCore in Libero IDE User Guide or Libero SoC online help for further instructions on core installation, licensing and general use.

Documentation

This release contains a copy of the *CoreTimer Handbook*, which describes the core functionality, step-by-step instructions on how to simulate, synthesize, place-and-route this core, and suggestions for implementation.

For more information about Intellectual Property, visit: http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores. For updates and additional information about software, FPGAs, and hardware, visit: www.microsemi.com.

Supported Test Environments

The following test environments are supported:

- VHDL user testbench
- Verilog user testbench

Known Issues and Workarounds

There are no known limitations or workarounds with the CoreTimer v2.0 release.

Release History

Table 1 provides the release history of CoreTimer.

Table 1 CoreTimer Release History

Version	Date	Changes
2.0	April 2015	Added support for RTG4 family devices.
1.0	January 2008	Initial release.

Resolved Issues in the v2.0 Release

Table 2 lists the Software Action Requests (SARs) that are resolved in the CoreTimer v2.0 release.

Table 2 Resolved Issues in the v2.0 Release

SAR	Description
63945	Added Support for RTG4 devices.

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