RN0050

CoreSPI v5.2 Release Notes

Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA
Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996
E-mail: sales.support@microsemi.com
www.microsemi.com

About Microsemi

Microsemi Corporation (Nasdaq: MSCC) offers a comprehensive portfolio of semiconductor and system solutions for aerospace & defense, communications, data center and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; enterprise storage and communication solutions, security technologies and scalable anti-tamper products; Ethernet solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, Calif., and has approximately 4,800 employees globally. Learn more at www.microsemi.com.

51300050-6/4.18

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 6.0

Updated changes related to CoreSPI v5.2.

1.2 Revision 5.0

Updated changes related to CoreSPI v5.1.

1.3 Revision 4.0

Updated changes related to CoreSPI v5.0.

1.4 Revision 3.0

Updated changes related to CoreSPI v4.2.

1.5 Revision 2.0

Updated changes related to CoreSPI v3.0.

1.6 Revision 1.0

Revision 1.0 was the first publication of this document. Created for CoreSPI v2.0.

Contents

2 CoreSPI v5.2 Release Notes

2.1 Overview

These release notes accompany the production release of CoreSPI v5.2. This document provides details about the features, enhancements, system requirements, supported families, implementations, and known issues and workarounds.

2.2 Features

- SPI clock rate configurable:
  - From PCLK/512 to PCLK/2 in steps of 2
  - Maximum data rate of PCLK/2 in Master mode and PCLK/8 in Slave mode.
- SPI protocol configurable
  - Master and slave operation
  - Supports up to eight slaves
  - Motorola SPI support
  - TI SPI support
  - NSC SPI support
  - Slave select behavior configurable during Idle cycles
  - Supports broadcast operation
  - Configurable frame size (4 to 32 bits)
- FIFO
  - Width set to frame size for optimal core size
  - Depth configurable through parameter
- Interrupt generation
  - Receive and transmit data interrupts
  - FIFO overflow and under run
  - Command transmitted interrupt
- APB3 compliant

2.3 Supported Interfaces

CoreSPI supports the following interfaces:

- Advanced peripheral bus (APB) slave interface
- Interrupt request interface
- Serial (SPI) Interface

2.4 Delivery Types

CoreSPI is not license locked. Complete HDL source code is provided for the core and testbench.

2.5 Supported Families

CoreSPI v5.2 is a generic core and supports all the device families.

2.6 Supported Tool Flows

Libero® software v9.1 or later supports CoreSPI v5.2.

Note: CoreSPI is compatible with Libero Integrated Design Environment (IDE), Libero System-on-Chip (SoC), and Libero System-on-Chip (SoC) PolarFire. Unless specified otherwise, this document uses the name, Libero to identify Libero IDE, Libero SoC, and Libero SoC PolarFire.

2.7 Installation Instructions

The CoreSPI CPZ must be installed into Libero software. This is done automatically through the Catalog update function in Libero, or the CPZ file can be manually added using the **Add Core** catalog feature. Once the CPZ file is installed in Libero, the core can be configured, generated, and instantiated within SmartDesign for inclusion in the Libero project.

Refer to the *Libero SoC Online Help* for further instructions on core installation, licensing, and general use.

2.8 Documentation

This release contains a copy of the *CoreSPI Handbook*. The handbook, describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and also implementation suggestions. Refer to the *Libero SoC Online Help* for instructions on obtaining IP documentation.

For updates and additional information about the software, devices, and hardware, visit the Intellectual Property pages on the Microsemi SoC Products Group website: visit:

http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores.

2.9 Supported Test Environments

The following test environments are supported:

- VHDL user testbench
- Verilog user testbench

2.10 Release History

Table 1 lists the release history for CoreSPI.

Table 1 • **Release History**

Version	Date	Changes
5.2	April 2018	Fixed SAR as listed in Table 2
5.1	November 2016	Fixed SAR as listed in Table 3
5.0	December 2014	• Added support for RTG4 family devices. • Updated configurator GUI • Modified configuration parameters. • RXAVAIL interrupt bit renamed to DATA_RX • Modified user testbench to highlight the operation of the TX_DONE and DATA_RX interrupt sources.
4.2	December 2013	• Added support for TI and NSC modes. • Configurable frame size support included. • TX and RX FIFO's added. • Modified SPI related port names. • Modified operational parameters to be configurable at time of instantiation exclusively. • Support for SmartFusion2 and IGLOO2 families added. Modified Interrupt Status register to enhance management of core during slave mode
3.0	June 2007	APB Interface added and testbench support for ProASIC3 modified.
2.0	November 2006	Initial Release.

2.11 Resolved Issues in the v5.2 Release

Table 2 • **Resolved Issues in the v5.2 Release**

SAR Number	Changes
94059	Resolved an internal signal being detected as unidentified clock by synthesis tool.
94224	Added APB register CLK_DIV to dynamically update the clock division factor of the SPI generated clock (SPICLKO) in master mode.
94973	Repackaged CoreSPI as a generic core supporting all devices families.
92192	Updated utilization and performance table in CoreSPI Handbook for AX and RTAX-S families.

2.12 Resolved Issues in the v5.1 Release

Table 3 • **Resolved Issues in the v5.1 Release**

SAR Number	Changes
68916	Unable to instantiate CoreSPI version 5.0.100 in Libero v9.2 SP2.
66515	CoreSPI do not return default reset values for Configuration Registers.
84364	Added waveforms and details of custom transfer.
84520	NSC standard mode SPIOEN signal was asserted with one clock cycle. As a result, delay in multi frame transfers was observed.
84582	In VHDL mode, SPISS was toggled during transfer (that is, MOTOROLA master mode).

2.13 Resolved Issues in the v5.0 Release

Table 4 • **Resolved Issues in the v5.0 Release**

SAR Number	Changes
12697	Updated configurator GUI to make the configuration of CoreSPI more intuitive.
57406	Support added for RTG4 family devices.
62506	INTRAW Register - RXAVAIL bit: Bit renamed to reflect the exact operation of the bit (DATA_RX).

2.14 Resolved Issues in the v4.2 Release

No Software Action Requests (SARs) have been resolved in the v4.2 release of CoreSPI.

2.15 Resolved Issues in the v3.0 Release

Table 5 • **Resolved Issues in the v3.0 Release**

SAR Number	Changes
67221	An APB interface has been added and the SFR interface has been removed for use with CoreConsole in bus-centric design.
61318	CoreSPI was missing ProASIC3 libraries for the verification testbench (v2.1), but the testbench no longer requires family-specific libraries (v3.0).

2.16 Discontinued Features and Devices

CoreSPI v5.0 and later versions supports a new configuration GUI, which is intended to make the CoreSPI configuration more straightforward.

The following parameters are removed:

- CFG_SPO
- CFG_SPH
- CFG_SPS

Instead, the following parameters must be configured at the time of instantiation:

- CFG_MOT_MODE
- CFG_MOT_SSEL
- CFG_TI_NSC_CUSTOM
- CFG_TI_NSC_FRC
- CFG_TI_JMB_FRAMES
- CFG_NSC_OPERATION

RXAVAIL bit in the Raw Interrupt Status register and Interrupt Clear register has been renamed to DATA_RX.

2.17 New Features and Devices

The top-level configuration parameters used in CoreSPI v5.0 and later versions differ from the parameters used in earlier versions of the core (core v4.2 or lower versions). When updating a design using an earlier version of CoreSPI (core v4.2 or lower version) to use CoreSPI v5.0 and later version, you may need to adjust the parameter settings for the CoreSPI instance). Refer to **Parameter Migration Table** in the Design Migration section of the CoreSPI v5.0 and later version handbook which details the required parameter configuration to migrate from previous versions of the core.

The following features were added in version 5.0:

Updated configurator GUI:

- Supports Motorola mode selection
- Enhanced configuration of TI and NSC modes

Modified top-level configuration parameters

- FIFO_DEPTH parameter renamed to CFG_FIFO_DEPTH
- Parameters added:
  - CFG_MOT_MODE
  - CFG_MOT_SSEL
  - CFG_TI_NSC_CUSTOM
  - CFG_TI_NSC_FRC
  - CFG_TI_JMB_FRAMES
  - CFG_NSC_OPERATIONS
- Renamed RXAVAIL interrupt bit in the Raw Interrupt Status and Interrupt Clear registers to DATA_RX
- Updated user testbench to highlight the operation of the TX_DONE and DATA_RX interrupts
- Support for RTG4 family devices

The following features are added to this version:

- Added APB register CLK_DIV to dynamically update the clock division factor of the SPI generated clock (SPICLKO) in master mode.

2.18 Known Limitations and Workarounds

The user testbench in CoreSPI v5.0 and later versions release provides support for fixed parameter configuration only.