CoreTSE v3.2

CoreTSE User Guide

Introduction

The CoreTSE provides 10/100/1000 Mbps Ethernet Media Access Controller (MAC) with a Gigabit Media Independent Interface (G/MII) or Serial Gigabit Media Independent Interface (SGMII) Ten Bit Interface (TBI) to support 1000BASE-T and 1000BASE-X.

The CoreTSE has the following major interfaces:

- G/MII or SGMII TBI physical layer (PHY) interface connects to Ethernet PHY
- Management data input/output (MDIO) interface to communicate with the MDIO manageable device (MMD) in the PHY
- MAC data path interface
- Advanced peripheral bus (APB) - Target interface for MAC configuration registers and status counters access

A triple speed MAC core is responsible for the main functionalities of CoreTSE. They are:

Statistics gathering - Statistics information is gathered from the data transmitted and received over the Ethernet link.

Station address functions - Station address (SAL) feature provides address filtering capability.

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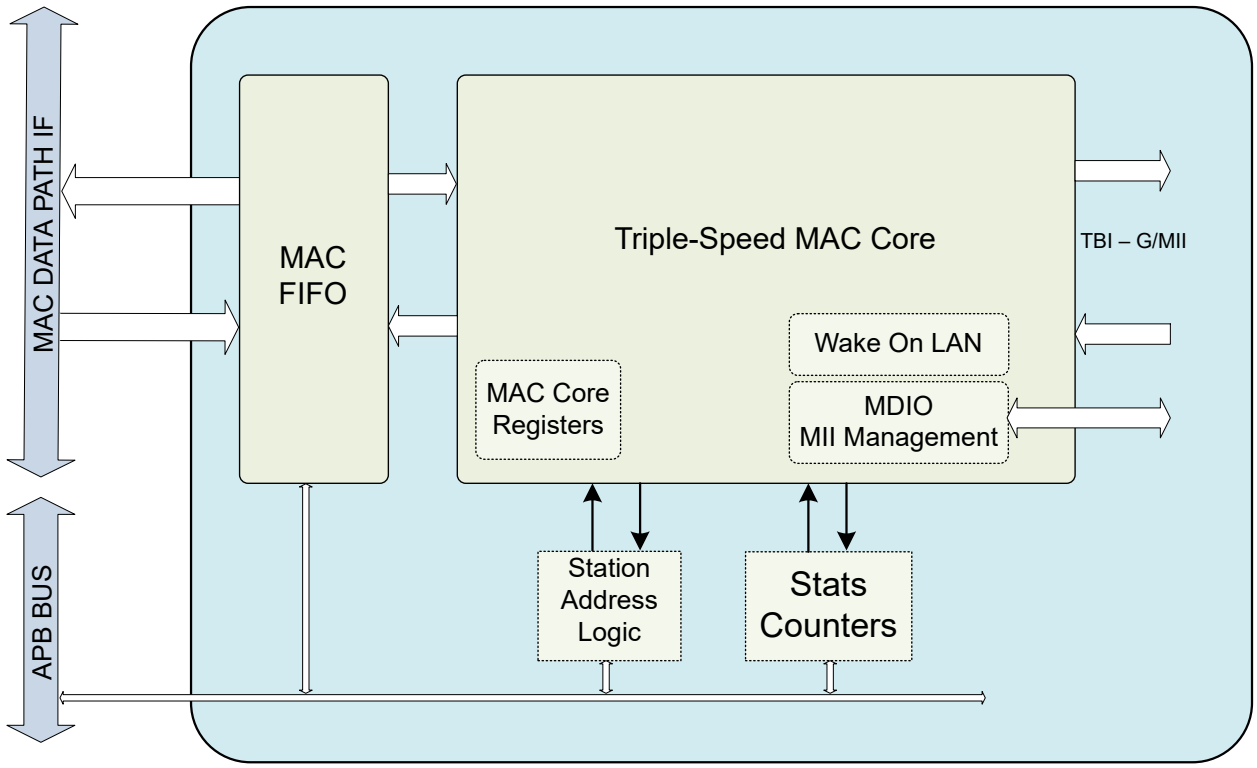
Figure 1. CoreTSE Block Diagram



Features

CoreTSE has the following features:

- 10/100/1000 Mbps Operation
- Full-duplex Support at 10/100/1000 Mbps
- Half-duplex Support at 10/100 Mbps
- Standard G/MII Interface
- MDIO Interface for PHY Register access
- SGMII Ten Bit Interface (TBI)
- Wake on LAN (WoL) with Magic Packet Detection
- Frame Statistics Counters
- Destination Address-Based Filtering

Core Version

This document applies to CoreTSE version 3.2.

Supported Families

- PolarFire® SoC
- PolarFire
- IGLOO®2
- RTG4™
- SmartFusion®2

Device Utilization and Performance

Device utilization and performance data is provided in Table 1 to Table 4 for the supported device families. The TXCLK, RXCLK, TBI_TX_CLK, and TBI_RX_CLK performance is above 125 MHz. The data in the following table is achieved using typical synthesis and layout settings. The data described in the table is only indicative. The overall device utilization and performance of the core is system dependent.

CoreTSE Device Utilization

The following table describes the CoreTSE device utilization applicable for these (G/MII, PACKET_SIZE = 256 Bytes, SAL-OFF, WoL-OFF, and STATS-OFF) parameters.

Table 1. CoreTSE Device Utilization

Family (Device)	Utilization				Performance (MHz)		
	Sequential (DFF)	Combinational (LUT)	Total	%	PCLK	MTXCLK	MRXCLK
SmartFusion2® (M2S050)	2347	3211	5558	9.87	190	220	197
IGLOO2® (M2GL050)	2347	3211	5558	9.87	190	220	197
RTG4® (RT4G150)	2323	3313	5635	3.71	156	186	152
PolarFire® (MPF300T)	2287	3143	5430	1.81	297	304	266
PolarFire SoC (MPFS250T)	2287	3143	5430	2.14	292	340	292

CoreTSE Device Utilization

The following table describes the CoreTSE device utilization applicable for these (G/MII, PACKET_SIZE = 32 KB, SAL-ON, WoL-ON, and STATS-ON) parameters.

Table 2. CoreTSE Device Utilization

Family (Device)	Utilization				Performance (MHz)		
	Sequential (DFF)	Combinational (LUT)	Total	%	PCLK	MTXCLK	MRXCLK
SmartFusion®2 (M2S050)	5564	8267	13831	24.55	140	186	124
IGLOO®2 (M2GL050)	5564	8267	13831	24.55	140	186	124
RTG4™ (RT4G150)	5579	8662	14241	9.38	115	146	91
PolarFire® (MPF300T)	5299	8568	13867	4.63	220	248	187
PolarFire SoC (MPFS250T)	5299	8568	13867	5.46	203	256	174

CoreTSE Device Utilization

The following table describes the CoreTSE device utilization applicable for these (TBI, PACKET_SIZE = 256 Bytes, SAL-OFF, WoL-OFF, and STATS-OFF) parameters.

Table 3. CoreTSE Device Utilization

Family (Device)	Utilization				Performance (MHz)		
	Sequential (DFF)	Combinational (LUT)	Total	%	PCLK	MTXCLK	MRXCLK
SmartFusion®2 (M2S050)	3408	5271	8679	15.40	177	221	184
IGLOO®2 (M2GL050)	3408	5271	8679	15.40	177	221	184
RTG4™ (RT4G150)	3374	5324	8698	5.73	162	163	154
PolarFire® (MPF300T)	3329	5113	8442	2.82	288	358	301
PolarFire SoC (MPFS250T)	3329	5113	8442	3.32	292	340	292

CoreTSE Device Utilization

The following table describes the CoreTSE device utilization applicable for these (TBI, PACKET_SIZE = 32 KB, SAL-ON, WoL-ON, and STATS-ON) parameters.

Table 4. CoreTSE Device Utilization

Family (Device)	Utilization				Performance (MHz)		
	Sequential (DFF)	Combinational (LUT)	Total	%	PCLK	MTXCLK	MRXCLK
SmartFusion®2 (M2S050)	6623	10206	16829	29.87	136	166	126
IGLOO®2 (M2GL050)	6623	10206	16829	29.87	136	166	126
RTG4™ (RT4G150)	6633	10718	17315	11.43	120	127	90
PolarFire® (MPF300T)	6341	10529	16870	5.63	207	290	191
PolarFire SoC (MPFS250T)	6341	10529	16870	6.64	203	256	174

Table of Contents

1. Functional Description

This section describes the functionality of the CoreTSE.

1.1 Triple Speed MAC

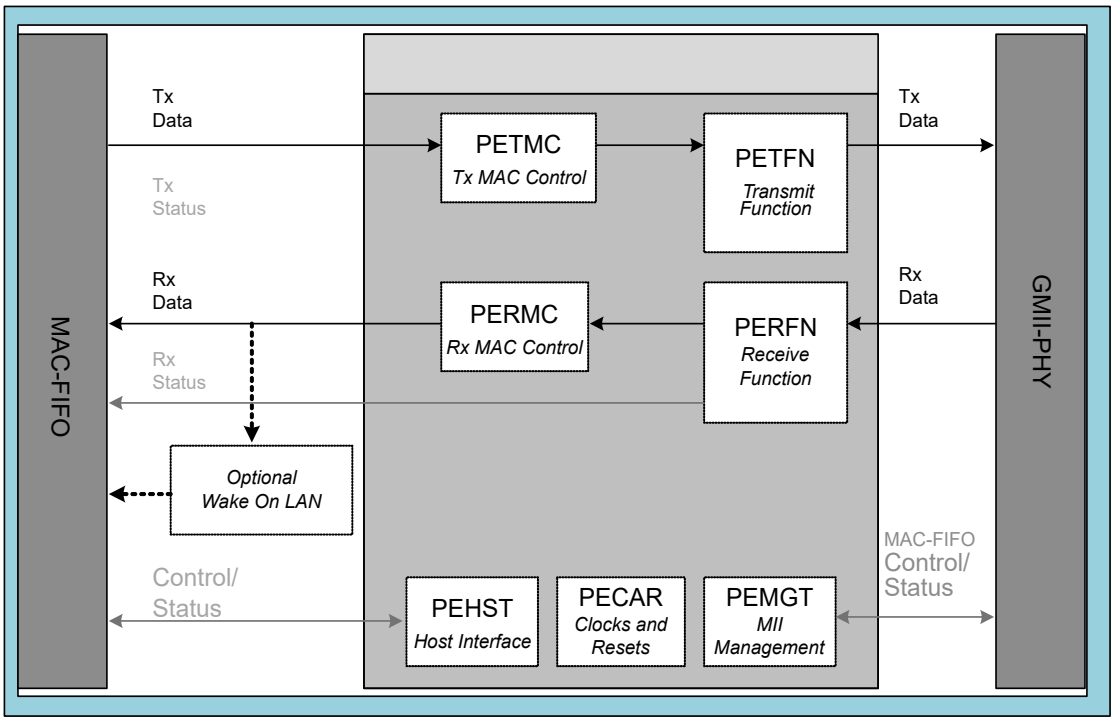
This core is a full-featured 10/100/1000 Mbps MAC with standard G/MII. The MAC has built in G/MII to TBI converter, which supports 1000 Mbps with TBI. The core is capable of full-duplex operation at 10, 100, or 1000 Mbps and of half duplex operation at 10 and 100 Mbps.

In half-duplex mode, the MAC adheres to the Carrier Sense Multiple Access/Collision Detect Access method as defined in IEEE 802.3 and its several supplements including IEEE 802.3u. In full-duplex mode, the MAC follows IEEE 802.3x, which ignores both carrier and collisions. Following each packet transmission or abortion, a transmit statistics vector is used for statistics collection.

The external PHY device presents packets to the MAC. The MAC scans the preamble searching for the start frame delimiter (SFD). When the SFD is found, the preamble and SFD are stripped and the frame is passed to the system. Following each frame reception, a Receive Statistics Vector is used for frame filtering and statistics collection.

CoreTSE supports PAUSE control frames. This core also includes optional support for Wake-on-LAN (WoL) module. The WoL module detects both IEEE 802.3-compliant unicast frames with a destination address that matches the station address and packets that use AMD's Magic Packet™ Detection technology. The detection functionality can be enabled or disabled.

Figure 1-1. Triple Speed MAC Functional Block Diagram



1.2 PAUSE Flow Control

MAC transmit logic (MACTL) provides native support for PAUSE flow control frames. PAUSE frames are control frames (frames with 0x8808 as the Ether Type) with a particular DA (01-80-c2-00-00-01) and the opcode 0x0001. The FIFO-logic automatically Request-to-Send a PAUSE frame by pulsing transmit-control-request (TCRQ) and provides the pause time value available on control-frame-register (CFPT [15:0]). Pause frame payload contains CFPT and CFEP (Control Frame extended parameter). Once a frame is received and detected as a control frame,

MAC checks for the DA and the Opcode fields. If the DA is either the reserved multicast address used by PAUSE (01-80-c2-00-00-01) or the station's unique address, and the Opcode is 0x0001, then the Control frame is considered to be a PAUSE Control frame.

When a PAUSE Control frame is received:

- The MAC receive logic (MACRL) module indicates the MACTL to pause the stream of data frames and allows control frames transmission to the link partner. When either a PAUSE frame with a zero-value pause time is received or the MACRL pause timer expires, MACTL is considered to be unpaused and normal data frames gets resumed.
- The pause time value is loaded into the PERMC pause timer. This pause timer is a 16-bit down counter that decrements every pause quanta (a speed-independent constant of 64 byte-times). Whenever the pause time counter is nonzero, the MAC is considered to be paused and no data frames are sent.

1.3 Jumbo Frame Support

The CoreTSE supports jumbo frames that exceed the 1500 byte maximum of the standard Ethernet frame. When using jumbo frames the amount of idles that are present in the systems reduced and therefore the frequency of clock compensation events are lower. When supporting jumbo frames the clocking tolerance between the transmit clock and the receive clock is required to be 0 ppm to account for the reduction in idles.

The Jumbo frame length transmitted/received by the CoreTSE is according to Maximum Frame Length (0x010) register configuration and supports up to 4000 bytes only.

1.4 Inter-Frame-Gap

MACRL provides the capability to filter frames that have less than a certain inter-frame-gap. The standard states that the inter-frame-gap should be 160 bit-times. This includes 96 bits of inter packet gap (IPG), 56 bits of preamble and 8 bits of start frame delimiter (SFD). To protect downstream logic from over-running, MACRL can be programmed with a minimum inter frame gap (IFG) parameter. The second of two back-to-back frames to violate the minimum IFG is dropped.

1.5 Address Detect

MACRL scans the frame and determine its address type. The 48-bit programmed station address is compared to each receive frame's DA. When they match, the unicast address detect (UCAD) is asserted. If the broadcast address is detected, MACRL asserts broadcast address detect (BCAD). If a multicast address is detected, the MAC asserts multicast address detect (MCAD).

1.6 Hash Table Support

MACRL supports hash table with up to 128 entries. Seven bits of the Cyclic Redundancy Check (CRC) of the DA are used as the Hash Value (HASHV [6:0]).

1.7 Length Checking and Maximum Length Enforcement

MACRL can optionally compare the length field with the actual length of the data field portion of the frame. This is enabled through the MAC Configuration #2 register. MACRL first determines if the length/type field is a valid length. If so, it is compared with the data field length and any mismatches are updated to the receive statistics.

MACRL can limit the length of receive frames passed to the system. The maximum length is programmed through the Maximum Frame Length register. Frames which exceed this maximum are truncated.

1.8 Internal Loopback at G/MII

Asserting the internal loopback enable bit in MAC Configuration #1 register, enables MAC transmit output's looped back to the MAC receive inputs at G/MII interface.

1.9 WoL

The MAC-WoL is based on AMD's Magic Packet Detection technology.

The first step of the detection procedure is to scan the first twelve bytes of the frame, which contain Destination and Station addresses. Magic Packet detection is only carried out when the incoming frame's destination address matches the MAC's station address, or if the frame's destination address is a multicast or broadcast address.

After the first twelve bytes of the frame have matched, core searches for the Magic Packet technology's defined preamble of six continuous aligned bytes with all bits asserted (0xFFh). Following a valid Magic Packet preamble, core immediately expects 16 back-to-back repetitions of the six-byte MAC station address. Failure to achieve this exact pattern by a single byte at any time during the frame resets the circuitry back to the preamble search state.

After successful recognition of the Magic Packet payload or a successful compare of the MAC's station address with the incoming frame's destination address, the Interface STATUS Register (bit field Wake on Lane Detected) is asserted and status bit can only be cleared through assertion of the Wake on Lane Detected Clear bit field of Interface Control register.

1.10 MDIO Management

Control and status is provided to and from the PHY through the two-wire MDIO management interface described in IEEE802.3u Clause22.

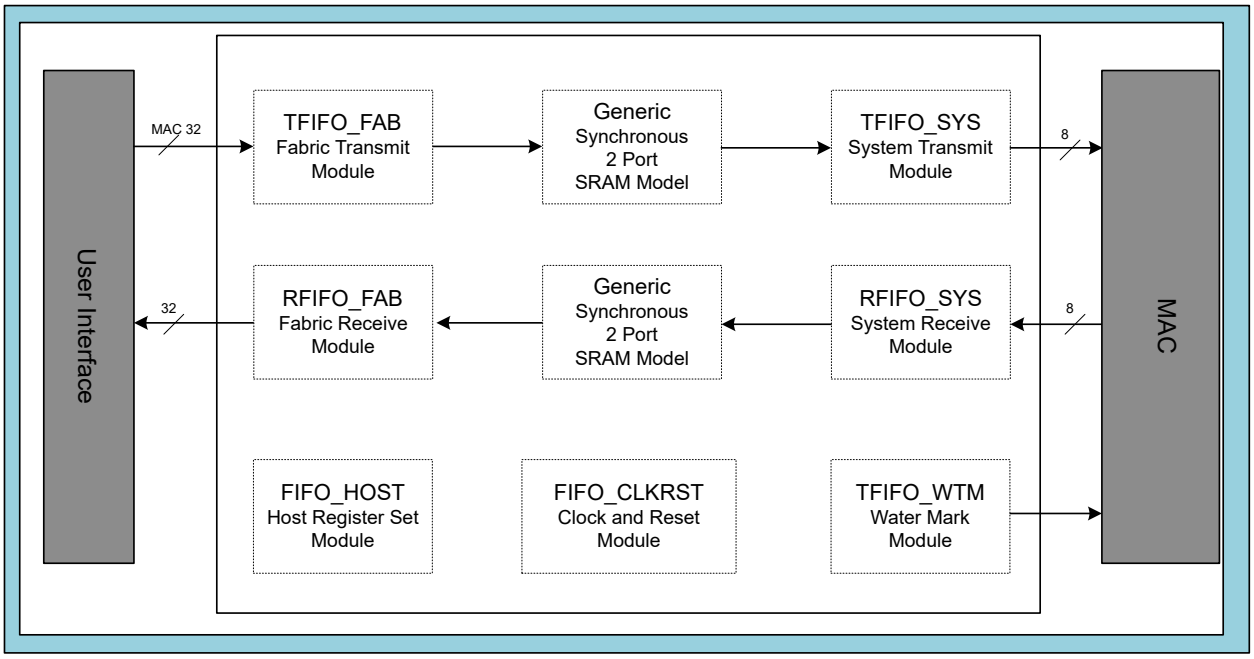
The MDIO write/read cycles are requested through the APB target. MAC performs a write cycle using the MDIO_PHYID, register address and 16-bit write data. MAC performs a read cycle using the MDIO_PHYID register address and updates the sixteen-bit read data into the MDIO Management STATUS Register, which can be read through APB target.

1.11 MAC FIFO

This core provides data queuing for increased throughput and sits between back-end, user-interface logic, and MAC core. The core provides clock-domain crossing, automatic pause frame handshaking, and graceful frame dropping.

The data is buffered between the system-interface and the MAC core by transmit and receive FIFOs. The FIFO size can be configured with PACKET_SIZE parameter.

Figure 1-2. MAC-FIFO Functional Block Diagram



Each RAM has additional associated control bits, which are additional to maximum frame data size.

Table 1-1. MAC-FIFO RAM Configurations

PACKET_SIZE Parameter (Bytes)	Transmit RAM		Receive RAM	
	RAM Size in Bits	Number of Address bits (TABITS)	RAM Size in Bits	Number of Address bits (RABITS)
256	64 x 39	6	128 x 36	7
512	128 x 39	7	256 x 36	8
1K	256 x 39	8	512 x 36	9
2K	512 x 39	9	1K x 36	10
4K	1K x 39	10	2K x 36	11
8K	2K x 39	11	4K x 36	12
16K	4K x 39	12	8K x 36	13
32K	8K x 39	13	16K x 36	14

1.12 Station Address Logic for Frame Filtering

This module provides a mechanism to statistically filter frames not intended for this node.

The MAC core performs DA comparison on all the received frames and provides three information signals: UCAD (Perfect DA match), MCAD, and BCAD along with seven most significant bits of the resulting CRC of DA. This information is used to perform a hashing algorithm, compare the result to a programmable hash table and then communicate to the FIFO logic to either delete or store the frame.

The programmability allows the user to assert any bits in a 128 bit hash table that corresponds to the desired Ethernet MAC DA. If the corresponding bit in the table is set, the frame is accepted. In addition, hashing can selectively be performed on unicast addresses or multicast addresses.

1.13 Statistics Counters Logic

This module has separate counters, which simply counts or accumulate conditions that occur upon packets transmitted and received. These counters support remote network monitoring (RMON) management information base (MIB) group 1, RMON MIB group 2, RMON MIB group 3, RMON MIB group 9, RMON MIB 2, and the dot 3 Ethernet MIB.

1.14 SGMII/Ten-Bit Interface

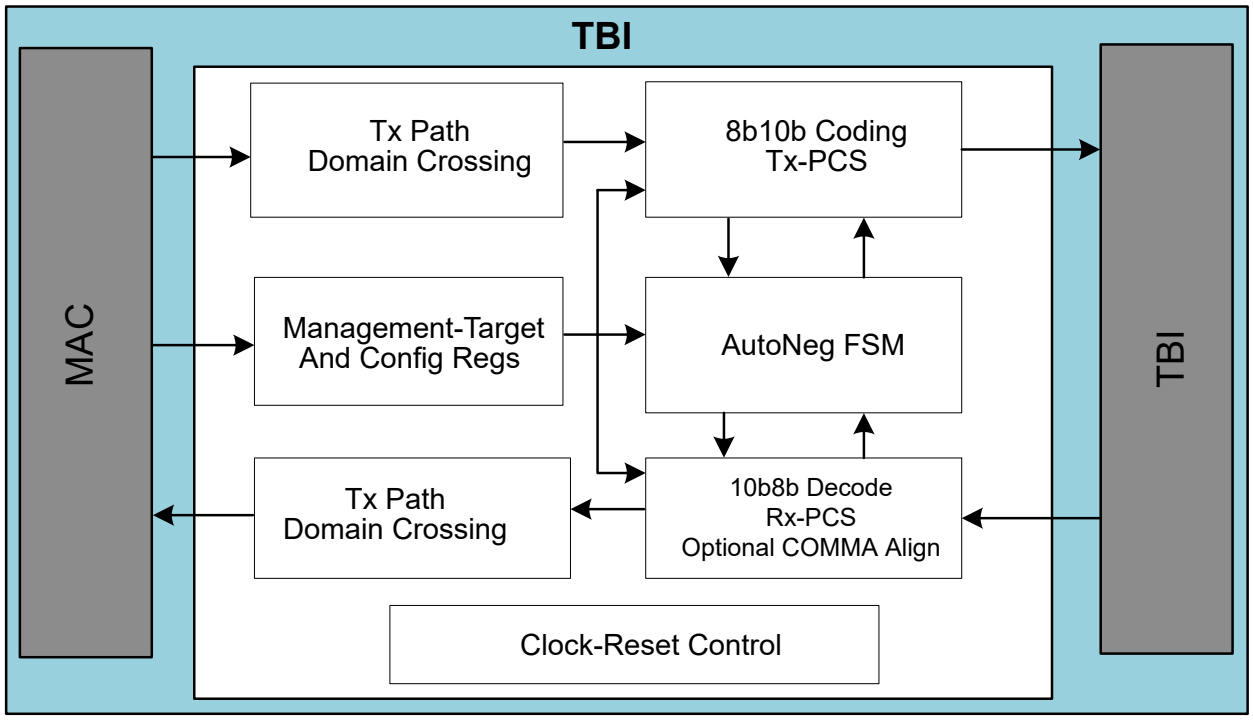
This module takes the transmit G/MII data stream, encodes it into 10-bit symbols and presents 10-bit interface data to Transceiver. Packet data replication is used to match data rates for the different modes of the MII to the transmit clock. In the receive direction de-serialized 10-bit symbols are decoded and converted into the receive G/MII signal set. Packet data under sampling is used to match data rates for the different modes of the MII to the TBI receive clock.

The design uses transmit, receive, and synchronization state machines as specified in Clause 36 of IEEE 802.3z. Also included auto-negotiation (AN) for 1000BASE-X, which is used to exchange information between the link partners. This module is managed and monitored through the MDIO management interface. The extended set of management registers is provided.

Both the transmit and receive paths leverage the physical coding sub layer and the Auto-negotiation sub-layers of the IEEE 802.3z specification, as contained in Clauses 36 and 37. For complete clock domain isolation of the TBI from the MAC, both transmit and receive elasticity FIFOs are used.

The control information exchanged differs from the IEEE specification. Instead of using the ability advertisement, the PHY sends the control information through its Tx_config_Reg [15:0], as listed in Table 1-2. Upon receiving control information, the MAC acknowledges the update of the control information by asserting bit 14 of its Tx_config_Reg [15:0].

Figure 1-3. SGMII/TBI Functional Block Diagram



To maintain a constant clock frequency at the PHY interface for all MAC speeds, the MII bus data must be replicated internally to the TBI. Nibble packet data transmitted by a 100 Mbps MAC must be aligned, concatenated, and replicated 10 times. Nibble packet data transmitted by a 10 Mbps MAC must be aligned, concatenated, and replicated 100 times.

Table 1-2. SGMII/TBI Auto-Negotiation Control Information Sent/Received

Bit	Tx_config from PHY to MAC	Tx_config from MAC to PHY
15	Link: • 1: Link up • 0: link down	0: Reserved
14	Reserved for AN ACK.	1
13	0: Reserved	0: Reserved
12	Duplex mode: • 1: Full • 0: Half	0: Reserved
[11:10]	Speed: • 00:10 Mbps • 01:100 Mbps • 10:1000 Mbps • 11: Reserved	0: Reserved
[9:1]	0: Reserved	0: Reserved
0	1	1

Packet data received by the TBI through the PHY must be under sampled by a factor of 10 before being sent to a 100 Mbps MAC. Packet data received by the TBI through the PHY must be under sampled by a factor of 100 before being sent to a 10 Mbps MAC. For half-duplex functionality, carrier sense is inferred from RXDV, and collision is derived from the simultaneous assertion of TXEN and RXDV.

1.15 COMMA Alignment Logic

The PHY layer includes COMMA alignment logic in the receive path. This logic detects COMMA data and aligns the 10-bit data to the proper word boundary before passing the data to the receive path.

2. Programmer Guide

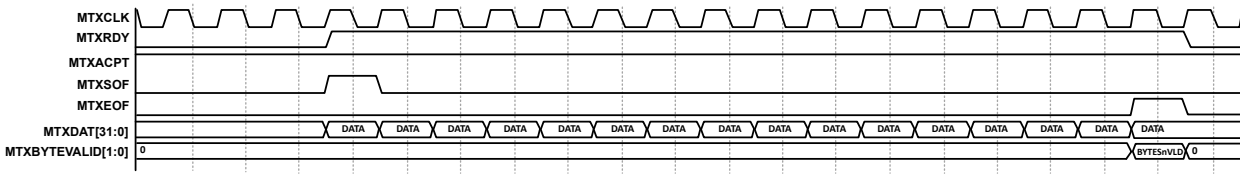
This section has all the information regarding utilization of the core.

2.1 Functional Overview

The MAC Data interface module is interfaced with MAC transmit FIFO for transmit data and MAC receive FIFO for receive data operations. The transmit and receive operations are described in Figure 2-1 and Figure 2-2 respectively.

2.1.1 Transmit Operation

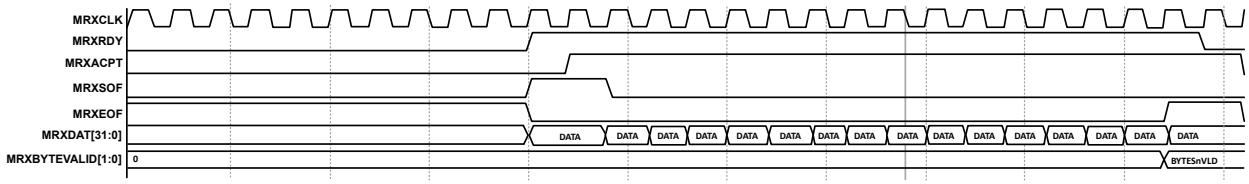
Figure 2-1. Transmit Operation



The MTXDAT(transmit data) word is recorded into MAC transmit FIFO on rising edge of MTXCLK upon the assertion of MTXRDY and MTXACPT and the MTXSOF should be asserted for the first word transfer of the frame. Transmit data stored into MAC transmit FIFO until MTXEOF (end of frame date). MTXBYTEVALID indicates the byte enables of the MTXDAT last word. MTXACPT is asserted when CoreTSE is capable of receiving at least one word from the MAC data path transmit interface. MTXACPT should be monitored for every transmission.

2.1.2 Receive Operation

Figure 2-2. Receive Operation



The core asserts the MRXRDY along with MRXSOF and MRXDAT (receive data) and waits for the MRXACPT. MRXDAT word is available on rising edge of MRXCLK from the MAC receive FIFO until MRXEOF (end of frame date). MRXBYTEVALID indicates the byte enables of the MRXDAT last word.

3. Register Map

The external APB initiator uses a 32-bit APB target interface for accessing control and status registers.

Table 3-1. Core Register MAP

Address Offset	Function
0x000–0x044	Access to MAC core registers
0x048–0x07C	Access to FIFO core registers
0x080–0x1BF	Access to Statistics Counters core registers 0x080–0x13C are valid addresses
0x1C0–0x1FF	Access to System Registers (SAL and miscellaneous controls) 0x1C0–0x1D4 are valid addresses.

3.1 MAC Core Registers

This section describes the MAC core registers used for the CoreTSE.

Table 3-2. Control/Status Registers

Address[9:0]	Function
0x000	MAC Configuration #1 **[31] (R/W) SOFT RESET: Default 1** Setting this bit puts all modules within the MAC in reset except the APB target interface. **[30:9] Reserved** **[8] (R/W) LOOP BACK: Default 0** Setting this bit causes the PETFN MAC Transmit outputs to be looped back to the MAC Receive inputs. Clearing this bit results in normal operation. **[7:6] Reserved** **[5] (R/W) RECEIVE FLOW CONTROL ENABLE: Default 0** Setting this bit causes the PERFN Receive MAC Control to detect and act on PAUSE Flow Control frames. Clearing this bit causes the Receive MAC Control to ignore PAUSE Flow Control frames. **[4] (R/W) TRANSMIT FLOW CONTROL ENABLE: Default 0** Setting this bit allows the PETMC Transmit MAC Control to send PAUSE Flow Control frames when requested by the system. Clearing this bit prevents the Transmit MAC Control from sending Flow Control frames. **[3] (RO) SYNCHRONIZED RECEIVE ENABLE:** Receive Enable synchronized to the receive stream. **[2] (R/W) RECEIVE ENABLE: Default 0** Setting this bit allows the MAC to receive frames from the PHY. Clearing this bit prevents the reception of frames. **[1] (RO) SYNCHRONIZED TRANSMIT ENABLE:** Transmit Enable synchronized to the transmit stream. **[0] (R/W) TRANSMIT ENABLE: Default 0** Setting this bit allows the MAC to transmit frames from the system. Clearing this bit prevents the transmission of frames.

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Address[9:0]	Function
0x004	MAC Configuration #2 **[31:16] Reserved** **[15:12] (R/W) PREAMBLE LENGTH: Default 0x7** This field determines the length of the preamble field of the packet, in bytes. Minimum value supported for this field is 0x3. **[11:10] Reserved** **[9:8] (R/W) INTERFACE MODE: Default 0x10** This field determines the type of MAC interface mode. • 2'b00: MAC Tx/Rx represents MII 10Mbps interface (Nibble Mode). • 2'b01: MAC Tx/Rx represents MII 100Mbps interface (Nibble Mode). • 2'b10: MAC Tx/Rx represents GMII 1000Mbps interface (Byte Mode). • 2'b11: Reserved. **[7:6] Reserved** **[5] (R/W) HUGE FRAME ENABLE: Default 0** Setting this bit allows frames longer than the MAXIMUM FRAME LENGTH to be transmitted and received. Clear this bit to have the MAC limit the length of frames at the MAXIMUM FRAME LENGTH value. (Maximum Frame Length is set in separate Maximum Frame Length register.) **[4] (R/W) LENGTH FIELD CHECKING: Default 0** Setting this bit causes the MAC to check the frame's length field to ensure it matches the actual data field length. Clear this bit if no length field checking is desired. **[3] Reserved** **[2] (R/W) PAD/CRC ENABLE: Default 0** Set this bit to have the MAC pad all short frames and append a CRC to every frame whether or not padding was required. Clear this bit if frames presented to the MAC have a valid length and contain a CRC. **[1] (R/W) CRC ENABLE: Default 0** Set this bit to have the MAC append a CRC to all frames. Clear this bit if frames presented to the MAC have a valid length and contain a valid CRC. If the PAD/CRC ENABLE Configuration bit or the per-packet PAD/CRC ENABLE is set, CRC ENABLE is ignored. **[0] (R/W) FULL-DUPLEX: Default 0** Setting this bit configures the MAC to operate in full-duplex mode. Clearing this bit configures the MAC to operate in half-duplex mode only.

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Address[9:0]	**Function**
0x008	IPG/IFG **[31] Reserved** **[30:24] (R/W) NON-BACK-TO-BACK INTER-PACKET-GAP PART1 (IPGR1):** This programmable field represents the optional carrier sense window referenced in IEEE 802.3/4.2.3.2.1 Carrier Deference. If a carrier is detected during the timing of IPGR1, the MAC defers to the carrier. If, however, the carrier becomes active after IPGR1, the MAC continues timing IPGR2 and transmits, knowingly causing a collision. This ensures fair access to the medium. The permitted range of values is 0x0 to IPGR2. Default is 0x40 (64d) which follows the two-thirds/one-thirds guideline. **[23] Reserved** **[22:16] (R/W) NON-BACK-TO-BACK INTER-PACKET-GAP PART2 (IPGR2):** This programmable field represents the Non-Back-to-Back Inter-Packet-Gap in bit times. Default is 0x60 (96d), which represents the minimum IPG of 96 bits. **[15:8] (R/W) MINIMUM IFG ENFORCEMENT: Default 0x50** This programmable field represents the minimum size of IFG to enforce between frames (expressed in bit times). A frame whose IFG is less than that programmed is dropped. The default setting of 0x50 (80d) represents half of the nominal minimum IFG which is 160 bits. **[7] Reserved** **[6:0] (R/W) BACK-TO-BACK INTER-PACKET-GAP: Default 0x60** This programmable field represents the IPG between Back-to-Back packets (expressed in bit times). This is the IPG parameter used exclusively in full-duplex mode when two transmit packets are sent back-to-back. Set this field to the desired number of bits. The default setting of 0x60 (96d) represents the minimum IPG of 96 bits. Minimum value supported for this field is 0x28 (40d).

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Address[9:0]	Function
0x00C	Half-Duplex **[31:24] Reserved** **[23:20] (R/W) ALTERNATE BINARY EXPONENTIAL BACKOFF TRUNCATION: Default 0xA** This field is used when ALTERNATE BINARY EXPONENTIAL BACKOFF ENABLE is set. The value programmed is substituted for the Ethernet standard value of ten. **[19] (R/W) ALTERNATE BINARY EXPONENTIAL BACKOFF ENABLE: Default 0** Setting this bit configures the Tx MAC to use the ALTERNATE BINARY EXPONENTIAL BACKOFF TRUNCATION setting instead of the 802.3 standard tenth collisions. The Standard specifies that any collision after the tenth uses 210-1 as the maximum backoff time. Clearing this bit causes the Tx MAC to follow the standard binary exponential backoff rule. **[18] (R/W) BACKPRESSURE NO BACKOFF: Default 0** Setting this bit configures the Tx MAC to immediately re-transmit following a collision during back pressure operation. Clearing this bit causes the Tx MAC to follow the binary exponential back off rule. **[17] (R/W) NO BACKOFF: Default 0** Setting this bit configures the Tx MAC to immediately re-transmit following a collision. Clearing this bit causes the Tx MAC to follow the binary exponential back off rule. **[16] (R/W) EXCESSIVE DEFER: Default 1** Setting this bit configures the Tx MAC to allow the transmission of a packet that has been excessively deferred. Clearing this bit causes the Tx MAC to abort the transmission of a packet that has been excessively deferred. **[15:12] (R/W) RETRANSMISSION MAXIMUM: Default 0xF** This is a programmable field specifying the number of retransmission attempts following a collision before aborting the packet due to excessive collisions. The Standard specifies the maximum number of attempts to be 0xF (15d). **[11:10] Reserved** **[9:0] (R/W) COLLISION WINDOW: Default 0x37** This programmable field represents the slot time or collision window during which collisions might occur in a properly configured network. Since the collision window starts at the beginning of transmission, the preamble and SFD are included. The default of 0x37 (55d) corresponds to the count of frame bytes at the end of the window.
0x010	Maximum Frame Length **[31:16] Reserved** **[15:0] (R/W) MAXIMUM FRAME LENGTH: Default 0x07D0 (2000 d)** This programmable field sets the maximum frame size in both the transmit and receive directions.
0x014	Control Frame extended parameter (Used for pause frame) **[31:16] Reserved** **[15:0] (R/W) CFEP: Default 0x0000** This register bits are append as Pause frame payload.
0x018	Control Frame parameter (Used for pause Value) **[31:16] Reserved** **[15:0] (R/W) CFPT: Default 0xFFFF** This register bits are append as Pause frame payload.

.....continued	
Address[9:0]	**Function**
0x01C	Test Register **[31:4] Reserved** **[3] (R/W) MAXIMUM BACKOFF: Default 0** Setting this bit causes the MAC to back off for the maximum possible length of time. This test bit is used to predict back off times in Half-Duplex mode. **[2] (R/W) REGISTERED TRANSMIT FLOW ENABLE: Default 0** Registered Transmit half-duplex Flow Enable. **[1] (R/W) TEST PAUSE: Default 0** Setting this bit allows the MAC to be paused through the APB target interface for testing purposes. **[0] (R/W) SHORTCUT SLOT TIME: Default 0** Setting this bit allows the slot time counter to expire regardless of the current count. This bit is for testing purposes only. Upon PAUSE condition frame transmission gets paused until slot time counter reached ‘h7e for 1G and ‘h3e non 1G modes and it can be overcome by writing 1 to this bit.
0x020	MDIO Mgmt: Configuration **[31] (R/W) RESET MDIO MGMT: Default 0** Setting this bit resets MDIO Mgmt. Clearing this bit allows MDIO Mgmt to perform Mgmt read/write cycles as requested via the APB target interface. **[30:6] Reserved** **[5] (R/W) SCAN AUTO INCREMENT: Default 0** Setting this bit causes MDIO Mgmt to continually read from a set of PHYs of contiguous address space. The starting address of the PHY is specified by the content of the PHY address field recorded in the MDIO Mgmt Address register. The next PHY to be read is PHY address + 1. The last PHY to be queried in this read sequence is the one residing at address 0x31, after which the read sequence returns to the PHY specified by the PHY address field. **[4] (R/W) PREAMBLE SUPPRESSION: Default 0** Setting this bit causes MDIO Mgmt to suppress preamble generation and reduce the Mgmt cycle from 64 clocks to 32 clocks. This is in accordance with IEEE 802.3/22.2.4.4.2. Clearing this bit causes MDIO Mgmt to perform Mgmt read/write cycles with the 64 clocks of preamble. **[2:0] (R/W) MGMT CLOCK SELECT: Default 0x0** This field determines the clock frequency of the Mgmt Clock (MDC). The following list of MDC select encoding determines how to program this field. PCLK is the source clock. • 3’b000/3’b001: Source clock divided by 4 • 3’b010: Source clock divided by 6 • 3’b011: Source clock divided by 8 • 3’b100: Source clock divided by 10 • 3’b101: Source clock divided by 14 • 3’b110: Source clock divided by 20 • 3’b111: Source clock divided by 28

.....continued	
Address[9:0]	**Function**
0x024	MDIO Mgmt: Command**[31:2] Reserved** **[1] (R/W) SCAN CYCLE: Default 0** This bit causes MDIO Mgmt to perform Read cycles continuously. This is useful for monitoring Link Fail. **[0] (R/W) READ CYCLE: Default 0** This bit causes MDIO Mgmt to perform a single Read cycle. The Read data is returned in MDIO Mgmt STATUS Register.
0x028	MDIO Mgmt: Address **[31:13] Reserved** **[12:8] (R/W) PHY ADDRESS: Default 0x0** This field represents the 5-bit PHY Address field used in Mgmt cycles. Up to 31 PHYs can be addressed. **[7:5] Reserved** **[4:0] (R/W) REGISTER ADDRESS: Default 0x0** This field represents the 5-bit Register Address field of Mgmt cycles.
0x02C	MDIO Mgmt: Control **[31:16] Reserved** **[15:0] (WO) MDIO MGMT CONTROL (PHY Control):Default 0x0** When written, an MDIO Mgmt write cycle is performed using the 16-bit data and the preconfigured PHY and Register addresses from the MDIO Mgmt Address Register.
0x030	MDIO Mgmt: Status **[31:16] Reserved** **[15:0] (RO) MDIO MGMT STATUS (PHY STATUS):** Following an MDIO Mgmt Read Cycle, the 16-bit data can be read from this location.
0x034	MDIO Mgmt: Indicators **[31:3] Reserved** **[2] (RO) NOT VALID: Default 0** When 1 is returned-indicates MDIO Mgmt Read cycle has not completed and the Read Data is not yet valid. **[1] (RO) SCANNING: Default 0** When 1 is returned-indicates a scan operation (continuous MDIO Mgmt Read cycles) is in progress. **[0] (RO) BUSY: Default 0** When 1 is returned-indicates MDIO Mgmt block is currently performing an MDIO Mgmt Read or Write cycle.

.....continued	
Address[9:0]	**Function**
0x038	Interface Control **[31:8] Reserved** **[7] (W/R) WoL: Unicast match enable: Default 0** Setting this bit configures WoL module to enable Wake On Lane Detected assertion based on Unicast match. **[6] (W/R) WoL: Magic Packet detection enable: Default 0** Setting this bit configures WoL module to enable Wake On Lane Detected assertion based on magic packet detection. **[5] (W/R) WoL: Wake On Lane Detected Clear status clear: Default 0** When this bit is asserted, Wake On Lane Detected status is held low. When this bit is cleared, Wake On Lane Detected may become asserted appropriately. **[4] (W/R) Stats Counters – Auto clear counters on read: Default 0** Setting this bit enables auto-clear-on-read feature for all the counters. **[3] (W/R) Stats Counters – Clear All counters: Default 0** Setting this bit clears all the statistics counters. **[2] (W/R) Stats Counters – Module enable: Default 0** Setting this bit enables statistics counter module. **[1:0] Reserved**
0x03C	Interface Status **[31:11] Reserved** **[10] (RO/LH) Wake On Lane Detected:** This bit is only used when the optional WoL module is integrated It is set when the MAC detects a Magic Packet and stays high until it is cleared by the assertion of Wake On Lane Detected Clear. Its reset value is low. **[9] (RO/LH) EXCESS DEFER:** This bit sets when the MAC excessively defers a transmission. It clears when read. This bit latches high. Excessive Deferred is a condition when the MAC has deferred sending a packet for a time longer than the length of two maximum length frames. **[8:4] Reserved** **[3] (RO) LINK FAIL:** When read as a 1, the MDIO management module has read the PHY link fail register to be 1. When read as a 0, the MDIO management module has read the PHY link fail register to be 0. Note that for asynchronous host accesses, this bit must be read at least once every scan read cycle of the PHY. **[2:0] Reserved**
0x040	Station Address Lower Register-Default 0x0000_0000 **[31:24] (W/R) First octet of the DA in the frame** **[23:16] (W/R) Second octet of the DA in the frame** **[15: 8] (W/R) Third octet of the DA in the frame** **[7: 0] (W/R) Fourth octet of the DA in the frame**

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Address[9:0]	**Function**
0x044	Station Address Higher Register Default 0x0000_0000 **[31:24] (W/R) Fifth octet of the DA in the frame** **[23:16] (W/R) Sixth octet of the DA in the frame** **[15:0] Reserved**

3.2 MAC-FIFO Core Registers

This section describes the MAC-FIFO Core Registers of the CoreTSE.

Table 3-3. MAC-FIFO Core Registers

Address[9:0]	Function
0x048	MAC-FIFO Configuration Register 0 **[31:21] Reserved** **[20] (RO) Fabric transmit module enable status (ftfenrply): Default 0** When asserted, the Fabric transmit module is enabled. When negated, the Fabric transmit module is disabled. The bit should be polled until it reaches the expected value. **[19] (RO) System transmit module enable status (stfenrply): Default 0** When asserted, the System transmit module is enabled. When negated, the System transmit module is disabled. The bit should be polled until it reaches the expected value. **[18] (RO) Fabric receive module enable status (frfenrply): Default 0** When asserted, the Fabric receive module is enabled. When negated, the Fabric receive module is disabled. The bit should be polled until it reaches the expected value. **[17] (RO) System receive module enable status (srfenrply): Default 0** When asserted, the System receive module is enabled and start of packet has been received. When negated, the System receive module is disabled and end-of-frame signal is received. **[16] (RO) Water mark module enable status(wtmenrply): Default** When asserted, the Water mark module is enabled. When negated, the Water mark module is disabled. The bit should be polled until it reaches the expected value. **[15:13] Reserved** **[12] (R/W) Fabric transmit module enable request(ftfenreq): Default 0** When asserted, requests enabling of the Fabric transmit module. When negated, requests disabling of the Fabric transmit module. **[11] (R/W) System transmit module enable request (stfenreq): Default 0** When asserted, requests enabling of the System transmit module. When negated, requests disabling of the System transmit module. **[10] (R/W) Fabric receive module enable request(frfenreq): Default 0** When asserted, requests enabling of the Fabric receive module. **[9] (R/W) System receive module enable request(srfenreq): Default 0** When asserted, requests enabling of the System receive module. When negated, requests disabling of the System receive module. **[8] (R/W) Water mark module enable request(wtmenreq): Default 0** When asserted, requests enabling of the Water mark module. When negated, requests disabling of the Water mark module. **[7:5] Reserved** **[4] (R/W) Host fabric transmit module reset (hstrstft): Default 1** When asserted this bit places fabric transmit module in reset. **[3] (R/W) Host MAC transmit module reset (hstrstst): Default 1** When asserted this bit places the System transmit module in reset. **[2] (R/W) Host fabric receive module reset (hstrstfr): Default 1** When asserted this bit places the fabric receive module in reset. **[1] (R/W) Host MAC receive module reset (hstrstsr): Default 1** When asserted this bit places the System receive module in reset. **[0] (R/W) Host transmit watermark module reset (hstrstwt): Default 1** When asserted this bit places the transmit watermark module in reset.

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Address[9:0]	Function
0x04C	MAC-FIFO Configuration Register 1 **[31:(RABITS+16)] Reserved** **[(RABITS+15):16] (R/W) system receive for cut through threshold (cfgsrth)** **[RABITS:0]:Default {(RABITS) {1'b1}}** This hex value represents the minimum number of 4 byte locations that simultaneously stores in the receive RAM, relative to the beginning of the frame being input, before fabric-receive-ready signal (frrdy) may be asserted. Note that frrdy latents a certain amount of time due to fabric transmit clock to system transmit clock time domain crossing, and conditional on fabric-receive-accept signal (fracpt) assertion. When set to maximum value, frrdy may be asserted only after the completion of the input frame. The value of this register must be greater than 18d when hstdrplt64 is asserted. The register length is shown for a receive RAM with 12 address bits (16KB). **[15:0] (R/W) number of pause quantas before xoff retransmission (cfgxoffrtx): Default 0xFFFF** This hex value represents the number of pause quanta (64 bit times) after an XOFF pause frame has been acknowledged until the MAC-FIFO re-asserts Transmit-Control Frame-Request (tcrq) if the MAC-FIFO receive storage level has remained higher than the low watermark.
0x050	MAC-FIFO Configuration Register 2 **[31: (RABITS+17)] Reserved** **[(RABITS+16):16] (R/W) Max words in receive FIFO (cfghwm) [RABITS+1:0]: Default {(RABITS + 1) { 1'b1 }}** Once the receive FIFO reach the configured water mark level (cfghwm) MAC-FIFO sends XOFF pause control frame. Each hex value represents 4 byte locations that simultaneously stores in the receive RAM. **[15:(RABITS+1)] Reserved** **[RABITS:0] (R/W) Min words in receive FIFO before (cfglwm) [RABITS+1:0]: Default {(RABITS + 1) { 1'b1 }}** Once the receive RAM reaches the cfglwm, XON (transmit ON) pause control frame transmits in response to a previously transmitted XOFF pause control frame. Each hex value represents 4 byte locations that simultaneously stores in the receive RAM.
0x054	MAC-FIFO Configuration Register 3 **[31: (TABITS+17)] Reserved** **[(TABITS+16):16] (R/W) Max number of words in transmit FIFO (cfghwmft) [TABITS+1:0]: Default {(TABITS + 1){1'b1}}** This hex value represents the maximum number of 4 byte locations that simultaneously stores in the transmit RAM before MTXHWM asserts. Note that MTXHWM has two MTXCLK clock periods of latency before assertion or negation. This should be considered when calculating any headroom required for maximum size packets. The register length is shown for a transmit RAM with 11 address bits (8KB). The register length varies with the configured transmit RAM size. **[15: (TABITS+1)] Reserved** **[TABITS:0] (R/W) fabric transmit cut through threshold (cfgftth) [TABITS + 1:0]: Default {(TABITS+1){ 1'b1 }}** Once the transmit FIFO reaches the cut through threshold (cfgftth), MAC core informs to start frame transmission. Each hex value represents 4 byte locations that simultaneously stores in the transmit RAM.

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Address[9:0]	**Function**
0x058	MAC-FIFO Configuration Register 4 **[31:18] Reserved** **[17:0] (R/W) Host filter frames (hstfltrfrm)[17:0]: Default 0x8** These configuration bits are used to signal the drop frame conditions internal to the MAC-FIFO. The setting of this bits along with respective don't care values in the hstfltrfrmdc configuration registers, create to drop the received packet by the System. For example, if it is desired to drop a frame that contains a FCS Error, bit 4 would be set. • 17: Unicast frame detected but did not match configured station address. • 16: Receive Frame Truncated. • 15: Receive Long Event. • 14: Receive VLAN Tag Detected: Frame's length/type field contained 0x8100 which is the VLAN Protocol Identifier. • 13: Receive Unsupported Op-code: Current Frame was recognized as a Control frame by the PEMCS, but it contains an unknown Op-code. • 12: Receive PAUSE Control Frame: Current frame was recognized as a Control frame containing a valid PAUSE Frame Op-code and a valid address. • 11: Receive Control Frame: Current Frame was recognized as a Control frame for having a valid Type-Length designation. • 10: Receive Dribble Nibble: Indicates that after the end of the packet an additional 1 to 7 bits were received. A single nibble, called the dribble nibble, is formed but not sent to the system (10/100 Mbps only). • 9: Receive Broadcast: Packet's destination address contained the broadcast address. • 8: Receive Multicast: Packet's destination address contained a multicast address. • 7: Receive OK. Frame contained a valid CRC and did not have a code error. • 6: Receive Length Out of Range: Indicates that frame's length was larger than 1,518 bytes but smaller than the host's maximum frame length value (type field). • 5: Receive Length Check Error: Indicates that frame length field value in the packet does not match the actual data byte length and is not a type field. • 4: Receive CRC Error: Packet's CRC did not match the internally generated CRC. • 3: Receive Code Error: One or more nibbles were signaled as errors during the reception of the packet. • 2: Receive False Carrier: Indicates that at some time since the last receive statistics vector, a false carrier was detected, noted, and reported with this the next receive statistics. The false carrier is not associated with this packet. False carrier is an activity on the receive channel that does not result in a packet receive attempt being made. Defined to be RXER = 1, RXDV = 0, RXD[3:0] = 0xE (RXD[7:0] = 0x0E). • 1: Receive RXDV Event: Indicates that the last receive event seen was not long enough to be a valid packet. • 0: Receive Previous Packet Dropped as IFG is small.

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Address[9:0]	Function
0x05C	MAC-FIFO Configuration Register 5 **[31:23] Reserved** **[22] (R/W) Half Duplex Indicator (cfghdplx): Default 0x0** Assertion of this bit configures the MAC-FIFO to enable half-duplex back pressure as a flow control mechanism. De-assertion of this bit configures the MAC-FIFO to enable pause frames as a flow control mechanism. **[21] (RO) System receive FIFO full (srfull): Default 0x0** Assertion of this read-only bit indicates that the maximum capacity of the receive FIFO storage has been met or exceeded. **[20] (R/W) Host clear System receive FIFO full (hstsrfullclr): Default 0x0** This bit should be written asserted when it is desired to clear the srfull indicator bit. After hstfullclr assertion, srfull should be read until it becomes unasserted. Hstfullclr should then be written unasserted for the indicator to become operational again. **[19] (R/W) One byte transfer per system clock (cfgbytmode): Default 0x1** This bit should be asserted when data is transferred at the tpd and rpd bus at a rate of one byte per qualified clock. This bit should be negated when data is transferred at the tpd and rpd bus at a rate of one nibble per qualified clock. This bit should therefore be asserted when the MAC is configured for GMII mode. **[18] (R/W) Host drop frames less than 64 bytes (hstdrplt64): Default 0x0** Setting this bit causes the frame to be dropped if a receive frame is less than 64 bytes in length. **[17:0] (R/W) Host dont care for filtering of frmes (hstfltrfrmdc) [17:0]: Default 0x3FFF7** The hstfltrfrmdc [17:0] configuration bits indicate which Receive Statistics Vectors are don’t cares for MAC-FIFO frame drop circuitry. Setting of an hstfltrfrmdc bit, indicates a don’t care for that hstfltrfrm bits. Clearing the bit looks for a matching level on the corresponding hstfltrfrm bit. If a match is made then the frame is dropped.

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Address[9:0]	Function
0x060	MAC-FIFO FIFO RAM Access* Register 0 **[31] (R/W) Host transmit RAM write request (hsttramwreq): Default 0x0** Host transmit RAM write request. Requests the handshake of hsttramwdat and hsttramwadx values to the transmit FIFO RAM. Should only be asserted while hsttramwack is negated and while the transmit data path is disabled from receiving data and is in a steady state. It should only be negated after receiving an asserted hsttramwack. **[30] (RO) Host transmit RAM write acknowledge (hsttramwack): Default 0x0** Host transmit RAM write acknowledge. Signifies the acceptance of hsttramwdat and hsttramwadx values to the transmit FIFO RAM or FIFO Transmit module. Will only be asserted or negated following assertion or negation of hsttramwreq. This is a read-only bit. Writes specifically to this bit have no effects. **[29:24] Reserved** **[23:16] (R/W) Host transmit RAM write data (hsttramwdat [39:32]): Default 0x00** Host transmit RAM write data. This is the upper byte of transmit FIFO RAM data that is written at the address of hsttramwadx [(TABITS-1):0] if hsttramwadx [TABITS+1] is negated and hsttramwreq is asserted. This part of the transmit FIFO RAM contains control information for the frame as follows: • hsttramwdat[39] = FIFO Transmit Control Frame (1'b1 for control frame) • hsttramwdat[38] = Reserved • hsttramwdat[37] = FIFO Transmit Per-Packet PAD Mode • hsttramwdat[36] = FIFO Transmit Per-Packet enable • hsttramwdat[35] = FIFO Transmit Per-Packet Generate FCS • hsttramwdat[34] = FIFO Transmit end of packet • hsttramwdat[33:32] = FIFO Transmit data valid, applicable only for the last word of the frame • 0: Indicates all bytes in the word are valid. • 1: Indicates the LSB 3 bytes are valid [23:0] bits. • 2: Indicates the LSB 2 bytes are valid [15:0] bits. • 3: Indicates the LSB 1 bytes are valid [7:0] bits. **[15:(TABITS+2)] Reserved** **[(TABITS+1):0] (R/W) Host transmit RAM write address (hsttramwadx [(TABITS+1):0]): Default (TABITS+2) {1'b0}** Host transmit RAM write address. This field has different functionality based on the value of hsttramwadx [(TABITS+1)] and whether it is being written to or read from. When read from, hsttramwadx [TABITS:0] field contains the actual write pointer value of the FIFO Transmit module. When written to the hsttramwadx register is loaded. If hsttramwadx[TABITS+1] is low, hsttramwadx [(TABITS-1):0] transmits the RAM address which hsttramwdat is written to. If hsttramwadx [TABITS+1] is high, hsttramwadx [TABITS:0] contains the pointer value that is written to FIFO Transmit module.
0x064	MAC-FIFO FIFO RAM Access* Register 1 **[31:0] (R/W) Host transmit RAM write data (hsttramwdat[31:0]): Default 0x00** Host transmit RAM write data. This is the lower 4 bytes of transmit FIFO RAM data that is written at the address of hsttramwadx[(TABITS-1):0] if hsttramwadx[(TABITS+1)] is negated and hsttramwreq is asserted.

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Address[9:0]	Function
0x068	MAC-FIFO FIFO RAM Access* Register 2 **[31] (R/W) Host transmit RAM read request. (hsttramrreq): Default 0x0** Host transmit RAM read request. Requests the handshake of hsttramradx values to the transmit FIFO RAM and hsttramrdat from the transmit FIFO RAM. Should only be asserted while hsttramrack is negated and while the transmit data path is disabled from receiving data and is in a steady state. It should only be negated after receiving an asserted hsttramrack. **[30] (RO) Host transmit RAM read acknowledge (hsttramrack): Default 0x0** Host transmit RAM read acknowledge. Signifies the acceptance of hsttramradx values to the transmit FIFO RAM and reception of hsttramrdat from the transmit FIFO RAM location addressed. Will only be asserted or negated following assertion or negation of hsttramrreq. This is a read-only bit. Writes specifically to this bit have no effects. **[29:24] Reserved** **[23:16] (RO) Host transmit RAM read data (hsttramrdat[39:32]): Default 0x0** Host transmit RAM read data. This is the upper byte of transmit FIFO RAM data that was read at the address of hsttramwadx[(TABITS-1):0] if hsttramwadx[(TABITS+1)] is negated and hsttramwreq is asserted. This part of the transmit FIFO RAM contains control information for the frame as follows: • hsttramrdat[39] = ‘1’/’0’ - Control Frame/ non control frame. • hsttramrdat[38:37] = FIFO receive Per-Packet PAD Mode. • hsttramrdat[38:37] = FIFO receive Per-Packet PAD Mode. • hsttramrdat[35] = FIFO receive Per-Packet Generate FCS. • hsttramrdat[34] = FIFO receive end of frame. • hsttramrdat[33:32] = Valid byte enables and applicable only for the last word of the frame. • 0: Indicates all bytes in the word are valid. • 1: Indicates the LSB 3 bytes are valid [23:0] bits. • 2: Indicates the LSB 2 bytes are valid [15:0] bits. • 3: Indicates the LSB 1 bytes are valid [7:0] bits. This is a read-only field. Writes specifically to this field have no effects. **[15: (TABITS+2)] Reserved** **[(TABITS+1):0] (R/W) Host transmit RAM read address (hsttramradx[(TABITS+1):0]): Default {(TABITS + 2) { 1'b0 }}** Host transmit RAM read address. If hsttramradx[TABITS+1] is written low, hsttramradx[(TABITS-1):0] is the transmit FIFO RAM address which hsttramrdat is read from. If hsttramradx[TABITS+1] is written high, hsttramradx[TABITS:0] contains the pointer value read from system transmit module.
0x06C	MAC-FIFO FIFO RAM Access* Register 3 **[31:0] (RO) Host transmit RAM read data (hsttramrdat[31:0]): Default 0x00** Host transmit RAM read data. This is the lower 4 bytes of transmit FIFO RAM data that is read at the address of hsttramradx[(TABITS-1):0] if hsttramradx[(TABITS+1)] is negated and hsttramrreq is asserted.This is a read-only field. Writes specifically to this field have no effects.

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Address[9:0]	Function
0x070	MAC-FIFO FIFO RAM Access* Register 4 **[31] (R/W) Host receive RAM write request (hstrramwreq): Default 0x0** Host receive RAM write request. Requests the handshake of hstrramwdat and hstrramwadx values to the receive FIFO RAM. Only be asserted while hstrramwack is negated and while the receive data path is disabled from receiving data in a steady state. **[30] (RO) Host receive RAM write acknowledge (hstrramwack): Default 0x0** Host receive RAM write acknowledge. Signifies the acceptance of hstrramwdat and hstrramwadx values to the receive FIFO RAM or System receive module. Will only be asserted or negated following assertion or negation of hstrramwreq. This is a read-only bit. Writes specifically to this bit no effects. **[29:24] Reserved** **[23:16] (R/W) Host receive RAM write data (hstrramwdat[39:32]): Default 0x0** Host receive RAM write data. This is the upper byte of receive FIFO RAM data that is written at the address of hstrramwadx[RABITS:0] if hstrramwadx[RABITS+2] is negated and hstrramwreq is asserted. This part of the receive FIFO RAM contains control information for the frame as follows: • hstrramwdat [39:36] = unused • hstrramwdat [35] = System receive start of frame. • hstrramwdat [34] = System receive end of frame. • hstrramwdat [33:32] = data valid Byte enable and applicable only for the last word of the frame. • 0: Indicates all bytes in the word are valid. • 1: Indicates the LSB 3 bytes are valid [23:0] bits. • 2: Indicates the LSB 2 bytes are valid [15:0] bits. • 3: Indicates the LSB 1 bytes are valid [7:0] bits. **[15:14] Reserved** **[(RABITS+2):0] (R/W) Host receive RAM write address (hsttramwadx[(RABITS+2):0]): Default {(RABITS+2) {1'b0}}** Host receive RAM write address. This field has different functionality based on the value of hstrramwadx[RABITS+1] and whether it is being written to or read from. When read from, hstrramwadx[12:0] field contains the actual write pointer value of the System receieve module. When written to the hstrramwadx register is loaded. If hstrramwadx[RABITS+1] is low, hstrramwadx[11:0] receives FIFO RAM address which hstrramwdat is written to. If hstrramwadx[RABITS+2] is high, hstrramwadx[RABITS+1:0] contains the pointer value that is written to System receieve module.
0x074	MAC-FIFO FIFO RAM Access* Register 5 **[31:0] (R/W) Host receive RAM write data (hstrramwdat [31:0]): Default 0x00** Host receive RAM write data. This is the lower 4 bytes of receive FIFO RAM data that writes at the address of hstrramwadx[RABITS:0] if hsttramwadx[RABITS+2] is negated and hstrramwreq is asserted.

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Address[9:0]	**Function**
0x078	MAC-FIFO FIFO RAM Access* Register 6 **[31] (R/W) Host receive RAM read request (hstrramrreq): Default 0x0** Host receive RAM read request. Requests the handshake of hstrramradx values to the receive FIFO RAM and hstrramrdat from the receive FIFO RAM. Should only be asserted while hstrramrack is negated and while the receive data path isdisabled from receiving data and is in a steady state. It should only be negated after receiving an asserted hstrramrack. **[30] (RO) Host receive RAM read acknowledge (hstrramrack): Default 0x0** Host receive RAM read acknowledge. Signifies the acceptance of hstrramradx values to the receive FIFO RAM and reception of hstrramrdat from the receive FIFO RAM location addressed. Will only be asserted or negated following assertion or negation of hstrramrreq. This is a read-only bit. Writes specifically to this bit have no effects. **[29:24] Reserved**[23:16] (RO) Host receive RAM read data (hstrramrdat[39:32]): Default 0x0 Host receive RAM read data. This is the upper byte of receive FIFO RAM data that was read at the address of hstrramwadx[RABITS:0] if hstrramwadx[RABITS+2] is negated and hstrramwreq is asserted. This part of the receive FIFO RAM contains control information for the frame as follows: • hstrramwdat [39:36] = unused. • hstrramwdat [35] = System receive start of frame. • hstrramwdat [34] = System receive end of frame. • hstrramwdat [33:32] = Data valid byte enable and applicable only for the last word of the frame. • 0: Indicates all bytes in the word are valid. • 1: Indicates the LSB 3 bytes are valid [23:0] bits. • 2: Indicates the LSB 2 bytes are valid [15:0] bits. • 3: Indicates the LSB 1 bytes are valid [7:0] bits. This is a read-only field. Writes specifically to this field have no effects. **[15:14] Reserved[13:0] (R/W) Host receive RAM read address (hstrramradx[31:0]): Default 0x00** Host receive RAM read address. If hstrramradx[RABITS+2] is written low, hstrramradx[11:0] is the receive FIFO RAM address which hstrramrdat is read from. If hstrramradx[RABITS+2] is written high, hstrramradx[12:0] contains the pointer value read from abric receive module.
0x07C	MAC-FIFO FIFO RAM Access* Register 7 **[31:0] (RO) Host receive RAM read data (hstrramrdat[31:0]): Default 0x00** Host receive RAM read data. This is the lower 4 bytes of receive FIFO RAM data that is read at the address of hstrramradx[RABITS:0] if hstrramradx[RABITS+2] is negated and hstrramrreq is asserted. This is a read-only field. Writes specifically to this field have no effects.

Note: Note: The FIFO RAM access registers are intended for non-real-time RAM testing and system debug. The MAC-FIFO I/O should be inactive before their use. The MAC_FIFO configuration registers one through five are intended to be written while the sub-modules are held in reset.

3.3 Statistics Counters Core Register

This section describes the Statistics Counters Core Register of the CoreTSE.

Table 3-4. Statistics Counters Core Register

Address[9:0]	Function
0x080	TR64 - Transmit and Receive 64 Byte Frame Counter: **Default 32'h0** **[31:18] (R/W) Reserved** **[17:0] (R/W) Transmit and Receive 64 Byte Frame Counter** Incremented for each good or bad frame transmitted and received which is 64 bytes in length inclusive (excluding framing bits but including FCS bytes).
0x084	TR127 - Transmit and Receive 65 to 127 Byte Frame Counter: **Default 32'h0** **[31:18] (R/W) Reserved** **[17:0] (R/W) Transmit and Receive 65 to 127 Byte Frame Counter** Incremented for each good or bad frame transmitted and received which is 65 to 127 bytes in length inclusive (excluding framing bits but including FCS bytes).
0x088	TR255 - Transmit and Receive 128 to 255 Byte Frame Counter: **Default 32'h0** **[31:18] (R/W) Reserved** **[17:0] (R/W) Transmit and Receive 128 to 255 Byte Frame Counter** Incremented for each good or bad frame transmitted and received which is 128 to 255 bytes in length inclusive (excluding framing bits but including FCS bytes).
0x08C	TR51 - Transmit and Receive 256 to 511 Byte Frame Counter: **Default 32'h0** **[31:18] (R/W) Reserved** **[17:0] (R/W) Transmit and Receive 256 to 511 Byte Frame Counter** Incremented for each good or bad frame transmitted and received which is 256 to 511 bytes in length inclusive (excluding framing bits but including FCS bytes).
0x090	TR1K - Transmit and Receive 512 to 1023 Byte Frame Counter: **Default 32'h0** **[31:18] (R/W) Reserved** **[17:0] (R/W) Transmit and Receive 512 to 1023 Byte Frame Counter** Incremented for each good or bad frame transmitted and received which is 512 to 1023 bytes in length inclusive (excluding framing bits but including FCS bytes).
0x094	TRMAX - Transmit and Receive 1024 to 1518 Byte Frame Counter: **Default 32'h0** **[31:18] (R/W) Reserved** **[17:0] (R/W) Transmit and Receive 1024 to 1518 Byte Frame Counter** Incremented for each good or bad frame transmitted and received which is 1024 to 1518 bytes in length inclusive (excluding framing bits but including FCS bytes).

.....continued	
Address[9:0]	**Function**
0x098	TRMGV - Transmit and Receive 1519 to 1522 Byte VLAN Frame Counter: **Default 32'h0** **[31:18] (R/W) Reserved** **[17:0] (R/W) Transmit and Receive 1519 to 1522 Byte VLAN Frame Counter** Incremented for each good VLAN frame transmitted and received which is 1519 to 1522 bytes in length inclusive (excluding framing bits but including FCS bytes).
0x09C	RBYT - Receive Byte Counter: **Default 32'h0** **[31:18] (R/W) Reserved** **[17:0] (R/W) Receive Byte Counter** The Statistic Counter register is incremented by the byte count of all frames received, including those in bad packets, excluding framing bits but including FCS bytes.
0x0A0	RPKT - Receive Packet Counter: **Default 32'h0** **[31:18] (R/W) Reserved** **[17:0] (R/W) Receive Packet Counter** Incremented for each frame received packet (including bad packets, all Unicast, Broadcast, and Multicast packets).
0x0A4	RFCS - Receive FCS Error Counter: **Default 32'h0** **[31:18] (R/W) Reserved** **[17:0] (R/W) Receive FCS Error Counter** Incremented for each frame received that has an integral 64 to 1518 length and contains a Frame Check Sequence error.
0x0A8	RMCA - Receive Multicast Packet Counter: **Default 32'h0** **[31:18] (R/W) Reserved** **[17:0] (R/W) Receive Multicast Packet Counter** Incremented for each Multicast good frame of lengths smaller than 1518 (non VLAN) or 1522 (VLAN) excluding Broadcast frames. This does not look at range/length errors.
0x0AC	RBCA - Receive Broadcast Packet Counter: **Default 32'h0** **[31:18] (R/W) Reserved** **[17:0] (R/W) Receive Broadcast Packet Counter** Incremented for each Broadcast good frame of lengths smaller than 1518 (non VLAN) or 1522 (VLAN) excluding Multicast frames. This does not look at range/length errors.

.....continued	
Address[9:0]	**Function**
0x0B0	RXCF - Receive Control Frame Packet Counter: **Default 32'h0** **[31:18] (R/W) Reserved** **[17:0] (R/W) Receive Control Frame Packet Counter** Incremented for each MAC Control frame received (PAUSE and Unsupported).
0x0B4	RXPF - Receive PAUSE Control Frame Counter: **Default 32'h0** **[31:12] (R/W) Reserved** **[11:0] (R/W) Receive PAUSE Frame Packet Counter** Incremented each time a valid PAUSE MAC Control frame is received.
0x0B8	RXUO - Receive Unknown OP code Packet Counter: **Default 32'h0** **[31:12] (R/W) Reserved** **[11:0] (R/W) Receive Unknown OP code Counter** Incremented each time a MAC Control Frame is received which contains an opcode other than a PAUSE.
0x0BC	RALN - Receive Alignment Error Counter: **Default 32'h0** **[31:12] (R/W) Reserved** **[11:0] (R/W) Receive Alignment Error Counter** Incremented for each received frame from 64 to 1518 which contains an invalid FCS and is not an integral number of bytes.
0x0C0	RFLR - Receive Frame Length Error Counter: **Default 32'h0** **[31:16] (R/W) Reserved** **[15:0] (R/W) Receive Frame Length Error Counter** Incremented for each frame received in which the 802.3 length field did not match the number of data bytes actually received (46-1500 bytes). The counter is not incremented if the length field is not a valid 802.3 length, such as an EtherType value.
0x0C4	RCDE - Receive Code Error Counter: **Default 32'h0** **[31:12] (R/W) Reserved** **[11:0] (R/W) Receive Code Error Counter** Incremented each time a valid carrier was present and at least one invalid data symbol was detected.

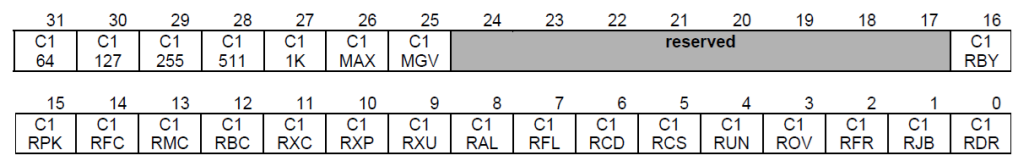
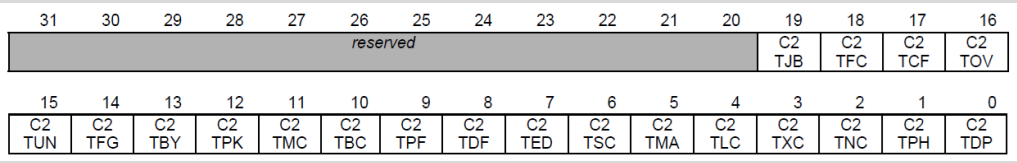
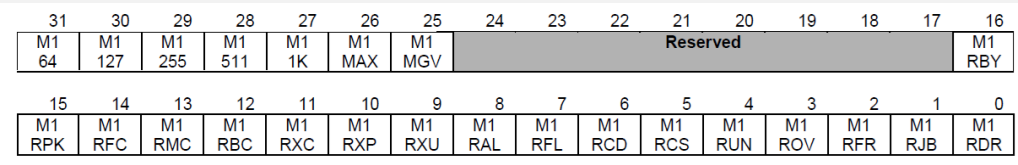
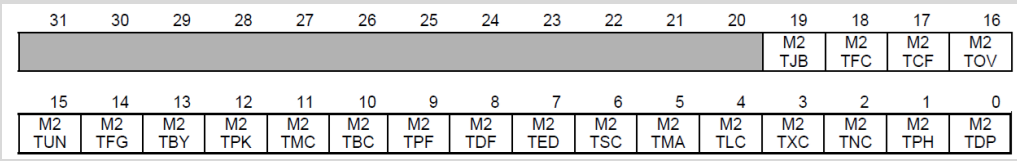
.....continued	
Address[9:0]	**Function**
0x0C8	RCSE - Receive Carrier Sense Error Counter: **Default 32'h0** **[31:12] (R/W) Reserved** **[11:0] (R/W) Receive False Carrier Counter** Incremented each time a false carrier is detected during idle, as defined by a 1 on RXER and an '0xE' on RXD. The event is reported along with the statistics generated on the next received frame. Only one false carrier condition can be detected and logged between frames.
0x0CC	RUND - Receive Undersize Packet Counter: **Default 32'h0** **[31:12] (R/W) Reserved** **[11:0] (R/W) Receive Undersize Packet Counter** Incremented each time a frame is received which is less than 64 bytes in length and contains a valid FCS and were otherwise well formed. This does not look at Range Length errors.
0x0D0	ROVR - Receive Oversize Packet Counter: **Default 32'h0** **[31:12] (R/W) Reserved** **[11:0] (R/W) Receive Oversize Packet Counter** Incremented each time a frame is received which exceeded 1518 (non VLAN) or 1522 (VLAN) and contains a valid FCS and were otherwise well formed. This does not look at Range Length errors.
0x0D4	RFRG - Receive Fragments Counter: **Default 32'h0** **[31:12] (R/W) Reserved** **[11:0] (R/W) Receive Fragments Counter** Incremented for each frame received which is less than 64 bytes in length and contains an invalid FCS, includes integral and non-integral lengths.
0x0D8	RJBR - Receive Jabber Counter: **Default 32'h0** **[31:12] (R/W) Reserved** **[11:0] (R/W) Receive Jabber Counter** Incremented for frames received which exceed 1518 (non VLAN) or 1522 (VLAN) bytes and contains an invalid FCS, includes alignment errors.
0x0DC	RDRP - Receive Drop: **Default 32'h0** **[31:12] (R/W) Reserved** **[11:0] (R/W) Receive Dropped packets Counter** Incremented for frames received which are streamed to system but are later dropped due to lack of system resources.

.....continued	
Address[9:0]	**Function**
0x0E0	TBYT - Transmit Byte Counter: **Default 32'h0** **[31:24] (R/W) Reserved** **[23:0] (R/W) Transmit Byte Counter** Incremented by the number of bytes that were put on the wire including fragments of frames that were involved with collisions. This count does not include preamble/SFD or jam bytes.
0x0E4	TPKT - Transmit Packet Counter: **Default 32'h0** **[31:18] (R/W) Reserved** **[17:0] (R/W) Transmit Packet Counter** Incremented for each transmitted packet (including bad packets, excessive deferred packets, excessive collision packets, late collision packets, all Unicast, Broadcast, and Multicast packets).
0x0E8	TMCA - Transmit Multicast Packet Counter: **Default 32'h0** **[31:18] (R/W) Reserved** **[17:0] (R/W) Transmit Multicast Packet Counter** Incremented for each Multicast valid frame transmitted (excluding Broadcast frames).
0x0EC	TBCA - Transmit Broadcast Packet Counter: **Default 32'h0** **[31:18] (R/W) Reserved** **[17:0] (R/W) Transmit Broadcast Packet Counter** Incremented for each Broadcast frame transmitted (excluding Multicast frames).
0x0F0	TXPF - Transmit PAUSE Control Frame Counter: **Default 32'h0** **[31:12] (R/W) Reserved** **[11:0] (R/W) Transmit PAUSE Frame Packet Counter** Incremented each time a valid PAUSE MAC Control frame is transmitted.
0x0F4	TDFR - Transmit Deferral Packet Counter: **Default 32'h0** **[31:12] (R/W) Reserved** **[11:0] (R/W) Transmit Deferral Packet Counter** Incremented for each frame, which was deferred on its first transmission attempt. Does not include frames involved in collisions.

.....continued	
Address[9:0]	**Function**
0x0F8	TEDF - Transmit Excessive Deferral Packet Counter: **Default 32'h0** **[31:12] (R/W) Reserved** **[11:0] (R/W) Transmit Excessive Deferral Packet Counter** Incremented for frames aborted which were deferred for an excessive period of time (3036 byte times).
0x0FC	TSCL - Transmit Single Collision Packet Counter: **Default 32'h0** **[31:12] (R/W) Reserved** **[11:0] (R/W) Transmit Single Collision Packet Counter** Incremented for each frame transmitted which experienced exactly one collision during transmission.
0x100	TMCL - Transmit Multiple Collision Packet Counter: **Default 32'h0** **[31:12] (R/W) Reserved** **[11:0] (R/W) Transmit Multiple Collision Packet Counter** Incremented for each frame transmitted which experienced 2-15 collisions (including any late collisions.
0x104	TLCL - Transmit Late Collision Packet Counter: **Default 32'h0** **[31:12] (R/W) Reserved** **[11:0] (R/W) Transmit Late Collision Packet Counter** Incremented for each frame transmitted which experienced a late collision during a transmission attempt.
0x108	TXCL - Transmit Excessive Collision Packet Counter: **Default 32'h0** **[31:12] (R/W) Reserved** **[11:0] (R/W) Transmit Excessive Collision Packet Counter** Incremented for each frame that experienced 16 collisions during transmission and was aborted.
0x10C	TNCL - Transmit Total Collision Counter: **Default 32'h0** **[31:13] (R/W) Reserved** **[12:0] (R/W) Transmit Total Collision Counter** Incremented by the number of collisions experienced during the transmission of a frame as defined as the simultaneous presence of signals on the DO and RD circuits (that is transmitting and receiving at the same time).
0x110	**Not Used**

.....continued	
Address[9:0]	**Function**
0x114	TDRP - Transmit Drop Frame Counter: **Default 32'h0** **[31:12] (R/W) Reserved** **[11:0] (R/W) Transmit Drop Frame Counter** Incremented each time input PFH is asserted.
0x118	TJBR - Transmit Jabber Frame Counter: **Default 32'h0** **[31:12] (R/W) Reserved** **[11:0] (R/W) Transmit Jabber Frame Counter** Incremented for each oversized transmitted frame with an incorrect FCS value.
0x11C	TFCS - Transmit FCS Error Counter: **Default 32'h0** **[31:12] (R/W) Reserved** **[11:0] (R/W) Transmit FCS Error Counter** Incremented for every valid sized packet with an incorrect FCS value.
0x120	TXCF - Transmit Control Frame Counter: **Default 32'h0** **[31:12] (R/W) Reserved** **[11:0] (R/W) Transmit Control Frame Counter** Incremented for every valid size frame with a Type Field signifying a Control frame.
0x124	TOVR - Transmit Oversize Frame Counter: **Default 32'h0** **[31:12] (R/W) Reserved** **[11:0] (R/W) Transmit Oversize Frame Counter** Incremented for each oversized transmitted frame with a correct FCS value.
0x128	TUND - Transmit Under size Frame Counter: **Default 32'h0** **[31:12] (R/W) Reserved** **[11:0] (R/W) Transmit Undersize Frame Counter** Incremented for every frame less than 64 bytes, with a correct FCS value.
0x12C	TFRG - Transmit Fragments Frame Counter: **Default 32'h0** **[31:12] (R/W) Reserved** **[11:0] (R/W) Transmit Fragment Counter** Incremented for every frame less than 64 bytes, with an incorrect FCS value.

.....continued

Address[9:0]	Function
0x130	**CAR1 - Carry Register One [R0]: Default 32'h0** 
0x134	**CAR2 - Carry Register Two Register: Default 32'h0** 
0x138	**CAM1 - Carry Register One Mask Register: Default 32'h fe01_ffff** 
0x13C	**CAM2 - Carry Register Two Mask Register: Default 32'h 000f_ffff** 

3.4 System Registers

This section describes the System registers of the CoreTSE.

Table 3-5. System Registers

Address[9:0]	Function
0x1C0	Frame filter controls. Default 32'h0000_003F • [5] (W/R) Pass the frame if the hash table entry matches for Multicast-DA • [4] (W/R) Pass the frame if the hash table entry matches for Unicast-DA • [3] (W/R) Promiscuous mode, allow all the frames to pass • [2] (W/R) Pass the frame if its Unicast-DA matches the configured-DA • [1] (W/R) Pass all multicast frames • [0] (W/R) Pass all broadcast frames
0x1C4	(R/W) Hash Table Register0: Hash Entries-[31:0] – Default 32'h0000_0000
0x1C8	(R/W) Hash Table Register1: Hash Entries-[63:32] - Default 32'h0000_0000
0x1CC	(R/W) Hash Table Register2: Hash Entries-[95:64] - Default32'h0000_0000
0x1D0	(R/W) Hash Table Register3: Hash Entries-[127:96] - Default 32'h0000_0000 Refer the Station Address Logic for Frame Filtering section of handbook for hash table utilization.

.....continued	
Address[9:0]	**Function**
0x1D4	(R/W) miscellaneous control register - Default 32'h0000_0000

3.5 SGMII/TBI/1000Base-X – Registers (Indirect Addressing through MDIO)

Configuration and status of the core is achieved by the Management Registers accessed through the serial MDIO. The TBI core is a dual mode core and to operate in TBI or 1000Base-X mode is user selectable.

The following registers are common in both modes:

- Control register at address 0x00
- STATUS Register at address 0x01
- Extended STATUS Register at address 0x0F
- Jitter Diagnostic register at address 0x10
- TBI Control register at address 0x11

Other registers (at address 0x04, 0x05, 0x06, 0x07, 0x08) are based on mode selected. In 0, these registers are described separately.

Table 3-6. MDIO Registers

Address	Function
0x00	**Control** **[15] (R/W, SC) PHY RESET: Default 0** Setting this bit causes the Tx, Rx, and AutoNegX sub-modules in the TBI core to be reset. This bit is self-clearing. **[14] (R/W) LOOP BACK: Default 0** Setting this bit causes the 10-bit transmit outputs of the TBI to be connected to the receive 10-bit inputs. Clearing this bit results in normal operation. This bit does not affect the clock signals, which for loopback must be handled external to the core. **[13] Reserved. Write as 0, ignore on read.** **[12] (R/W) AUTO-NEGOTIATION ENABLE Default 0** Setting this bit enables the Auto-negotiation process. If cleared, then the values programmed determines the operating condition of the link. **[11:10] Reserved. Write as 0, ignore on read.** **[9] (R/W, SC) RESTART AUTO-NEGOTIATION: Default 0** Setting this bit causes the Auto-negotiation process to restart. This action is only available when Auto-Negotiation has been enabled. **[8:0] Reserved. Write as 0, ignore on read.**

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Address	Function
0x01	**Status** **[15:9] Reserved. Write as 0, ignore on read.** **[8] (RO) EXTENDED STATUS: Default 1** This bit indicates that PHY status information is also contained in Register 0x0F – EXTENDED STATUS. **[7] Reserved. Write as 0, ignore on read.** **[6] (RO) MF PREMABLE SUPPRESSION ENABLE: Default 1** This bit indicates whether the PHY is capable of handling MDIO management Frames without the 32-bit preamble field. Returns 1 indicating support for suppressed preamble MDIO management Frames. **[5] (RO) AUTO-NEGOTIATION COMPLETE:** When 1, this bit indicates that the Auto-negotiation process has completed. This bit returns “0” when either the Auto-negotiation process is underway or when the Auto-negotiation function is disabled. **[4] (RO) REMOTE FAULT: Default 0** When 1, a remote Fault condition has been detected between the TBI and the PHY. **[3] (RO) AUTO-NEGOTIATION ABILITY: Default 1** When 1, this bit indicates that the TBI has the ability to perform Auto-negotiation. **[2] (RO) LINK STATUS: Default 0** When 1, this bit indicates that a valid link has been established between the TBI and the PHY. When 0, no valid link has been established. **[1] Reserved. Write as 0, ignore on read.** **[0] (RO) EXTENDED CAPABILITY: Default 1** This bit indicates that the TBI contains the extended set of registers.
0x02	**Reserved**
0x03	**Reserved**

.....continued

Address	Function
0x04	**AN Advertisement (1000BASE-T)** **[15] (R/W) LINK UP:** This bit must be written 0 for TBI operation. **[14] (RO) ACK (Reserved). Ignore on read.** **[13] (R/W) Reserved** This bit must be written 0 for TBI operation. **[12] (R/W) FULL-DUPLEX:** This bit must be written 0 for TBI operation. **[11:10] (R/W) LINK SPEED:** These bits must be written 00 for TBI operation. **[9:0] (R/W):** These bits must always be written 0000000001 for TBI operation.
	AN Advertisement (1000BASE-X) **[15] (R/W) NEXT PAGE: Default 0** The local device asserts this bit to either request Next Page transmission or advertise Next Page exchange capability. This bit can thus be set when the local has no Next Pages but wishes to allow reception of Next Pages. If the local device has no Next Pages, and the Link Partner wishes to send Next Pages, the local device should send Null Message Codes and have the MESSAGE PAGE set to 0b000_0000_0001. This bit should be cleared where the local device wishes not to engage in Next Page exchange. **[14] Reserved. Write as 0, ignore on read.** **[13:12] (R/W) REMOTE FAULT: Default 0x0** Encodes the local device's remote Fault condition. A Fault may be indicated by setting a nonzero Remote Fault encoding and re-negotiating. For more information, refer to Table 3-7. **[11:9] Reserved** **[7:8] (R/W) PAUSE: Encodes the local device's PAUSE capability.** **Pause Encoding:**For more information, refer to Table 3-8. **[6] (R/W) HALF-DUPLEX:** Setting this bit means local device is capable of half-duplex operation. **[5] (R/W) FULL-DUPLEX:** Setting this bit means local device is capable of full-duplex operation. **[4:0] Reserved**

.....continued

Address	Function
0x5	**AN Link Partner Base Page Ability (1000BASE-T)** **[15] (RO) LINK UP:** Assertion of this bit indicates that the link is up. **[14] (RO) Auto-Negotiation ACK as specified in 802.3z** **[13] Reserved** **[12] (RO) FULL-DUPLEX:** Assertion of this bit indicates that the link is transferring data in Full-Duplex mode. **[11:10] (RO) LINK SPEED:** Assertion of these 2 bits indicates the speed that the link is transferring data. • 2'b00: 10Mbps • 2'b01: 100Mbps • 2'b10: 1000Mbps • 2'b11: Reserve **[9:0] (R/W): These bits must always be written 0000000001 for TBI operation.**
	AN Link Partner Base Page Ability (1000BASE-X) **[15] (RO) NEXT PAGE:** The Link Partner asserts this bit either to request Next Page transmission or to indicate the capability to receive Next Pages. When 0, the Link Partner has no subsequent Next Pages or is not capable of receiving Next Pages. **[14] (RO) ACK (Reserved): Ignore on read** **[13:12] (RO) REMOTE FAULT:** For more information, refer to Table 3-7. Encodes the Link Partner's remote Fault condition. **[11:9] Reserved** **[8:7] (RO) PAUSE:** Encodes of the Link Partner's PAUSE capability. **Pause Encoding:**For more information, refer to Table 3-10. **[6] (RO) HALF-DUPLEX:** When 1, Link Partner is capable of half-duplex operation. When 0, Link Partner is incapable of half-duplex mode. **[5] (RO) FULL-DUPLEX:** When 1, Link Partner is capable of full-duplex operation. When 0, Link. Partner is incapable of full-duplex mode. **[4:0] Reserved**

.....continued	
Address	**Function**
0x06	**AN Expansion (1000BASE-T)** **[15:3] Reserved** **[2] (RO) NEXT PAGE ABLE: Default 1** When 1, indicates that the local device supports the Next Page function. **[1] (RO) PAGE RECEIVED:** When 1, indicates that a new page has been received and stored in the applicable AN LINK PARTNER ABILITY or AN NEXT PAGE. **[0] Reserved**
	AN Expansion (1000BASE-X) **[15:3] Reserved** **[2] (RO) NEXT PAGE ABLE:** 1 indicates local device supports Next Page function. Returns 1 on read. **[1] (RO,LH) PAGE RECEIVED:** 1 indicates that a new page has been received and stored in the applicable AN LINK PARTNER ABILITY or AN NEXT PAGE register. This bit latches high in order for software to detect when polling. The bit is cleared on a read to the register. **[0] Reserved**
0x07	**AN Next Page Transmit (1000BASE-T)** Use of this register is user dependent. User can define functionality of bits of this register as per system requirement. **[15:0] User defined Register**
	AN Next Page Transmit (1000BASE-X) **[15] (R/W) NEXT PAGE:** Assert this bit to indicate additional Next Pages to follow. Bit is cleared to indicate last page. **[14] (RO) ACK (Reserved): Write 0, ignore on read.** **[13] (R/W) MESSAGE PAGE:** Assert bit to indicate Message Page. Clear bit to indicate unformatted page. **[12] (R/W) ACKNOWLEDGE 2:** Used by Next Page function to indicate device has ability to comply with the message. Assert bit if local device complies with message. Clear bit if local device cannot comply with message. **[11] (RO) TOGGLE:** Used to ensure synchronization with the Link Partner during Next Page exchange. This bit always takes opposite value of the Toggle bit of the previously exchanged Link Code Word. The initial value in the first Next Page transmitted is the inverse of bit 11 in the base Link Code Word. **[10:0] (R/W) MESSAGE/UNFORMATTED CODE FIELD:** Message pages are formatted pages that carry a predefined Message Code, which is enumerated in IEEE 802.3u/Annex 28C. Unformatted Code Fields take on an arbitrary value.

.....continued	
Address	**Function**
0x08	**AN Link Partner Ability Next Page (1000BASE-T)** Use of this register is user dependent. User can define functionality of bits of this register as per system requirement. **[15:0] User defined Register**
	AN Link Partner Ability Next Page (1000BASE-X) **[15] (RO) NEXT PAGE:** The Link Partner asserts this bit to indicate additional Next Pages to follow. When 0, indicates last Next Page from link partner. **[14] (RO) ACK (Reserved): Ignore on read.** **[13] (RO) MESSAGE PAGE:** When 1, indicates Message Page. When 0, indicates Unformatted Page. **[12] (RO) ACKNOWLEDGE 2:** Indicates Link Partner's ability to comply with the message. When 1, Link Partner complies with message. When 0, Link Partner cannot comply with message. **[11] (RO) TOGGLE:** Used to ensure synchronization with the Link Partner during Next Page exchange. This bit always takes opposite value of the Toggle bit of the previously exchanged Link Code Word. The initial value in the first Next Page transmitted is the inverse of bit 11 in the base Link Code Word. **[10:0] (RO) MESSAGE/UNFORMATTED CODE FIELD:** Message pages are formatted pages that carry a predefined Message Code, which is enumerated in IEEE 802.3u/Annex 28C. Unformatted Code Fields take on an arbitrary value.
0x0F	**Extended Status** **[15] (RO) 1000BASE-X FULL-DUPLEX: Default 1** When 1, indicates PHY can operate in 1000BASE-X Full-Duplex mode. When 0, indicates PHY cannot operate in this mode. **[14] (RO) 1000BASE-X HALF-DUPLEX: Default 0** When 1, indicates PHY can operate in 1000BASE-X Half-Duplex mode. When 0, indicates PHY cannot operate in this mode. **[13] (RO) 1000BASE-T FULL-DUPLEX: Default 1** When 1, indicates PHY can operate in 1000BASE-T Full-Duplex mode. When 0, indicates PHY cannot operate in this mode. **[12] (RO) 1000BASE-T HALF-DUPLEX: Default 0** When 1, indicates PHY can operate in 1000BASE-T Half-Duplex mode. When 0, indicates PHY cannot operate in this mode. **[11:0] Reserved**

.....continued	
Address	**Function**
0x10	**Jitter Diagnostics** **[15] (R/W) JITTER DIAGNOSTIC ENABLE: Default 0** Set this bit to enable the TBI to transmit the jitter test patterns defined in IEEE 802.3z 36A. Clear this bit to enable normal transmit-operation. **[14:12] (R/W) JITTER PATTERN SELECT: Default 0x0** For more information refer to Table 3-9. Selects the jitter pattern to be transmitted in diagnostics mode. **[11:10] Reserved** **[9:0] (R/W) CUSTOM JITTER PATTERN: Default 0x0** Used in conjunction with JITTER PATTERN SELECT and JITTER DIAGNOSTIC ENABLE. Set this field to the desired custom pattern, which transmits continuously.
0x11	**SGMII/Ten Bit Interface Control** **[15] (R/W) SOFT RESET: Default 0** This bit resets the functional modules in the TBI. Clear it for normal operation. **[14] (R/W) SHORTCUT LINK TIMER: Default 0** Set this bit 1 to reduce the value of Go Link Timer and Sync. Status Fail Timer to 64 clock pulse. Ultimately this reduces the amount of simulation time needed to time the 1.6ms Link Timer. Clear it for normal operation. In normal operation the value of Go Link Timer is 200000 clock pulses and the value of the Sync. Status Fail Timer is 1250000 clock pulses. **[13] (R/W) DISABLE RECEIVE RUNNING DISPARITY: Default 0** Set this bit to disable the running disparity calculation and checking in the receive direction. This bit must be 0 for TBI operation. **[12] (R/W) DISABLE TRANSMIT RUNNING DISPARITY: Default 0** Set this bit to disable the running disparity calculation and checking in the transmit direction. This bit must be 0 for TBI operation. **[11] (R/W) GO LINK TIMER VALUE CONTROL: Default 0** When 0 the Go Link Timer Value=1.6 ms When set to 1 the Go Link Timer Value=10 ms **[10:9] Reserved** **[8] (R/W) AUTO-NEGOTIATION SENSE: Default 0** Set this bit to allow the Auto-Negotiation function to sense either a MAC in Auto-Negotiation bypass mode or an older MAC without Auto-Negotiation capability. When sensed, Auto-Negotiation Complete becomes true; however Page Received is low, indicating no page was exchanged. Management can then act accordingly. Clear this bit when IEEE 802.3z Clause 37 behaviour is desired, which results in the link not coming up. **[7:0] Reserved**

Table 3-7. Remote Fault

RF1 (4, 12)	RF2 (4, 13)	Description
0	0	No error, link Ok.
0	1	Offline.
1	0	Link_Failure.

.....continued		
RF1 (4, 12)	**RF2 (4, 13)**	**Description**
1	1	Auto-Negotiation_Error.

Table 3-8. Pause Encodig

PAUSE1 (4.7)	ASM_DIR (4.8)	Capability
0	0	No PAUSE.
0	1	Asymmetric PAUSE toward link partner.
1	0	Symmetric PAUSE.
1	1	Asymmetric PAUSE toward local device.

Table 3-9. Jitter Pattern Select

Jitter Pattern Select	Bit 14	Bit 13	Bit 12
User Defined Custom Pattern	0	0	0
Annex 36A Defined High Frequency 10101010101010101010…	0	0	1
Annex 36A Defined Mixed Frequency 11111010110000010100…	0	1	0
Custom Defined Low Frequency 11111000001111100000…	0	1	1
Random Jitter Pattern	1	0	0
Annex 36A Defined Low Frequency 11111000001111100000…	1	0	1
Reserved	1	1	0
Reserved	1	1	1

Table 3-10. Pause Encodig

PAUSE1 (4.7)	ASM_DIR (4.8)	Capability
0	0	No PAUSE.
0	1	Asymmetric PAUSE toward link partner.
1	0	Symmetric PAUSE.
1	1	Both Symmetric PAUSE and Asymmetric PAUSE toward local device.

4. Interface

This section describes the interface of the CoreTSE.

4.1 Ports

The port signals for CoreTSE are described in the following table.

Table 4-1. I/O Signal Description

Port Name	Width	Direction	Description
Clock and Reset			
STBP	1	Input	Set Reset Bypass, used only in test-mode, where all the internal sync-resets are bypassed prior to SCAN testing. For the CoreTSE normal operation STBP must be set to '0'.
TXCLK	1	Input	2.5/25/125 MHz transmit clock generated from transmit clock of Transceiver according to 10/100/1000 Mbps support.
RXCLK	1	Input	2.5/25/125 MHz receive clock generated from receive clock of according to 10/100/1000 Mbps support.
SGMII/TBI PHY interface signals			
TBI_TX_CLK	1	Input	125 MHz TBI from transmit clock of Transceiver.
TBI_RX_CLK	1	Input	125 MHz TBI from receive clock of Transceiver.
RCG	10	Input	Receive code group.
TCG	10	Output	Transmit code group.
ANX_STATE	10	Output	Auto negotiation status information • 0th bit-DISABLE_LINK_OK state. • First bit-AN_ENABLE state. • Second bit-AN_RESTART state. • Third bit-ABILITY_DETECT state. • Fourth bit-ACKNOWLEDGE_DETECT state. • Fifth bit-NEXT_PAGE_WAIT state. • Sixth bit-COMPLETE_ACKNOWLEDGE state. • Seventh bit-IDLE_DETECT state. • Eighth bit-LINK_OK state. • Ninth bit-Received configuration frame data.
SYNC	1	Output	Receive link sync status.
SIGNAL_DETECT	1	Input	The SIGNAL_DETECT is typically provided from the optical module to indicate when an optical signal is valid otherwise that should be driven HIGH.

.....continued

Port Name	Width	Direction	Description
TBI_RX_READY	1	Input	RCG valid, recommended to connect with Transceiver receive Ready. For PolarFire® and PolarFire SoC this signal is available only when parameter SLIP_ENABLE is 1.
TBI_TX_VALID	1	Output	TCG valid, recommended to connect with Transceiver transmit valid.
TBI_RX_VALID	1	Input	Available only in PolarFire and PolarFire SoC when SLIP_ENABLE is 1, recommended to connect with Transceiver receive valid.
RX_SLIP	1	Output	Available only in PolarFire and PolarFire SoC when SLIP_ENABLE is 1, recommended to connect with receive slip signal of Transceiver.
G/MII PHY interface signals			
GTXCLK	1	Input	125 MHz clock from G/MII PHY.
TXD	8	Output	Transmit data • TXD[3:0] used for MII 100/10 Mbps (Nibble Mode). • TXD[7:0] used for GMII 1000 Mbps (Byte mode).
TXEN	1	Output	Transmit enable.
TXER	1	Output	Transmit error.
RXD	8	Input	Receive data • RXD[3:0] used for MII 100/10 Mbps (Nibble mode). • RXD[7:0] used for GMII 1000 Mbps (Byte mode).
RXDV	1	Input	Receive data valid.
RXER	1	Input	Receive error.
CRS	1	Input	G/MII carrier sense flag.
COL	1	Input	G/MII collision detect flag.
Management interface MDIO signals			
MDI	1	Input	MDIO management data input from pad.
MDC	1	Output	MDIO management data clock.
MDO	1	Output	MDIO management data output.
MDOEN	1	Output	MDIO management data output enable.
MAC Data Path Transmit Interface Signals			
MTXCLK	1	Input	MAC Transmit Clock
MTXRDY	1	Input	MAC Transmit Ready
MTXACPT	1	Output	MAC Transmit Accept
MTXSOF	1	Input	MAC Transmit Start of Frame

.....continued

Port Name	Width	Direction	Description
MTXEOF	1	Input	MAC Transmit End of Frame
MTXDAT	32	Input	MAC Transmit Frame Data
MTXBYTEVALID	2	Input	MAC Transmit data bytes valid indicator, applicable only for the last word of the frame • 0: Indicates all bytes in the word are valid. • 1: Indicates the LSB 3 bytes are valid (23:0 bits). • 2: Indicates the LSB 2 bytes are valid (15:0 bits). • 3: Indicates the LSB 1 bytes are valid (7:0 bits).
MTXCFRM	1	Input	MAC Transmit Pause Control Frame. Asserted for transfer of a pause control frame. Valid whenever MTXRDY asserted. Transferred whenever MTXRDY and MTXACPT and the rising edge of MTXCLK occur. Should remain constant for duration of frame.
MTXHWM	1	Output	MAC Transmit High Watermark Asserted whenever the amount of word locations used in the MAC. Transmit Data RAM exceeds configured FIFO register value.
MAC Data path Receive Interface			
MRXCLK	1	Input	MAC Receive Clock
MRXRDY	1	Output	MAC Receive Ready
MRXACPT	1	Input	MAC Receive Accept
MRXSOF	1	Output	MAC Receive Start of Frame
MRXEOF	1	Output	MAC Receive End of Frame
MRXDAT	32	Output	MAC Receive Frame Data
MRXBYTEVALID	2	Output	MAC Receive data bytes valid indicator, applicable only for the last word of the frame • 0: Indicates all bytes in the word are valid. • 1: Indicates the LSB 3 bytes are valid (23:0 bits). • 2: Indicates the LSB 2 bytes are valid (15:0 bits). • 3: Indicates the LSB 1 bytes are valid (7:0 bits).
APB Interface			
PCLK	1	Input	APB System Clock: reference clock for all internal logic
PRESETN	1	Input	APB active-low asynchronous reset
PADDR	32	Input	APB address bus
PSEL	1	Input	APB target select

.....continued			
Port Name	**Width**	**Direction**	**Description**
PENABLE	1	Input	APB enable
PWRITE	1	Input	• 1: APB Write • 0: APB Read
PWDATA	32	Input	APB write data
PRDATA	32	Output	APB read data
PSLVERR	1	Output	APB error signal to indicate the failure of transfer.
PREADY	1	Output	APB ready signal
Miscellaneous Signals			
TSM_INTR	2	Output	Interrupt signals. Providing these individual interrupt at top allows user to connect required interrupts to host-processor based on application requirement. • [1] Wake on LAN detected interrupt • [0] Statistics counter carry interrupt
TSM_CONTROL	32	Output	32-bit GPIO output signals mapped to system miscellaneous control register (0x1D4).
RCG_ERROR	1	Output	Indicates the receive code group error.

4.2 Configuration Parameters

The register transfer level (RTL) code for CoreTSE has parameters for configuring the core. While working with the core in the SmartDesign tool, a configuration GUI is used to set the values of these parameters. CoreTSE parameters are described in the following table.

Table 4-2. CoreTSE Configuration Parameters

Name	Valid Range	Default	Description
GMII_TBI	0 or 1	0	• 0: G/MII is active • 1: SGMII/TBI is active
PACKET_SIZE	256 Bytes to 32 KB	8KB	PACKET_SIZE parameter in the design is transmit FIFO address width and supported PACKET_SIZE choices are: • 256 Bytes • 512 Bytes • 1 KB • 2 KB • 4 KB • 8 KB • 16 KB • 32 KB
SAL	0 or 1	1	Include Station Address filtering logic (SAL): • 0: Disable • 1: Enable

.....continued			
Name	**Valid Range**	**Default**	**Description**
WoL	0 or 1	1	Include Wake on LAN (WoL) detection logic [1]: • 0: Disable • 1: Enable
STATS	0 or 1	1	Include Statistics counters logic: • 0: Disable • 1: Enable
MDIO_PHYID	0 to 31	18	MDIO Physical Address, it is an integer value [2]
SLIP_ENABLE	0 or 1	0	Include receive slip logic [3] [4]: • 0: Disable • 1: Enable

Notes:

1. Supports Wake on LAN using AMD's Magic Packet™ Detection technology.
2. This parameter is available for configuration only when GMII_TBI parameter is set to 1 (TBI mode).
3. This parameter is available for configuration only in PolarFire and PolarFire SoC device families and when GMII_TBI parameter is set to 1 (TBI mode).
4. This parameter should be enabled only if CDR Bit-Slip port is enabled in Transceiver.

5. Tool Flow

This section describes the tool flow of the CoreTSE.

5.1 License

CoreTSE is available in two versions:

- **Evaluation**: Evaluation version is available for free and supports user tesbench simulations and four hours of the functionality on silicon.
- **Obfuscated**: Obfuscated version is license locked and supports user tesbench simulations and unlimited functionality on silicon.

5.2 RTL

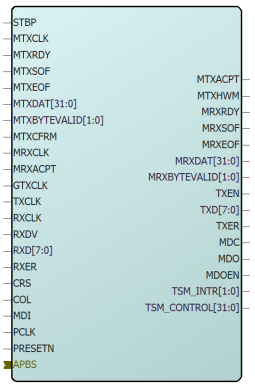
Complete encrypted RTL source code is provided for the core.

5.3 SmartDesign

CoreTSE is available through the Libero SoC IP catalog. Download it from a remote web-based repository and install into your local vault to make it ready to use. Once installed in the Libero software, the core can be instantiated, configured, connected, and generated using the SmartDesign tool.

An example instantiated view is shown in the following figure.

Figure 5-1. SmartDesign CoreTSE Instance View

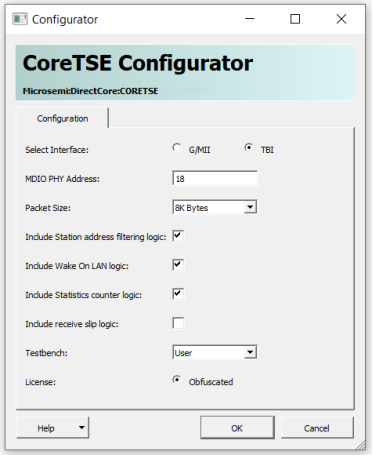


For more information on using SmartDesign to instantiate and generate cores, refer to the Libero SoC v12.0 and later or consult the Libero SoC v11.9 and earlier.

5.4 Configuring CoreTSE in SmartDesign

The core can be configured using the configuration GUI within SmartDesign. An example of the GUI is as shown in following figure.

Figure 5-2. Configuring CoreTSE in SmartDesign



5.5 Simulation Flows

To run user testbench simulations, select the User testbench flow in the core configurator GUI. When the core is generated Libero installs the user testbench files. After the files are generated; set the design root to the CoreTSE top level module in the **Libero Design Hierarchy** pane, then set the CoreTSE testbench top level module as active stimulus in the **Libero Stimulus Hierarchy** pane and click **Simulation** option in the **Libero Design Flow** pane. This invokes ModelSim® and automatically runs the simulation.

5.6 Synthesis in Libero SoC

To run synthesis, set the design root to the SmartDesign IP component instance and click the **Synthesize** option in the **Libero Design Flow** pane. This invokes Synplify Pro and automatically runs the synthesis.

5.7 Place-and-Route in Libero SoC

After design is synthesized, click **Place and Route** option in the **Libero Design Flow** pane to run place and route. No special place and route settings are required.

6. Clocks and Reset

This section describes the clocks and reset of the CoreTSE.

6.1 Clocks

Following clocks are used in the IP core.

- **PCLK** – Clock input for APB interface.
- **MTXCLK** – Clock input for MAC data path transmit interface.
- **MRXCLK** – Clock input for MAC data path receive interface.
- **TBI_TX_CLK** – 125 MHz clock input for TBI transmit interface. This clock is connected to the Transmit clock from the Transceiver. This clock is available only in TBI mode.
- **TXCLK** – 125/25/2.5 MHz clock input for G/MII interface/MAC operations in 1000/100/10 Mbps data-rate respectively. In TBI mode, this clock is generated from TBI_TX_CLK. In G/MII mode, this clock is connected to the Transmit clock from the G/MII PHY.
- **TBI_RX_CLK** – 125 MHz clock input for TBI receive interface. This clock is connected to the Receive clock from the Transceiver. This clock is available only in TBI mode.
- **RXCLK** – 125/25/2.5 MHz clock input for G/MII interface/MAC operations in 1000/100/10 Mbps data-rate respectively. In TBI mode, this clock is generated from TBI_RX_CLK. In G/MII mode, this clock is connected to the Receive clock from the G/MII PHY.
- **MDC** – Management clock output for MDIO interface. This clock is generated by the IP core. PCLK is the source clock. The MGMT CLOCK SELECT field of MDIO Mgmt: Configuration register (address 0x020) determines the frequency of this clock.

6.2 Reset

Following reset is used in the IP core.

PRESETN

Active-Low reset input. This reset is asserted asynchronously, but de-asserted synchronous to PCLK.

For all clock domains except PCLK clock domain, PRESETN reset input is synchronized to the respective clock domain and used within that clock domain.

In SmartFusion2, IGLOO2, PolarFire, and PolarFire SoC device families, reset is used as asynchronous reset. In RTG4 device family, reset is used as synchronous reset.

In RTG4 device family, all the clock inputs shall be available and stable before reset assertion. And the reset shall be asserted for atleast three clock cycles of the slowest clock used in this IP.

7. Design Constraints

This section describes the design constraints of the CoreTSE.

7.1 Timing Constraints

This section provides the information on the timing constraints required for this IP core.

It is recommended to you to use false path constraints for the reset synchronizers used in the core. Reset synchronizers are used in the core to synchronize the PRESETN reset input to all the clock domains except PCLK clock domain.

- Constraints required for RTG4 device family:
  Following constraints are required in both TBI and GMII modes (RTG4).

```
set_false_path -to [ get_pins { CORETSE_C0_0/CORETSE_C0_0/CoreTSE_TOP_INST/CLKRST_U/
SYNC_RESET.hstrst_ft_* } ]
set_false_path -to [ get_pins { CORETSE_C0_0/CORETSE_C0_0/CoreTSE_TOP_INST/CLKRST_U/
SYNC_RESET.hstrst_fr_* } ]
set_false_path -to [ get_pins { CORETSE_C0_0/CORETSE_C0_0/CoreTSE_TOP_INST/CLKRST_U/
SYNC_RESET.hstrst_tx_* } ]
set_false_path -to [ get_pins { CORETSE_C0_0/CORETSE_C0_0/CoreTSE_TOP_INST/CLKRST_U/
SYNC_RESET.hstrst_rx_* } ]
set_false_path -to [ get_pins { CORETSE_C0_0/CORETSE_C0_0/CoreTSE_TOP_INST/tsmac_top_U0/
amcxfif_U0/ACT_UNIQUE_AMCXFIF_CLKRST_1/ftrst_* } ]
set_false_path -to [ get_pins { CORETSE_C0_0/CORETSE_C0_0/CoreTSE_TOP_INST/tsmac_top_U0/
amcxfif_U0/ACT_UNIQUE_AMCXFIF_CLKRST_1/frrst_* } ]
set_false_path -to [ get_pins { CORETSE_C0_0/CORETSE_C0_0/CoreTSE_TOP_INST/tsmac_top_U0/
amcxfif_U0/ACT_UNIQUE_AMCXFIF_CLKRST_1/wtrst_* } ]
set_false_path -to [ get_pins { CORETSE_C0_0/CORETSE_C0_0/CoreTSE_TOP_INST/tsmac_top_U0/
amcxfif_U0/ACT_UNIQUE_AMCXFIF_CLKRST_1/strst_* } ]
set_false_path -to [ get_pins { CORETSE_C0_0/CORETSE_C0_0/CoreTSE_TOP_INST/tsmac_top_U0/
amcxfif_U0/ACT_UNIQUE_AMCXFIF_CLKRST_1/srrst_* } ]
set_false_path -to [ get_pins { CORETSE_C0_0/CORETSE_C0_0/CoreTSE_TOP_INST/tsmac_top_U0/
pe_mcxmac_U0/ACT_UNIQUE_PECAR_1/srtmc_* } ]
set_false_path -to [ get_pins { CORETSE_C0_0/CORETSE_C0_0/CoreTSE_TOP_INST/tsmac_top_U0/
pe_mcxmac_U0/ACT_UNIQUE_PECAR_1/srrmc_* } ]
set_false_path -to [ get_pins { CORETSE_C0_0/CORETSE_C0_0/CoreTSE_TOP_INST/tsmac_top_U0/
pe_mcxmac_U0/ACT_UNIQUE_PECAR_1/srtfn_* } ]
set_false_path -to [ get_pins { CORETSE_C0_0/CORETSE_C0_0/CoreTSE_TOP_INST/tsmac_top_U0/
pe_mcxmac_U0/ACT_UNIQUE_PECAR_1/srrfn_* } ]
Following constraints are required in TBI mode only (RTG4).
set_false_path -to [ get_pins { CORETSE_C0_0/CORETSE_C0_0/CoreTSE_TOP_INST/CLKRST_U/
SYNC_RESET.hstrst_tbi_tx_* } ]
set_false_path -to [ get_pins { CORETSE_C0_0/CORETSE_C0_0/CoreTSE_TOP_INST/CLKRST_U/
SYNC_RESET.hstrst_tbi_rx_* } ]
set_false_path -to [ get_pins { CORETSE_C0_0/CORETSE_C0_0/CoreTSE_TOP_INST/
SGMII_INSTANCE.msgmii_core_u0/ACT_UNIQUE_MSGMII_CLKRST_1/SYNC_RESET.tx_clkirst_* } ]
set_false_path -to [ get_pins { CORETSE_C0_0/CORETSE_C0_0/CoreTSE_TOP_INST/
SGMII_INSTANCE.msgmii_core_u0/ACT_UNIQUE_MSGMII_CLKRST_1/SYNC_RESET.rx_clkirst_* } ]
set_false_path -to [ get_pins { CORETSE_C0_0/CORETSE_C0_0/CoreTSE_TOP_INST/
SGMII_INSTANCE.msgmii_core_u0/ACT_UNIQUE_MSGMII_CLKRST_1/SYNC_RESET.gtx_clkirst_* } ]
set_false_path -to [ get_pins { CORETSE_C0_0/CORETSE_C0_0/CoreTSE_TOP_INST/
SGMII_INSTANCE.msgmii_core_u0/ACT_UNIQUE_MSGMII_CLKRST_1/SYNC_RESET.pma_rx_clkrst_* } ]
set_false_path -to [ get_pins { CORETSE_C0_0/CORETSE_C0_0/CoreTSE_TOP_INST/
SGMII_INSTANCE.msgmii_core_u0/ACT_UNIQUE_MSGMII_TBI_1/ACT_UNIQUE_PETCR_1/rtex_* } ]
set_false_path -to [ get_pins { CORETSE_C0_0/CORETSE_C0_0/CoreTSE_TOP_INST/
SGMII_INSTANCE.msgmii_core_u0/ACT_UNIQUE_MSGMII_TBI_1/ACT_UNIQUE_PETCR_1/rrex_* } ]
```

  Following constraints are required in TBI mode only (RTG4).

```
set_false_path -to [ get_pins { CORETSE_C0_0/CORETSE_C0_0/CoreTSE_TOP_INST/CLKRST_U/
SYNC_RESET.hstrst_tbi_tx_* } ]
set_false_path -to [ get_pins { CORETSE_C0_0/CORETSE_C0_0/CoreTSE_TOP_INST/CLKRST_U/
SYNC_RESET.hstrst_tbi_rx_* } ]
set_false_path -to [ get_pins { CORETSE_C0_0/CORETSE_C0_0/CoreTSE_TOP_INST/
SGMII_INSTANCE.msgmii_core_u0/ACT_UNIQUE_MSGMII_CLKRST_1/SYNC_RESET.tx_clkirst_* } ]
set_false_path -to [ get_pins { CORETSE_C0_0/CORETSE_C0_0/CoreTSE_TOP_INST/
SGMII_INSTANCE.msgmii_core_u0/ACT_UNIQUE_MSGMII_CLKRST_1/SYNC_RESET.rx_clkirst_* } ]
set_false_path -to [ get_pins { CORETSE_C0_0/CORETSE_C0_0/CoreTSE_TOP_INST/
```

```
SGMII_INSTANCE.msgmii_core_u0/ACT_UNIQUE_MSGMII_CLKRST_1/SYNC_RESET.gtx_clkirst_* } ]
set_false_path -to [ get_pins { CORETSE_C0_0/CORETSE_C0_0/CoreTSE_TOP_INST/
SGMII_INSTANCE.msgmii_core_u0/ACT_UNIQUE_MSGMII_CLKRST_1/SYNC_RESET.pma_rx_clkrst_* } ]
set_false_path -to [ get_pins { CORETSE_C0_0/CORETSE_C0_0/CoreTSE_TOP_INST/
SGMII_INSTANCE.msgmii_core_u0/ACT_UNIQUE_MSGMII_TBI_1/ACT_UNIQUE_PETCR_1/rtex_* } ]
set_false_path -to [ get_pins { CORETSE_C0_0/CORETSE_C0_0/CoreTSE_TOP_INST/
SGMII_INSTANCE.msgmii_core_u0/ACT_UNIQUE_MSGMII_TBI_1/ACT_UNIQUE_PETCR_1/rrex_* } ]
```

- Constraints required for all supported device families except RTG4:
  Following constraints are required in both TBI and GMII modes (non-RTG4).

```
set_false_path -to [ get_pins { CORETSE_C0_0/CORETSE_C0_0/CoreTSE_TOP_INST/CLKRST_U/
ASYNC_RESET.hstrst_ft_* } ]
set_false_path -to [ get_pins { CORETSE_C0_0/CORETSE_C0_0/CoreTSE_TOP_INST/CLKRST_U/
ASYNC_RESET.hstrst_fr_* } ]
set_false_path -to [ get_pins { CORETSE_C0_0/CORETSE_C0_0/CoreTSE_TOP_INST/CLKRST_U/
ASYNC_RESET.hstrst_tx_* } ]
set_false_path -to [ get_pins { CORETSE_C0_0/CORETSE_C0_0/CoreTSE_TOP_INST/CLKRST_U/
ASYNC_RESET.hstrst_rx_* } ]
set_false_path -to [ get_pins { CORETSE_C0_0/CORETSE_C0_0/CoreTSE_TOP_INST/tsmac_top_U0/
amcxfif_U0/ACT_UNIQUE_AMCXFIF_CLKRST_1/ftrst_* } ]
set_false_path -to [ get_pins { CORETSE_C0_0/CORETSE_C0_0/CoreTSE_TOP_INST/tsmac_top_U0/
amcxfif_U0/ACT_UNIQUE_AMCXFIF_CLKRST_1/frrst_* } ]
set_false_path -to [ get_pins { CORETSE_C0_0/CORETSE_C0_0/CoreTSE_TOP_INST/tsmac_top_U0/
amcxfif_U0/ACT_UNIQUE_AMCXFIF_CLKRST_1/wtrst_* } ]
set_false_path -to [ get_pins { CORETSE_C0_0/CORETSE_C0_0/CoreTSE_TOP_INST/tsmac_top_U0/
amcxfif_U0/ACT_UNIQUE_AMCXFIF_CLKRST_1/strst_* } ]
set_false_path -to [ get_pins { CORETSE_C0_0/CORETSE_C0_0/CoreTSE_TOP_INST/tsmac_top_U0/
amcxfif_U0/ACT_UNIQUE_AMCXFIF_CLKRST_1/srrst_* } ]
set_false_path -to [ get_pins { CORETSE_C0_0/CORETSE_C0_0/CoreTSE_TOP_INST/tsmac_top_U0/
pe_mcxmac_U0/ACT_UNIQUE_PECAR_1/srtmc_* } ]
set_false_path -to [ get_pins { CORETSE_C0_0/CORETSE_C0_0/CoreTSE_TOP_INST/tsmac_top_U0/
pe_mcxmac_U0/ACT_UNIQUE_PECAR_1/srrmc_* } ]
set_false_path -to [ get_pins { CORETSE_C0_0/CORETSE_C0_0/CoreTSE_TOP_INST/tsmac_top_U0/
pe_mcxmac_U0/ACT_UNIQUE_PECAR_1/srtfn_* } ]
set_false_path -to [ get_pins { CORETSE_C0_0/CORETSE_C0_0/CoreTSE_TOP_INST/tsmac_top_U0/
pe_mcxmac_U0/ACT_UNIQUE_PECAR_1/srrfn_* } ]
```

  Following constraints are required in TBI mode only (non-RTG4).

```
set_false_path -to [ get_pins { CORETSE_C0_0/CORETSE_C0_0/CoreTSE_TOP_INST/CLKRST_U/
ASYNC_RESET.hstrst_tbi_tx_* } ]
set_false_path -to [ get_pins { CORETSE_C0_0/CORETSE_C0_0/CoreTSE_TOP_INST/CLKRST_U/
ASYNC_RESET.hstrst_tbi_rx_* } ]
set_false_path -to [ get_pins { CORETSE_C0_0/CORETSE_C0_0/CoreTSE_TOP_INST/
SGMII_INSTANCE.msgmii_core_u0/ACT_UNIQUE_MSGMII_CLKRST_1/ASYNC_RESET.tx_clkirst_* } ]
set_false_path -to [ get_pins { CORETSE_C0_0/CORETSE_C0_0/CoreTSE_TOP_INST/
SGMII_INSTANCE.msgmii_core_u0/ACT_UNIQUE_MSGMII_CLKRST_1/ASYNC_RESET.rx_clkirst_* } ]
set_false_path -to [ get_pins { CORETSE_C0_0/CORETSE_C0_0/CoreTSE_TOP_INST/
SGMII_INSTANCE.msgmii_core_u0/ACT_UNIQUE_MSGMII_CLKRST_1/ASYNC_RESET.gtx_clkirst_* } ]
set_false_path -to [ get_pins { CORETSE_C0_0/CORETSE_C0_0/CoreTSE_TOP_INST/
SGMII_INSTANCE.msgmii_core_u0/ACT_UNIQUE_MSGMII_CLKRST_1/ASYNC_RESET.pma_rx_clkrst_* } ]
set_false_path -to [ get_pins { CORETSE_C0_0/CORETSE_C0_0/CoreTSE_TOP_INST/
SGMII_INSTANCE.msgmii_core_u0/ACT_UNIQUE_MSGMII_TBI_1/ACT_UNIQUE_PETCR_1/rtex_* } ]
set_false_path -to [ get_pins { CORETSE_C0_0/CORETSE_C0_0/CoreTSE_TOP_INST/
SGMII_INSTANCE.msgmii_core_u0/ACT_UNIQUE_MSGMII_TBI_1/ACT_UNIQUE_PETCR_1/rrex_* } ]
```

It is recommended to use the generated clock constraints for the management clock. PCLK is the source clock. The MGMT CLOCK SELECT field of the MDIO Mgmt: Configuration register (address 0x020) determines the frequency of this clock. An example is shown in the following code block for division factor 8 (MGMT CLOCK SELECT = 3'b011).

```
create_generated_clock -name {MGMT_CLK} -add  -master_clock  PCLK -divide_by 8 -source
[ get_ports { PCLK } ] [ get_pins { CORETSE_C0_0/CORETSE_C0_0/CoreTSE_TOP_INST/tsmac_top_U0/
pe_mcxmac_U0/ACT_UNIQUE_PEMGT_1/mdc/Q } ]
```

It is recommended to use the false path constraints between the clock domains of the CoreTSE IP. The false path constraint is not required between the PCLK and the management clock.

Note: In all the timing constraints provided here, 'CORETSE_C0_0' is the instance name of CoreTSE IP in the Libero Smart Design. User shall replace the instance name while using these timing constraint in the user design.

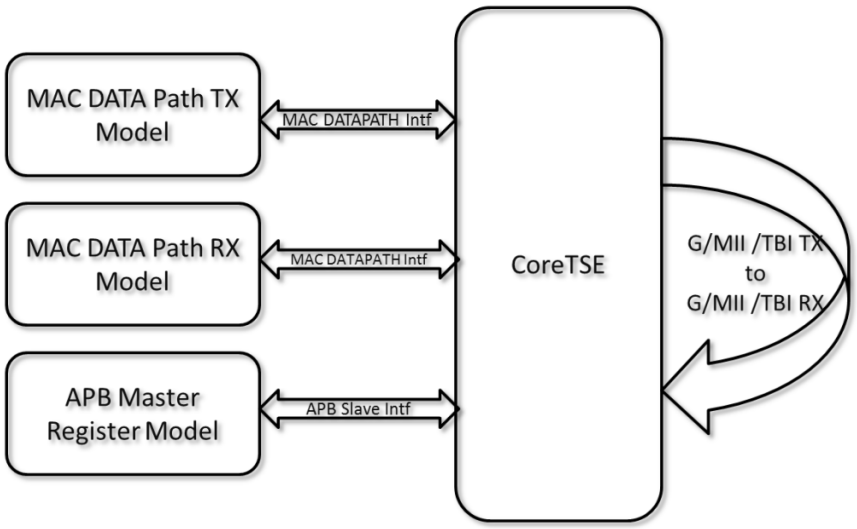
8. Testbench

A unified testbench is used to verify and test CoreTSE called as user testbench.

8.1 User Testbench

A simplified block diagram of the user testbench is shown in the following figure. The user testbench instantiates the CoreTSE with near end loopback at TBI/G/MII interface. Testbench provides behavioral, non-synthesizable MAC data path interface models for descriptors and MAC configurations.

Figure 8-1. CoreTSE User Testbench



Testbench has task based library models for MAC data interface, MAC data transmit, MAC data receive, MAC link transmit, MAC link receive, and generic testbench to check and report errors.

8.1.1 TBI Mode

In TBI mode, the following test case is available:

1. Auto negotiation test case
   - Configure MDIO registers using APB Target register interface for Auto negotiation restart & enable.
   - Waits for auto negotiation completion.
   - Verifies the Auto negation status in MDIO registers and ANX_STATE port status.
2. TBI near end loopback test case
   - Configures MAC registers for full duplex and specific speed mode of operation
   - Test case waits few clocks for CoreTSE to transmit and looped back at TBI interface
   - MAC Data path RX Target model receives the looped back packet and testbench checks for data integrity.
   - Above steps are repeated for 10/100/1000 speed modes with for loop of few iterations.

8.1.2 G/MII Mode

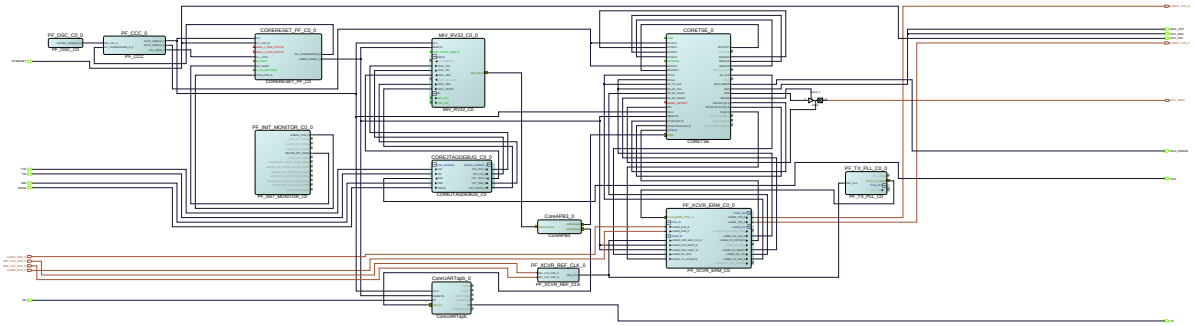
In G/MII mode, the following test cases are available:

1. G/MII near end loopback test case
   - Configures MAC registers for full duplex and specific speed mode of operation.
   - Test case waits few clocks for CoreTSE to transmit and looped back at G/MII interface.
   - MAC Data path RX Target model receives the looped back packet and testbench checks for data integrity.
   - Above steps are repeated for 10/100/1000 speed modes with for loop of few iterations.

9. System Integration

This section provides the details to ease the integration of CoreTSE.

Figure 9-1. CoreTSE System Integration



- FABRIC_RESET_N of CORE_RESET_PF_C0 is used as reset for all modules.
- CoreTSE_0 has PCLK, MTXCLK, MRXCLK, TXCLK, RXCLK, TBI_TX_CLK, TBI_RX_CLK and MDC clocks.
- PCLK is 50MHz clock generated from PF_CCC_0.
- MTXCLK and MRXCLK are 125MHz clocks generated from PF_CCC_0
- TBI_TX_CLK and TXCLK are connected to 125MHz LANE0_TX_CLK_R of PF_XCVR_0.
- TBI_RX_CLK and RXCLK are connected to 125MHz LANE0_RX_CLK_R of PF_XCVR_0.
- 2.5 MHz MDC is generated by CoreTSE_0 from PCLK.

Run the Libero flow with enabling the timing driven and high effort place and route option. The example design can be obtained from the Microchip technical support team.

10. References

Following is a list of documents referred in this user guide.

- SmartFusion2 Microcontroller Subsystem User Guide
- Third-party documents
  For more information about the following documents, contact Microchip technical support team.
  - 802.3-2012_section2.pdf
  - 802.3-2012_section3.pdf

11. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 11-1. Revision History

Revision	Date	Description
C	02/2022	The following is the list of changes in revision C of the document: • Updated Device Utilization and Performance. • Updated Table 3-2 in 3.1. MAC Core Registers. • Updated Table 4-1 in 4.1. Ports. • Updated Table 4-2 in 4.2. Configuration Parameters. • Updated 5.1. License. • Updated Figure 5-1 in 5.3. SmartDesign. • Updated Figure 5-2 in 5.4. Configuring CoreTSE in SmartDesign. • Updated 6.2. Reset.
B	01/2022	The following is the list of changes in revision B of the document: • Updated Device Utilization and Performance. • Updated 1.14. SGMII/Ten-Bit Interface. • Updated 5.1. License. • Updated 7.1. Timing Constraints. • Updated 9. System Integration.
A	12/2021	The following is the list of changes in revision A of the document: • The document was migrated to the Microchip template. • The document number was updated to DS50003245A from 50200549. • Added 6. Clocks and Reset and 7. Design Constraints. • Updated Supported Families. • Updated Device Utilization and Performance. • Updated Table 1-2 in 1.14. SGMII/Ten-Bit Interface. • Updated Table 3-2 in 3.1. MAC Core Registers. • Updated Table 3-3 in 3.2. MAC-FIFO Core Registers. • Updated Table 4-1 in 4.1. Ports. • Updated Table 4-2 in 4.2. Configuration Parameters. • Updated Figure 5-1 in 5.3. SmartDesign. • Updated Figure 5-2 in 5.4. Configuring CoreTSE in SmartDesign. • Updated 5.5. Simulation Flows. • Updated 5.6. Synthesis in Libero SoC. • Updated 5.7. Place-and-Route in Libero SoC. • Replaced Transceiver with XCVR throughout the document. • Removed the Ordering Information section.
4	—	Updated changes related to CoreTSE v3.2.
3	—	Updated changes related to CoreTSE v3.1.
2	—	Updated changes related to CoreTSE v3.0.
1	—	Revision 1.0 was the first publication of this document. Created for CoreTSE v2.0.

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