CoreSDR_AXI v2.0 Release Notes

These release notes accompany the production release for CoreSDR_AXI v2.0. This is the first production release of CoreSDR_AXI. This document provides details about the features, enhancements, supported families, system requirements, implementations, and known limitations and workarounds.

Features

CoreSDR_AXI is a highly configurable core and has the following features:

- High performance, single data rate (SDR) controller for standard static random access memory (SDRAM) chips and dual in-line memory (DIMMs)
- Accesses the advanced extensible interface (AXI) slave interface through the SmartFusion®2 REVFIC64 fabric interface
- Supports 8,16, and 32-bit memory
- Supports up to 1,024 MB of memory
- Bank management logic monitors status of up to 8 SDRAM banks
- Fully synchronous, buffered register interface

Delivery Types

CoreSDR_AXI is licensed in two ways: Obfuscated and register transfer level (RTL).

Obfuscated

Complete RTL code is provided for the core, enabling the core to be instantiated with SmartDesign. Simulation, synthesis, and layout can be performed with Libero® System-on-Chip (SoC) software. The RTL code for the core is obfuscated.

RTL

Complete RTL source code is provided for the core and testbenches.

Supported Families

- SmartFusion2

Supported Tool Flows

Use Libero SoC v11.0 software or later with the CoreSDR_AXI release.

Installation Instructions

For the RTL version of the core, the FlexLM® license must be installed before the core can be exported. Consult Libero SoC online help for the instructions on core installation and licensing.

Documentation

This release contains a copy of the CoreSDR_AXI handbook, which describes core functionality, gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and also provides implementation suggestions.

For updates and additional information about the software, devices, and hardware, visit the Intellectual Property pages on Microsemi® website at: www.microsemi.com/soc.

Supported Test Environments

- Verilog User Testbench

Discontinued Features and Devices

This is the first production release of CoreSDR_AXI.

Known Limitations

This release of CoreSDR_AXI does not support the following:

- AXI transactions that are narrower than the width of the SDR SRAM. For example, when SDR_DQSIZE is 64, 16-bit AXI transaction may not be performed.

Release History

There are no resolved issues in the CoreSDR_AXI v2.0 release. This is the first production release of CoreSDR_AXI.

Table 1 Release History

Version	Date	Changes
2.0	March 2013	Initial release

Known Issues and Workarounds

There are no known issues in this release.

Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo CA 92656 USA
Within the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996

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