CoreSDR v4.3 Release Notes

This document accompanies the production release of CoreSDR v4.3 IP core. It describes the features and enhancements. It also contains the information on system requirements, supported families, implementations, known limitations and workarounds, and resolved issues of previous version.

Features

CoreSDR is a highly configurable core and has the following features:

- High performance, single data rate controller for standard SDRAM chips and DIMMs
- Synchronous interface, fully pipelined internal architecture
- Supports up to 1,024 MB of memory
- Bank management logic monitors status of up to 8 SDRAM banks

Delivery Types

The CoreSDR is licensed as register transfer level (RTL). Complete RTL source code is provided for the core and testbenches.

Supported Families

- Axcelerator®
- RTAX™-S
- ProASIC®3
- ProASIC®3E
- ProASIC®3L
- ProASIC PLUS®
- Fusion®
- SmartFusion®
- SmartFusion®2
- IGLOO®
- IGLOO®e
- IGLOO®2
- IGLOO PLUS®
- RTG4™
- PolarFire
- PolarFire SoC

Supported Tool Flows

This version must be used with Libero® integrated design environment (IDE) v9.2 SP2 or later Libero System-on-Chip (SoC) v11.5 SP2 or later with this CoreSDR release.

Installation Instructions

Within the Libero IDE or SoC software, click **Add Core** in the Catalog to locate and install a local CPZ file, or use the automatic web update feature in Libero IDE or SoC. Once the CPZ file is installed in the Libero IDE or SoC, the core can be instantiated, configured, and generated within SmartDesign for inclusion in your Libero IDE or SoC project. Refer the Libero online help for further instructions on core instantiation, licensing, and general use.

Documentation

For more information about Microsemi Intellectual Property, visit http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores. For updates and additional information about Microsemi software, FPGAs, and hardware, visit http://www.microsemi.com.

Supported Test Environments

The following test environments are supported for CoreSDR:

- Verilog user testbench
- VHDL user testbench
- Verilog Verif testbench
- VHDL Verif testbench (Supported using Mixed Mode)

Discontinued Features and Devices

There are no discontinued features in the v4.3 release.

New Features and Devices

Added VHDL Verif testbench for SDR 64Mx40 which instantiates a Micron 512 Mbit SDRAM model(16Meg x 8x 4 banks) with five instances and SDR 64Mx48 which instantiates a Micron 512 Mbit SDRAM model(16Meg x 8 x 4 banks) with six instances.

Release History

Table 1 details the release history of this core.

Table 1 CoreSDR Release History

Version	Date	Changes
4.3	May 2020	Added VHDL Verif testbench to support SDR 64MX40 and SDR64MX48, and SAR fixes.
4.2	November 2019	Added Verilog Verif testbench to support SDR 64Mx40 and SDR64Mx48, and SAR fixes.
4.1	June 2015	Added SmartFusion2, IGLOO2, RTG4, and SAR fixes
4.0	March 2009	SAR fixes (refer to Table 4) Delivery mechanism through SmartDesign
3.0	May 2007	Delivery mechanism through CoreConsole
2.0	January 2005	Initial version

Resolved Issues in the v4.3 Release

Table 2 lists the Software Action Requests (SARs) that were resolved in the CoreSDR v4.3 release.

Table 2 Resolved Issues in the v4.3 Release

SAR	Description
111357	Added VHDL Verif Testbench support for CoreSDR 64Mx48 and 64Mx40 SDRAM.
111823	Added SDR Initial values r_shift and m_shift in Syn/Asyn Reset as did in SD_INIT always block.

Resolved Issues in the v4.2 Release

Table 2 lists the Software Action Requests (SARs) that were resolved in the CoreSDR v4.2 release.

Table 3 Resolved Issues in the v4.2 Release

SAR	Description
108235	Added support for CoreSDR 64Mx48 and 64Mx40 SDRAM.
91017	Fixed RTL issue for max column address size 13 bits.

Resolved Issues in the v4.1 Release

Table 3 lists the Software Action Requests (SARs) that were resolved in the CoreSDR v4.1 release.

Table 4 Resolved Issues in the v4.1 Release

SAR	Description
66863	Added support for RTG4 family devices.
44933	Core categorization incorrect/incomplete.
36152	Need to check that device family support for this core is correct.

Resolved Issues in the v4.0 Release

Table 4 lists the Software Action Requests (SARs) that were resolved in the CoreSDR v4.0 release.

Table 5 Resolved Issues in the v4.0 Release

SAR	Description
11386, 11880, 11881, 13876	Some CoreSDR parameters are not configurable. Even though the parameters are defined at the top level, if we change some of the parameters, the design breaks, although it is in valid range. The design has been changed to support all ranges of the given parameters.
11404	Table 8 of the handbook shows standard SDR SDRAM device configurations. It is not clear to the user how to use this table. The handbook was updated with more detailed explanation.
11405	Updated the handbook on how to set the SDRAM controller parameters using an example
11707	Changed from $finish to $stop to specify simulation end-point in the verilog user testbench
11756	Updated the wave file with testbench signals
11833	Removed floating signals in the testbench
11834	Removed floating signals in the design
12111	Fixed the issue with load mode register in VHDL base code

Known Issues and Workarounds

There are no known limitations or workarounds in the CoreSDR v4.3.

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