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Release Notes
CorePCS v3.5

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 7.0

Updated changes related to CorePCS v3.5.

1.2 Revision 6.0

Updated changes related to CorePCS v3.4.

1.3 Revision 5.0

Updated changes related to CorePCS v3.3.

1.4 Revision 4.0

Updated changes related to CorePCS v3.2.

1.5 Revision 3.0

Updated changes related to CorePCS v3.1.

1.6 Revision 2.0

Updated changes related to CorePCS v3.0.

1.7 Revision 1.0

Revision 1.0 was the first publication of this document. Created for CorePCS v2.0.

2 CorePCS v3.5 Release Notes

This document accompanies the release of CorePCS v3.5. It describes the features and enhancements of CorePCS v3.5. It also contains the information on system requirements, supported families, implementations, known issues and workarounds, and resolved issues with the previous version.

2.1 Features

CorePCS has the following features:

- 8B10B encoding in the transmitter lane.
- Word alignment and 8B10B decoding in the receiver lane.
- EPCS data width of 10, 20, 40, or 80 bits can be selected, depending on the EPCS_DWIDTH parameter/generic.
- The core can be configured as a transmitter only, receiver only, or both transmitter and receiver, depending on the LANE_MODE parameter/generic.
- Supports 8, 16, 32, or 64 bit word alignment, depending on the SHIFT_EN parameter/generic.
- Fixed or configurable COMMA character detection options for word alignment.

2.2 Delivery Types

CorePCS is license free RTL.

2.2.1 RTL

Complete RTL source code is provided for the core and testbenches.

2.3 Supported Families

CorePCS supports the following families:

- PolarFire™
- RTG4™
- SmartFusion®2
- IGLOO®2

2.4 Supported Tool Flows

Use Libero® System-on-Chip (SoC) software v11.0 or later with the CorePCS v3.5 release.

2.5 Installation Instructions

The CorePCS CPZ file must be installed into Libero software. This is done automatically through the Catalog update function in Libero, or the CPZ file can be manually added using the **Add Core** catalog feature. Once the CPZ file is installed in Libero, the core can be configured, generated, and instantiated within SmartDesign for inclusion in the Libero project.

Refer to the *Libero SoC Online Help* for further instructions on core installation, licensing, and general use.

2.6 Documentation

This release contains a copy of the *CorePCS Handbook*. The handbook, describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and also implementation suggestions. Refer to the *Libero SoC Online Help* for instructions on obtaining IP documentation.

For updates and additional information about the software, devices, and hardware, visit the Intellectual Property pages on the Microsemi SoC Products Group website: visit:

http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores.

2.7 Supported Test Environments

- Verilog user testbench
- VHDL user testbench

2.8 Known Issues and Workarounds

There are no known limitations or workarounds in the CorePCS v3.5 release.

2.9 Release History

Table 1 lists the release history for CorePCS

Table 1 • **Release History**

Version	Date	Changes
3.5	September 2017	SAR fixes and a new parameter/generic added.
3.4	July 2016	Added support for PolarFire.
3.3	January 2015	Added support for RTG4.
3.2	March 2014	Added support for configurable COMMA character detection.
3.1	December 2013	SAR fixes and a new parameter/generic added.
3.0	August 2013	Additional ports added to support more features.
2.0	December 2012	Initial release.

2.10 Resolved Issues in the v3.5 Release

Table 2 lists the SARs that were resolved in the CorePCS v3.5 release

Table 2 • **Resolved SARs in CorePCS v3.5 Release**

SAR	Description
87443	Add support for K28.7 comma characters
87478	min comma char limit for word alignment (for 40bit and 80bit)

2.11 Resolved Issues in the v3.4 Release

There were no resolved issues in the v3.4 release.

2.12 Resolved Issues in the v3.3 Release

Table 3 lists the SARs that were resolved in the CorePCS v3.3 release

Table 3 • **Resolved SARs in CorePCS v3.3 Release**

SAR	Description
60601	Change default consecutive K28.5 characters.

2.13 Resolved Issues in the v3.2 Release

Table 4 lists the SARs that were resolved in the CorePCS v3.2 release

Table 4 • **Resolved SARs in CorePCS v3.2 Release**

SAR	Description
54362	Add programmable COMMA character support.

2.14 Resolved Issues in the v3.1 Release

Table 5 lists the SARs that were resolved in the CorePCS v3.1 release

Table 5 • **Resolved SARs in CorePCS v3.1 Release**

SAR	Description
53212	Add parameter to enable shifting of the data.
53196	Encoded value mismatch when FORCE_DISP enabled.

2.15 Resolved Issues in the v3.0 Release

Table 6 lists the SARs that were resolved in the CorePCS v3.0 release

Table 6 • **Resolved SARs in CorePCS v3.0 Release**

SAR	Description
47717	Add ability to force disparity on transmit.
47718	Add word aligner reset port to support external link state machine.
49406	Add signal to indicate that the core is word aligned.

2.16 Resolved Issues in the v2.0 Release

As this is the initial version, there were no SARs resolved in the v2.0 release.