RN0103

Release Notes

CoreMMC v3.0

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a Microchip company

Contents

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 4.0

Revision 4.0 was published in June 2018. In this revision, CLK_OE and CLKI ports are removed.

1.2 Revision 3.0

Revision 3.0 was published in May 2018. The following changes are made in revision 3.0 of the document.

- Added Multiple block support
- FIFO width changed from 8- to 32-bit
- DMA control signals asserted on a 32-bit basis
- Created BFM based user testbench
- Added VHDL support
- Added IGLOO2 support
- Added PolarFire support

1.3 Revision 2.0

Revision 2.0 was published in October 2013. It was the first publication of this document.

2 CoreMMC v3.0 Release Information

This document accompanies the release of CoreMMC v3.0. It describes the features and enhancements of CoreMMC v3.0. It also contains the information on system requirements, supported families, implementations, known issues and workarounds, and resolved issues in the previous version.

2.1 Key Features

The key supported features in CoreMMC are as follows:

- Up to 52 MHz MMC clock rate, making for a maximum of ~52 MBs throughput at 8-bit data width (theoretical throughput of CoreMMC. Actual throughput will be affected by eMMC device throughput and AHB bandwidth)
- Configurable data bus widths
  - 1-/4-/8-bit
- Supports Block mode transfer:
  - Single block write
  - Multiple block write
  - Single block read
  - Multiple block read
- Cyclic redundancy check (CRC) protection for both commands and data transfers
- AHB-Lite compliant
  - Command, Response, Write, and Read Data registers for indirect access to MMC part
  - 8-/16-/32-bit AHB transfers
- Write DATA FIFO:
  - To decouple AHB from MMC bus for write data transfers
  - Depth configurable from 512 bytes to 32 KB
  - Overrun and Underrun error flags
- Read DATA FIFO:
  - To decouple AHB from MMC bus for read data transfers
  - Depth configurable from 512 bytes to 32 KB
  - Overrun and Underrun error flags
- Interrupt generation:
  - Command sent and response received interrupts
  - Error flag interrupt
  - Single block write and read done interrupt
  - Multiple block write and read done interrupts
- Automatic Sleep mode for eMMC when clock pulls Low

2.2 Supported Interfaces

CoreMMC supports the following interfaces.

- AHB-Lite slave interface
- Interrupt request interface
- MMC master interface
- Peripheral direct memory access (PDMA) interface

2.3 Delivery Types

A License is not required for using CoreMMC v3.0 .

2.3.1 Register Transfer Level (RTL)

The complete RTL source code is provided for the core and testbenches.

2.4 Supported Families

CoreMMC supports the following families.

- SmartFusion®2
- IGLOO®2
- PolarFire®

2.5 Supported Tool Flows

CoreMMC supports the following tools.

- Libero® System-on-Chip (SoC) software v11.1 or later
- Supports Windows and Linux operating systems

2.6 Installation Instructions

The CoreMMC CPZ file must be installed in the Libero software. This is installed automatically through the Catalog update function in the Libero software or the .CPZ file can be manually added using the **Add Core** catalog feature. Once installed in the Libero software Catalog, the core can be instantiated and configured. Refer to Libero SoC online help for further instructions on core installation, licensing, and general use.

2.7 Documentation

The release contains a copy of the *CoreMMC Handbook*. The handbook describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, along with implementation suggestions. For updates and additional information about the software, devices, and hardware, visit the intellectual property pages on the Microsemi SoC Products Group website at http://www.microsemi.com/soc.

2.8 Supported Test Environments

Verilog and VHDL user testbench test environments are supported by CoreMMC.

2.9 Known Issues and Workarounds

CoreMMC does not support the following features.

- Sequential mode transfers
- Stream Read and Stream Write
- ECC error correction (handled on the device side instead)
- Double data rate (DDR) for this release
- Boot mode
- Selecting VHDL 2008 syntax when using VHDL source code

3 Release History

The following tables show the release history for CoreMMC.

3.1 Resolved Issues in v3.0 Release

Table 1 • Resolved SARs in CoreMMC v3.0 Release

SAR	Description
67363	Clock register description updated in Handbook
67461	Added multiple block support to increase CoreMMC throughput
54007	VHDL support added

3.2 Resolved Issues in v2.0 Release

Table 2 • Resolved SARs in CoreMMC v2.0 Release

SAR	Description
-	Initial Release

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