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CoreLSM v2.0 Release Notes





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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.0

Revision 1.0 is the first publication of this document. Created for CoreLSM v2.0.

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2 CoreLSM v2.0 Release Notes

2.1 Overview

These release notes accompany the production release of CoreLSM v2.0. This document provides details about the features, enhancements, system requirements, supported families, implementations, and known issues and workarounds.

2.2 Features

- Identifies when a link is word aligned
- Identifies Code Violations and Disparity Errors and increments the respective counter
- If the maximum number of Code Violations or Disparity Errors are not met within the 2^{32} clock cycles then the counters are reset

2.3 Delivery Types

No License is required to use CoreLSM. Complete RTL source code is provided for the core.

2.4 Supported Families

- PolarFire™

2.5 Supported Tool Flows

CoreLSM v2.0 requires Libero® System-on-Chip (SoC) PolarFire software v12.0 or later.

2.6 Installation Instructions

The CoreLSM CPZ file must be installed into Libero software. This is done automatically through the Catalog update function in Libero, or the CPZ file can be manually added using the **Add Core** catalog feature. Once the CPZ file is installed in Libero, the core can be configured, generated, and instantiated within SmartDesign for inclusion in the Libero project.

Refer to the [Libero SoC Online Help](#) for further instructions on core installation, licensing, and general use.

2.7 Documentation

This release contains a copy of the *CoreLSM Handbook*. The handbook, describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and also implementation suggestions. Refer to the [Libero SoC Online Help](#) for instructions on obtaining IP documentation.

For updates and additional information about the software, devices, and hardware, visit the Intellectual Property pages on the Microsemi SoC Products Group website: visit:

<http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores>.

2.8 Resolved History

Table 1 lists the release history for CoreLSM.

Table 1 • Release History

Version	Date	Changes
2.0	September 2017	Initial release.

2.9 Known Limitations and Workarounds

There are no known limitations and workarounds for CoreLSM.