RN0009

CorеI2C v7.2 Release Notes

Microsemi
Power Matters.™

Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA
Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996
E-mail: sales.support@microsemi.com
www.microsemi.com

About Microsemi

Microsemi Corporation (Nasdaq: MSCC) offers a comprehensive portfolio of semiconductor and system solutions for aerospace & defense, communications, data center and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; enterprise storage and communication solutions, security technologies and scalable anti-tamper products; Ethernet solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, Calif., and has approximately 4,800 employees globally. Learn more at www.microsemi.com.

51300009-9/5.17

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 9.0

Updated changes related to CoreI2C v7.2.

1.2 Revision 8.0

Updated changes related to CoreI2C v7.1.

1.3 Revision 7.0

Updated changes related to CoreI2C v7.0.

1.4 Revision 6.0

Updated changes related to CoreI2C v6.0.

1.5 Revision 5.0

Updated changes related to CoreI2C v5.0.

1.6 Revision 4.0

Updated changes related to CoreI2C v4.0.

1.7 Revision 3.0

Updated changes related to CoreI2C v3.0.

1.8 Revision 2.0

Updated changes related to CoreI2C v2.1.

1.9 Revision 1.0

Revision 1.0 was the first publication of this document. Created for CoreI2C v2.0.

Contents

2 CorеI2C v7.2 Release Notes

2.1 Overview

These release notes accompany the production release of CorеI2C v7.2. This document provides details about the features, enhancements, system requirements, supported families, implementations, and known issues and workarounds.

2.2 Features

CorеI2C provides an APB-driven serial interface, supporting I2C, SMBus, and PMBus data transfers. Several Verilog/VHDL parameters are available to minimize FPGA fabric area for a given application. CorеI2C also allows for multiple I2C channels, reusing logic across channels to reduce overall tile count.

CorеI2C has the following features:

- Conforms to the Philips Inter-Integrated circuit (I2C) v2.1 Specification (7-bit addressing format at 100 Kbps and 400 Kbps data rates)
- Supports SMBus v2.0 Specification
- Supports PMBus v1.1 Specification
- Data transfers up to at least 400 kbps nominally; faster rates can be achieved depending on external load and/or I/O pad circuitry
- Modes of operation configurable to minimize size
- Advanced peripheral bus (APB) register interface
- Multi-master collision detection and arbitration
- Own address and general call address detection
- Second Slave address decode capability
- Data transfer in multiples of bytes
- SMBus timeout and real-time idle condition counters
- IPMI 3 ms SCL low timeout
- Optional SMBus signals, SMBSUS_N and SMBALERT_N, controllable through APB IF
- Configurable spike suppression width
- Multiple channel configuration option

2.3 Supported Interfaces

CorеI2C supports the following interfaces:

- APB slave interface
- Interrupt request interface
- Serial (I2C) interface

2.4 Delivery Types

No License is required to use CorеI2C. A complete hardware description language (HDL) source code is provided for the core and testbench.

2.5 Supported Families

CorеI2C v7.2 is a generic core and supports all the device families.

2.6 Supported Tool Flows

CorеI2C v7.2 requires Libero v8.6 or later.

Note: CorеI2C is compatible with Libero Integrated Design Environment (IDE), Libero System-on-Chip (SoC), and Libero System-on-Chip (SoC) PolarFire. Unless specified otherwise, this document uses the name Libero to identify Libero IDE, Libero SoC, and Libero SoC PolarFire.

2.7 Installation Instructions

The CoreI2C CPZ file must be installed into Libero software. This is done automatically through the Catalog update function in Libero, or the CPZ file can be manually added using the **Add Core** catalog feature. Once the CPZ file is installed in Libero, the core can be configured, generated, and instantiated within SmartDesign for inclusion in the Libero project.

Refer to the *Libero SoC Online Help* for further instructions on core installation, licensing, and general use.

2.8 Documentation

This release contains a copy of the *CoreI2C Handbook*. The handbook, describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and also implementation suggestions. Refer to the *Libero SoC Online Help* for instructions on obtaining IP documentation.

For updates and additional information about the software, devices, and hardware, visit the Intellectual Property pages on the Microsemi SoC Products Group website: visit:

http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores.

2.9 Supported Test Environments

- Verilog user testbench
- VHDL user testbench

2.10 Release History

Table 1 lists the release history for CoreI2C

Table 1 • **Release History**

Version	Date	Changes
7.2	May, 2017	Re-packaged CoreI2C as a generic core supporting all device families.
7.1	December, 2014	Added support for RTG4 family devices. Resolved issue with disabling CoreI2C whilst SCL line low. CoreI2C no longer enters deadlock when the core is disabled whilst the SCL line is low.
7.0	June, 2011	Interrupt generation after STOP bit is sent. I2C slave 2nd address capability functionality corrected (SAR 30964). Operation details for Master mode example updated.
6.0	November, 2009	Remove 50 µs SMBus idle condition check (not required). Multiple channel mode, up to 16 I^2C/SMBus channels on a single APB interface. Improved tile utilization.
5.0	November, 2008	Added the ability to further reduce tile count by hardwiring some configuration parameters. Added IPMI SCL low timeout functionality. Added second slave address capability. Configurable spike suppression width.
4.0	August, 2008	Start hold timing violation corrected. Serviced many software action requests (SARs). SMBus/PMBus functionality added to v4.0. IGLOO/e device support added. Added synthesis constraint to prevent Synopsys® tile error when using FSM compiler. Added Master Transmit and Slave Receive modes to reduce tile counts for write-only applications.
3.0	November, 2007	Switched from SFR to APB interface.
2.1	January, 2005	Discontinued support of Actel A54SX and eX families.
2.0	August, 2003	Initial release.

2.11 Resolved Issues in the v7.2 Release

Table 2 lists the Software Action Requests (SARs) that were resolved in the CoreI2C v7.2 release.

Table 2 • **Resolved Issues in the v7.2 Release**

SAR	Description
68127	List of device families in phase0 doc and package do not match.

2.12 Resolved Issues in the v7.1 Release

Table 3 lists the Software Action Requests (SARs) that were resolved in the CoreI2C v7.1 release.

Table 3 • **Resolved Issues in the v7.1 Release**

SAR	Description
59782	Added SmartFusion2 and IGLOO2 to the supported families list.
60104	Added ProASIC3L to the supported families list.
57406	Added support for RTG4 family devices.
53359	Resolved issue with disabling CoreI2C whilst SCL line low. CoreI2C no longer enters deadlock when the core is disabled whilst the SCL line is low.

2.13 Resolved Issues in the v7.0 Release

Table 4 lists the SARs that were resolved in the CoreI2C v7.0 release.

Table 4 • **Resolved Issues in the v7.0 Release**

SAR	Description
25023	A pending Master Tx aborts (NACK) concurrent Slave Rx.
25400	SMBus Timeout Issue During Master TX/RX transaction.
25401	IPMI timeout issue during Master TX/RX transactions.
29537	Generate an interrupt after STOP bit is set.
30964	I2C slave 2nd address capability doesn't work.

2.14 Resolved Issues in the v6.0 Release

Table 5 lists the SARs that were resolved in the CoreI2C v6.0 release

Table 5 • **Resolved Issues in the v6.0 Release**

SAR	Description
20288	Remove 50 µS SMBus idle condition check (not required).

2.15 Resolved Issues in the v5.0 Release

Table 6 lists the SARs that were resolved in the CoreI2C v5.0 release.

Table 6 • **Resolved Issues in the v5.0 Release**

SAR	Description
78614	Fixed GlitchReg Value parameter.
78611	Required SMBus Optional Signal Interrupts.
78608	3 ms IPMI timeout required.
78610	IPMI extra Slave Address mode
78609	Fixed Slave Address mode for decreasing tile count
78613	Changed I2CCLK and I2CDAT signals to SCL/SDA.
78612	Fixed Baud Rate (saves about 50 tiles)
78560	The SMBUS signals float when not in use

2.16 Resolved Issues in the v4.0 Release

Table 7 lists the SARs that were resolved in the CoreI2C v4.0 release

Table 7 • **Resolved Issues in the v4.0 Release**

SAR	Description
78449	Device/family metadata issues - v4.0.106.
78444	Added synthesis constraint to prevent Synplicity tile error.
78443	Added SMBus functionality.
78220	CCZ verification: Synthesis warnings
77968	Request for a Master Transmit, Slave Receive mode to reduce tile counts for IPMI or any write-only application
77967	Start hold timing violation corrected.
69300	The handbook needs to describe the open drain I/O.
68890	CoreI2C simulation in Evaluation mode
68382	Utilization in VHDL is about two times that of Verilog.
68111	SPIRIT description missing link between APBslave i/f and RegisterMap
67496	CoreI2C shows up under non-AMBA bus list.
67475	The link to the datasheet for CoreI2C in CoreConsole does not work.
67474	Block diagram for CoreI2C does not show BCLK.
67450	CoreConsole does not generate C code for I^2C.
66806	Update the Data Transfers rate.
66574	Request to show the open drain configuration in the handbook.
65986	Data should be labeled PWDATA instead of PRDATA.
62885	Link to datasheet in core description is broken.

2.17 Resolved Issues in the v3.0 Release

Table 8 lists the SARs that were resolved in the CoreI2C v3.0 release.

Table 8 • **Resolved Issues in the v3.0 Release**

SAR	Description
62412	An APB interface has been added and the SFR interface has been removed for use with CoreConsole in bus-centric designs.
57330	The datasheet provided with previous versions of the core incorrectly described serdati as “serial clock input.” The datasheet has since been superseded by a handbook, which accurately describes the serial data input (I2CDATI).

2.18 Known Limitations and Workarounds

There are no known limitations and workarounds for CoreI2C v7.2.

2.19 Discontinued Features and Devices

No features have been discontinued in the CoreI2C v7.2 release.