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CoreGPIO v3.2 Release Notes

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 6.0

Updated changes related to CoreGPIO v3.2.

1.2 Revision 5.0

Updated changes related to CoreGPIO v3.1.

1.3 Revision 4.0

Updated changes related to CoreGPIO v3.0.

1.4 Revision 3.0

Updated changes related to CoreGPIO v2.0.

1.5 Revision 2.0

Updated changes related to CoreGPIO v1.2.

1.6 Revision 1.0

Revision 1.0 was the first publication of this document. Created for CoreGPIO v1.0.

Contents

2 CoreGPIO v3.2 Release Notes

2.1 Overview

These release notes accompany the production release of CoreGPIO v3.2. This document provides details about the features, enhancements, system requirements, supported families, implementations, and known issues and workarounds.

CoreGPIO provides an advanced peripheral bus (APB) register-based interface to up to 32 general purpose inputs and 32 general purpose outputs. The input logic contains a simple 3-stage synchronization circuit and the output is set synchronously. Each bit can be set to either a fixed or register-based configuration via top-level parameters, including input type, interrupt type/enable, and output enable.

2.2 Features

CoreGPIO has the following features:

- Advanced microcontroller bus architecture (AMBA) 2 APB support, forward compatibility with AMBA 3 APB
- 8-, 16-, or 32-bit APB data width
- 1 to 32 bits of I/O for all APB-width configurations
- Fixed or configurable interrupt generation:
  - Negative edge
  - Positive edge
  - Both edges
  - Level high
  - Level low
- Parameter-configurable for single-interrupt signal or up to 32-bit wide interrupt bus
- Fixed or configurable I/O type (input, output, or both)
- Configurable output enable (internal or external implementation)

2.3 Interfaces

CoreGPIO is available with an AMBA APB register interface.

2.4 Delivery Types

No license is required to use CoreGPIO. Complete RTL source code is provided for the core and testbench.

2.5 Supported Families

CoreGPIO is a generic core and supports all the device families.

2.6 Supported Tool Flows

This version must be used with Libero® Integrated Design Environment (IDE) v8.6 or System-on-Chip (SoC) v11.5 or later.

2.7 Installation Instructions

The CoreGPIO CPZ file must be installed into Libero software. This is done automatically through the Catalog update function in Libero, or the CPZ file can be manually added using the **Add Core** catalog feature. Once the CPZ file is installed in Libero, the core can be configured, generated, and instantiated within SmartDesign for inclusion in the Libero project.

Refer to the *Libero SoC Online Help* for further instructions on core installation, licensing, and general use.

2.8 Documentation

This release contains a copy of the *CoreGPIO Handbook*. The handbook, describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and also implementation suggestions. Refer to the *Libero SoC Online Help* for instructions on obtaining IP documentation.

For updates and additional information about the software, devices, and hardware, visit the Intellectual Property pages on the Microsemi SoC Products Group website: visit:

http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores.

2.9 Supported Test Environments

- Verilog user testbench
- VHDL user testbench

2.10 Resolved History

Table 1 lists the release history for CoreGPIO.

Table 1 • **Release History**

Version	Date	Changes
3.2	June 2017	• Resolved SARs listed in Table 2. • Re-packaged CoreGPIO as a generic core supporting all device families.
3.1	February 2015	• Resolved SARs listed in Table 3. • Added RTG4 support.
3.0	August 2009	• Resolved SARs listed in Table 4. • Updated for Libero IDE v8.5. • Added variable APB data width support. • Added per-bit configurability. • Added interrupt generation. • Added output enable.
2.0	July 2008	• Minor fixes.
1.2	August 2007	• Added support for GPIO widths other than 8 bits.
1.0	December 2005	• First Production release.

2.10.1 Resolved Issues in the v3.2 Release

Table 2 lists the Software Action Requests (SARS) that were resolved in the CoreGPIO v3.2 release.

Table 2 • **Resolved Issues in the v3.2 Release**

SAR Number	Changes
21606	No memory / register map defined in packaging.
63100	Min configuration in HB does not match.
68353	Spelling error in the CoreGPIO configurator.
57173	CoreGPIO simulation error.
26094	Interrupt Clear register is actually Interrupt Status (R) and Interrupt Clear (W) register.
22750	Output on reset ” redundant for I/O bits set as input.
20407	Packaged docs are in <core-root> not <core-root>/docs.
21763	CoreGPIO replicates IO bits on both GPIO_IN and GPIO_OUT ports.

2.10.2 Resolved Issues in the v3.1 Release

Table 3 lists the Software Action Requests (SARS) that were resolved in the CoreGPIO v3.1 release.

Table 3 • **Resolved Issues in the v3.1 Release**

SAR Number	Changes
57399	Added RTG4 support.

2.10.3 Resolved Issues in the v3.0 Release

Table 4 lists the Software Action Requests (SARS) that were resolved in the CoreGPIO v3.0 release.

Table 4 • **Resolved Issues in the v3.0 Release**

SAR Number	Changes
11663 11759	Added 8-, 16-, 32-bit mode to testbench.
11959	Added handbook to core package.
11593	Split VHDL package and VHDL top-level entity.
11805	Added support for reset value configuration.
11689 11475	Added support for 8-, 16-, and 32-bit mode in core.

2.10.4 Resolved Issues in the v2.0 Release

No resolved issues in the v2.0 release.

2.10.5 Resolved Issues in the v1.2 Release

No resolved issues in the v1.2 release.

2.11 Known Issues and Workarounds

There are no known limitations or workarounds in the CoreGPIO v3.2 release.