RN0060
Release Notes
CoreEDAC v2.10

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Contents

Tables

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 11.0

Updated changes related to CoreEDAC v2.10.

1.2 Revision 10.0

Updated changes related to CoreEDAC v2.9.

1.3 Revision 9.0

Updated changes related to CoreEDAC v2.8.

1.4 Revision 8.0

Updated changes related to CoreEDAC v2.7.

1.5 Revision 7.0

Updated changes related to CoreEDAC v2.6.

1.6 Revision 6.0

Updated changes related to CoreEDAC v2.5.

1.7 Revision 5.0

Updated changes related to CoreEDAC v2.4.

1.8 Revision 4.0

Updated changes related to CoreEDAC v2.3.

1.9 Revision 3.0

Updated changes related to CoreEDAC v2.2.

1.10 Revision 2.0

Updated changes related to CoreEDAC v2.1.

1.11 Revision 1.0

Revision 1.0 was the first publication of this document. Created for CoreEDAC v2.0.

2 CoreEDAC v2.10 Release Notes

This document accompanies the release of CoreEDAC v2.10. It describes the features and enhancements of CoreEDAC v2.10. It also contains the information on system requirements, supported families, implementations, known issues and workarounds, and resolved issues with the previous version.

2.1 Features

CoreEDAC has the following features:

- Parameterizable RTL generator.
- Modes of operation:
  - Error detection and correction (EDAC) with internal RAM. EDAC RAM generation with optional background scrubbing circuitry.
  - EDAC encoder and decoder generation. The mode can be used to apply EDAC encoder and decoder to external memories.
- Flexible user data size from 4 to 64 bits. This corresponds to a codeword size from 8 to 72 bits.
- User-defined pipeline options to enhance EDAC throughput.
- Parameterizable refresh (scrubbing) rate.
- Improved latency and area characteristics.
- Correctable and error flags.
- Option to suppress writeback during the scrubbing session.
- Optional triple EDAC redundancy.

2.2 Interfaces

No standard interface available.

2.3 Delivery Types

No license is required to use CoreEDAC. Complete RTL source code is provided for the core and testbench.

Note: CoreEDAC is compatible with both Libero integrated design environment (IDE) and Libero SoC. Unless specified otherwise, this document uses the common name Libero to identify Libero IDE and Libero SoC.

2.4 Supported Families

CoreAHBLite supports the following families:

- PolarFire™
- RTG4™
- SmartFusion®2
- IGLOO®2
- SmartFusion®
- IGLOO®
- IGLOO®e
- IGLOO® PLUS
- Fusion®
- ProASIC®3
- ProASIC®3E
- ProASIC®3L
- Axcelerator®
- RTAX-S
- RTAX-D
- ProASIC^{PLUS}

2.5 Supported Tool Flows

- CoreEDAC v2.10 requires the Libero software v9.1 or later.
- Supports Windows® and Linux operating systems.

2.6 Installation Instructions

The CoreEDAC CPZ file must be installed into Libero software. This is done automatically through the Catalog update function in Libero, or the CPZ file can be manually added using the **Add Core** catalog feature. Once the CPZ file is installed in Libero, the core can be configured, generated, and instantiated within SmartDesign for inclusion in the Libero project.

Refer to the *Libero SoC Online Help* for further instructions on core installation, licensing, and general use.

2.7 Documentation

This release contains a copy of the *CoreEDAC Handbook*. The handbook, describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and also implementation suggestions. Refer to the *Libero SoC Online Help* for instructions on obtaining IP documentation.

For updates and additional information about the software, devices, and hardware, visit the Intellectual Property pages on the Microsemi SoC Products Group website: visit:

http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores.

2.8 Supported Test Environments

The following test environments are supported:

- Verilog user testbench
- VHDL user testbench

2.9 Resolved History

Table 1 lists the release history for CoreEDAC.

Table 1 • **Release History**

Version	Date	Changes
2.10	October 2017	Resolved SARs listed in Table 2.
2.9	July 2017	Resolved SARs listed in Table 3.
2.8	December 2015	Resolved SARs listed in Table 4.
2.7	August 2015	Resolved SARs listed in Table 5.
2.6	February 2015	Support for RTG4 family is added and reported issues are fixed.
2.5	November 2013	Resolved SARs listed in Table 7.
2.4	August 2013	FPGA fabric register replaces a hard RAM macro read data pipeline on AX and RTAX-S/SL/DSP devices.
2.3	June 2013	Support for multiple EDAC instances.
2.2	March 2013	Resolved SARs listed in Table 10.
2.1	February 2012	Maintenance, fix for VHDL synthesis error and reducing the number of synthesis warnings. Optional error injection test port added.
2.0	January 2009	First Production release.

2.10 Resolved Issues in the v2.10 Release

Table 2 • **Resolved SARs in CoreEDAC v2.10 Release**

SAR	Description
92242	Provide PolarFire support

2.11 Resolved Issues in the v2.9 Release

Table 3 • **Resolved SARs in CoreEDAC v2.9 Release**

SAR	Description
83017	Handbook update related to timing diagram with NGRST and RST, related to RAM simulation and update on START_SCRUB, STOP_SCRUB and RST_TIMER ports and '?' is observed in CoreEDAC hierarchy.
89984	Handbook corrections related to ERROR/CORRECTABLE flags.

2.12 Resolved Issues in the v2.8 Release

Table 4 • **Resolved SARs in CoreEDAC v2.8 Release**

SAR	Description
69637	Add IGLOO2 family to a packager list
74020	Eliminate difference between pre- and post-synthesis simulation results

2.13 Resolved Issues in the v2.7 Release

Table 5 • **Resolved SARs in CoreEDAC v2.7 Release**

SAR	Description
64039	Minor HB correction
68390	Add RTG4 Utilization and performance numbers to the HB
68546	Fix VHDL code causing simulation failure when AX or RTAX families are selected

2.14 Resolved Issues in the v2.6 Release

Table 6 • **Resolved SARs in CoreEDAC v2.6 Release**

SAR	Description
11878	Limit the minimal scrubbing period by ten times the protected RAM depth
45742	Eliminate RAM initialization on synchronous RST signal. The initialization should only start on asynchronous NGRST signal that signifies powering of an FPGA device
55647	Fix VHDL initialization circuitry
61231	Reset TimerCnt upon scrubbing completion
61305	Provide flexible RAM generator DEVICE parameter value based on actual FPGA device selection
62323	Provide RTG4 support

2.15 Resolved Issues in the v2.5 Release

Table 7 • **Resolved SARs in CoreEDAC v2.5 Release**

SAR	Description
39138	Hide IP symbol unused ports on the SmartDesign canvas view when the core is configured for ECC Codec mode.
50680	Fixed incomplete scrubbing that can occur when a user interrupts the scrubbing.

2.16 Resolved Issues in the v2.4 Release

Table 8 • **Resolved SARs in CoreEDAC v2.4 Release**

SAR	Description
49523	The SAR was resolved in the v2.4 release of CoreEDAC. The SAR requested hard RAM read data pipeline to be bypassed on AX and RTAX-S/SL/DSP devices. Instead an FPGA fabric-based register is used when necessary.

2.17 Resolved Issues in the v2.3 Release

Table 9 • **Resolved SARs in CoreEDAC v2.3 Release**

SAR	Description
48154	Support for multiple core instances

2.18 Resolved Issues in the v2.2 Release

Table 10 • **Resolved SARs in CoreEDAC v2.2 Release**

SAR	Description
22618	Scrubber must not overwrite fresh user data
38358	Support for SmartFusion2 family
39584	Add CODE_FROM_RAM port to be used with external memories
40613	Better differentiation between flags raised during user access and scrubbing
40804	Fix a design error preventing scrubber of processing the last RAM address
43052	Suppress ERROR/CORRECTABLE flags until valid user read data appear at the output

2.19 Resolved Issues in the v2.1 Release

Table 11 • **Resolved SARs in CoreEDAC v2.1 Release**

SAR	Description
20147	Reduce number of synthesis warnings and eliminate a fatal simulation error.
24067	Implement user access to the optional error injection test port.
22315	Eliminate VHDL synthesis error.
30469	Eliminate VHDL synthesis error.
31782	Eliminate VHDL synthesis error.
33092	Eliminate VHDL synthesis error.
32157	Remove a handbook inaccurate resource utilization note.

2.20 Discontinued Features and Devices

There are no discontinued features or devices.

2.21 Known Issues and Workarounds

USER_REN_TRPx ports are not available when SmartFusion2, IGLOO2, RTG4, or PolarFire micro-RAM is used (URAM = 1). In that configuration the micro-RAM read output is always enabled.