CoreDDR v4.0 Release Notes

This is the production release for the CoreDDR IP core. These release notes describe the features and enhancements. They also contain information about system requirements, supported families, implementations, and known issues and workarounds.

Features

CoreDDR is a highly configurable core and has the following features:

• High performance, double data rate controller for standard SDRAM chips and DIMMs

• Synchronous interface, fully pipelined internal architecture

• Supports up to 1,024 MB of memory

• Bank management logic monitors status of up to four SDRAM banks

• Extensive test suite

Delivery Types

The CoreDDR core is licensed in two ways: Obfuscated and RTL.

Obfuscated

Complete RTL code is provided for the core, enabling the core to be instantiated with SmartDesign. Simulation, Synthesis, and Layout can be performed with Actel Libero® Integrated Design Environment (IDE). The RTL code for the core is obfuscated and the some of the testbench source files are not provided. They are precompiled into the compiled simulation library instead.

RTL

Complete RTL source code is provided for the core and testbenches.

Supported Families

ProASIC®3E

Fusion

Supported Tool Flows

Use Libero IDE v8.5 or later with this CoreDDR release.

Install Instructions

Within Libero IDE, click the **Add Core** button in the Catalog to locate and install a local CCZ file, or use the automatic web update feature in Libero IDE. Once the CCZ file is installed in Libero IDE, the core can be instantiated, configured, and generated within SmartDesign for inclusion in your Libero IDE project. Refer to the Libero IDE online help for further instructions on core instantiation, licensing, and general use.

Documentation

The release contains a copy of the CoreDDR Handbook. The handbook describes the core functionality, gives implementation suggestions, and provides step-by-step instructions on how to simulate, synthesize, and place-and-route this core.

For updates and additional information about the software, devices, and hardware, visit the Intellectual Property pages on the Actel website at http://www.actel.com.

Supported Test Environments

The following test environments are supported for CoreDDR:

- Verilog user testbench
- VHDL user testbench

Discontinued Features and Devices

None

New Features and Devices

The following new features and devices are included in the v4.0 release:

- Delivery mechanism is now through SmartDesign

Release History

Table 1 details the release history of this core

Table 1 · CoreDDR Release History

Core Version	Date	Changes
4.0	June 09	SAR fixes (refer to Table 3 on page 3). Delivery mechanism through SmartDesign.
3.0	May 07	SAR fixes (refer to Table 2 on page 2). Delivery mechanism through CoreConsole.
2.0	May 04	Initial version

Resolved Issues in the v4.0 Release

Table 2 lists Software Action Requests (SARs) that were resolved in the CoreDDR v4.0 release.

Table 2 · Resolved Issues in the CoreDDR v4.0 Release

SAR No.	Description
11824	Updated the RTL to work with configurable parameters.
12120	Fixed the wrong default value set on No. Of Column Bits to correct default value.

Resolved Issues in the v3.0 Release

Table 2 lists Software Action Requests (SARs) that were resolved in the CoreDDR v3.0 release.

Table 3 · Resolved Issues in the CoreDDR v3.0 Release

SAR No.	Description
56067	Generated PLL with latest version of SmartGen.

Known Issues and Workarounds

None

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