CoreCORDIC v4.0 Release Notes

This document accompanies the production release of CoreCORDIC v4.0 IP core. It describes the features, enhancements, system requirements, supported families, implementations, known issues and workarounds, and resolved issues of previous version.

Key Features

CoreCORDIC has the following key features:

- Parameterizable RTL generator
- Functional modes:
  - General vector rotation
  - Conversion from Polar to Rectangular co-ordinates
  - Translation from Rectangular to Polar co-ordinates
  - Sine and Cosine calculation
  - Arctangent (angle) calculation
- Configurable 8 to 48 bits input and output data bit resolution
- Automatic or user-controllable precision of internal calculations up to 48 bits
- Variety of output rounding options:
  - Truncation
  - Convergent rounding (round to nearest even)
  - Symmetric rounding (round to positive or negative infinity)
  - Round up (round to positive infinity)
- Word-serial architecture for smaller area
- Parallel architecture for high throughput
- Configurable number of iterations up to 48
- Synchronous design using a single clock

Supported Interfaces

CoreCORDIC does not have any standard interface available.

Delivery Types

CoreCORDIC is distributed with Libero® System-on-Chip (SoC) or Integrated Design Environment (IDE) design software. Complete hardware description language (HDL) source code is provided for the core and testbenches.

Note: CoreCORDIC is compatible with both Libero IDE and Libero SoC. Unless specified otherwise, this document uses the common name Libero to identify Libero IDE and Libero SoC.

Supported Families

CoreCORDIC v4.0 supports the following families:

- SmartFusion®2
- IGLOO®2
- IGLOO®
- IGLOOe
- IGLOO^{PLUS}
- RTG4™
- ProASIC®3
- ProASIC3E
- ProASIC3L
- ProASIC^{PLUS}
- SmartFusion®
- Fusion
- Axcelerator®
- RTAX-S/SL and RTAX-DSP

Supported Tool Flows

CoreCORDIC v4.0 supports the following tool flows:

- CoreCORDIC v4.0 requires the Libero software v9.1 or later.
- Supports Windows® and Linux operating systems.

Installation Instructions

The CoreCORDIC CPZ file must be installed into the Libero software. This is done automatically through the Catalog update function in Libero, or the CPZ file can be added using the **Add Core** catalog feature manually. Once installed in the Libero Catalog, the core can be instantiated and configured.

Refer to the *Using DirectCore in Libero IDE User's Guide* or Libero SoC online help for further instructions on core installation, licensing, and general use.

Documentation

The release contains a copy of the CoreCORDIC Handbook. The handbook describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, as well as implementation suggestions. For more information about Intellectual Property, visit: http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores. For updates and additional information about software, FPGAs, and hardware, visit: http://www.microsemi.com.

Supported Test Environments

CoreCORDIC v4.0 supports the following test environments:

- VHDL user testbench
- Verilog user testbench

Discontinued Features and Devices

Support for bit-serial CORDIC implementation is discontinued in the CoreCORDIC v4.0 release.

New Features and Devices

CoreCORDIC v4.0 has the following new features and devices:

- Coarse rotation was added to cover the full circle range of in and out vectors
- Selection of four output rounding modes
- Automatic selection of internal CORDIC engine data path widths

Release History

Table 1 shows the release history of this document.

Table 1. CoreCORDIC Release History

Version	Date	Changes
4.0	May 2015	As listed in Table 2 below
3.0	May 2010	As listed in Table 3 below.
2.0	April 2006	Initial release.

Resolved Issues in the v4.0 Release

Table 2 shows SARs resolved in the CoreCORDIC v4.0 release.

Table 2. Resolved SARs in CoreCORDIC v4.0

SAR No.	Description
26547	Provide support for the core to follow SmartDesign flow.
29075	Eliminate synthesis failure due to RTL parameter mismatch.
34711	Expose only valid core ports to a user.
34712	Simplify the core use flow.
35321, 34940	Prevent a possible mismatch between RTL module parameters/entity generics.
43062, 50809	Provide better user interface to avoid user's confusion.
34658	Connect synchronous reset line to all CORDIC registers.
55916	Extend CORDIC support to cover recently emerged FPGA families.
57144	Support for negative input X values.

Resolved Issues in the v3.0 Release

Table 3 shows SARs resolved in the CoreCORDIC v3.0 release.

Table 3. Resolved SARs in CoreCORDIC v3.0

SAR	Description
13497	Generated core does not seem to match up with the datasheet pin descriptions.
19458	CoreCORDIC for Verilog requires Package Directory.
19459	Remove package directory dependency for VHDL.
20132	CoreCORDIC in Word Serial mode has RTL and Doc mismatches.

Known Limitations and Workarounds

There are no known limitations or workarounds in the CoreCORDIC v4.0 release.

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