CoreAPBLSRAM v3.0 Release Notes

This document is the production release notes of CoreAPBLSRAM v3.0 IP core. It describes the features, system requirements, supported families, implementations, known issues, and workarounds.

Key Features

CoreAPBLSRAM supports the following features:

- Configurable memory sizes
- Configurable parameter to access either LSRAM or uSRAM
- Merge multiple SRAM blocks to form large SRAMs or uSRAMs
- APB3 interface for 8, 16, or 32 bits

Delivery Types

CoreAPBLSRAM is licensed as RTL. Complete RTL source code is provided for the core and testbenches.

Supported Families

- SmartFusion®2
- IGLOO®2

Supported Tool Flows

This version must be used with Libero SoC v11.0 or later.

Installation Instructions

Within the Libero SoC software, click **Add Core** in the Catalog to locate and install a local CPZ file, or use the automatic web update feature in Libero SoC. After the CPZ file is installed in the Libero SoC, the core can be instantiated, configured, and generated within SmartDesign for inclusion in the Libero SoC project.

For the RTL version of the core, the FlexLM license must be installed before exporting the core. For more information about core installation, licensing, and general use, refer to the *Libero SoC Online Help*.

Documentation

For more information about Microsemi Intellectual Property, visit *http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores*. For updates and additional information about Microsemi software, FPGAs, and hardware, visit *http://www.microsemi.com*.

Supported Test Environments

- Verilog user testbench
- VHDL user testbench

Release History

Table 1 shows the release history of CoreAPBLSRAM v3.0.

Table 1 Release History

Version	Date	Changes
3.0	November 2015	As listed in Table 2.
2.0	October 2012	Initial release.

Resolved Issues in the v3.0 Release

Table 2 shows the list of SARs resolved in the v3.0 release.

Table 2 Resolved SARs

SAR	Description
43496	Missing modules in Libero Design Hierarchy > Components view
43497	RTL license option presented even when no RTL license available
57579	CoreAPBLSRAM: Doc improvement
71059	CoreAPBLSRAM only supports 8-bit (sequential) addressing

Discontinued Features and Devices

APB_DWIDTH = 24 is no longer supported.

Known Limitations and Workarounds

There are no known limitations and workarounds.

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