CoreAPBLSRAM v3.0

Handbook

Microsemi

Revision History

Date	Revision	Change
November 2015	1	Second release
November 2012	0	Initial release

Confidentiality Status

This is a non-confidential document.

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Preface

About this Document

This handbook describes the CoreAPBLSRAM DirectCore module and how to use it.

Intended Audience

FPGA designers using Libero® System-on-Chip (SoC).

Introduction

General Description

The CoreAPBLSRAM provides access to the embedded large SRAM (LSRAM) and small SRAM (uSRAM) blocks present on the SmartFusion®2 system-on-chip (SoC) field programmable gate array (FPGA) family devices through APB slave interface. It facilitates convenient access to SRAM by APB masters such as CoreABC. The core can logically group a number of SRAM blocks into a single large SRAM block.

Various configuration parameters or generics apply to CoreAPBLSRAM to control the amount of memory which it provides access to, and the data width of the core.

Core Version

This handbook applies to CoreAPBLSRAM version 3.0.

Supported Families

- SmartFusion®2
- IGLOO®2

Utilization and Performance

Table 1 shows the utilization and performance data for the SmartFusion2 (M2S050) and IGLOO®2 device families. The data listed in this table is indicative only. The overall device utilization and performance of the core is system dependent.

Table 1 Device Utilization and Performance

Family	APB Data Width	SRAM Type	LSRAM Depth	uSRAM Depth	Logic Elements				Frequency (MHz)
					Sequential	Combinational	Total	Percentage	
SmartFusion2	32	LSRAM	2048	128	176	179	355	.315	274.6
SmartFusion2	16	uSRAM	2048	1280	739	759	1498	1.33	291.2
SmartFusion2	8	uSRAM	2048	9216	2604	2663	5267	4.675	213.1
IGLOO2	32	uSRAM	2048	1408	1620	1720	3340	2.965	313.0
IGLOO2	16	LSRAM	21504	128	777	828	1605	1.425	220.0
IGLOO2	8	LSRAM	21504	128	2499	2594	5093	4.52	162.9

- *The data in this table is achieved using typical synthesis and layout settings. Frequency (in MHz) was set to 100 and speed grade was STD.*

Functional Block Description

The CoreAPBLSRAM consists three major functional blocks: APB slave interface logic, data and address handling control logic, and SRAM block instances, as shown in Figure 1.

The IP core selects either the LSRAM or uSRAM based on the user configurable parameter 'SEL_RAM_TYPE'.

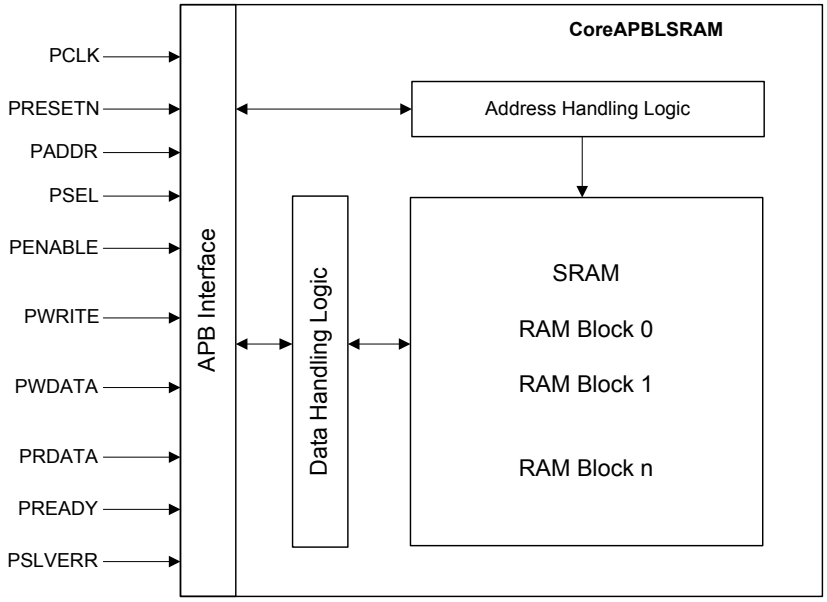

Figure 1 CoreAPBLSRAM Block Diagram

SRAM Block

The core provides configurable parameter to select either LSRAM or uSRAM based on the configurable parameter 'SEL_SRAM_TYPE'.

The SRAM memory begins at address offset 0x0000 and continues to an upper limit, which depends on the configuration of the core.

The minimum number of memory locations for LSRAM of APB_DWIDTH = 32, 16, and 8 are 512, 1024, and 2048. Multiple LSRAMs merge to form a large LSRAM. The maximum number of possible memory locations for APB_DWIDTH = 32, 16, and 8 are 34.5k, 69k, and 138k in steps of 512, 1024, and 2048 locations.

The minimum number of memory locations for uSRAM of APB_DWIDTH = 32, 16, and 8 are 64, 64, and 128. Multiple uSRAMs merge to form a large uSRAM. The maximum number of possible memory locations for APB_DWIDTH = 32, 16, and 8 are 2.3k, 4.5k, and 9k in steps of 64, 64, and 128 locations.

The APB data width is configurable for 8, 16, and 32.

Operation

Data and Address Handling Control Logic

The control logic block converts the APB read/write transactions into the corresponding transactions on the LSRAM/uSRAM memory block.

The Large SRAM memory size can be configured from 512 to 35328 word locations in steps of 512 for APB data width of 32 bits, 1024 to 70656 half word locations in steps of 1024 for APB data width of 16 bits, and 2048 to 141312 byte locations in steps of 2048 for APB data width of 8 bits.

The uSRAM memory size can be configured from 64 to 2304 word locations in steps of 32 for APB data width of 32 bits, 64 to 4608 half word locations in steps of 64 for APB data width of 16 bits, and 128 to 9216 byte locations in steps of 128 for data width of 8 bits.

Addressing scheme followed for LSRAM/uSRAM memory block:

For APB data width of 32 bits, the addresses are word aligned, that is, 0x00, 0x04, 0x08, and so on.

For APB data width of 16 bits, the addresses are half word aligned, that is, 0x00, 0x02, 0x04, and so on.

For APB data width of 8 bits, the addresses are byte aligned, that is, 0x00, 0x01, 0x02, and so on.

Each of these SRAMs contains a system IP interface (SII), which allows access by the System Controller. Also, it supports the BUSY output signal from the RAM macros to provide access to the SII interface. The RAM macro asserts the BUSY signal, if the SII interface requests for access to the RAM macros. If any APB transaction is in progress, it is allowed to complete successfully. The PREADY signal is pulled low, thereby preventing any further transactions on the APB bus. When the BUSY signal is deasserted again, the APB bus transactions continue normally.

Interface Description

Table 2 shows the signal descriptions for CoreAPBLSRAM.

Table 2 CoreAPBLSRAM I/O Signals

Name	Direction	Description
APB Bus Signals		
PCLK	Input	APB System Clock – Reference clock for all internal logic
PRESETN	Input	APB active low asynchronous reset
PWDATA [APB_DWIDTH-1:0]	Input	APB write data
PRDATA [APB_DWIDTH-1:0]	Output	APB read data
PADDR [19:0]	Input	APB address bus
PENABLE	Input	APB strobe – Indicates the second cycle of an APB transfer.
PSEL	Input	APB slave select
PWRITE	Input	APB write/read select signal
PREADY	Output	APB 3 ready signal for future APB 3 compliance. It is used to extend APB transfer.
PSLVERR	Output	APB Slave Error. This signal indicates transfer failure. It is tied to LOW.

Core Parameters

CoreAPBLSRAM Configurable Options

There are a number of configurable options that apply to CoreAPBLSRAM, as shown in Table 3. If a configuration other than the default is required, the configuration dialog box in the SmartDesign used to select appropriate values for the configurable options.

Table 3 CoreAPBLSRAM Configuration Options

Name	Valid Range	Description
FAMILY	19,24	Must be set to the required FPGA family. 19: SmartFusion. 24: IGLOO2
APB_DWIDTH	8, 16, 32	APB data width. Controls the data width of each memory location.
LSRAM_NUM_LOCATIONS_DWIDTH	512–35328 for APB_DWIDTH = 32 1024–70656 for APB_DWIDTH = 16 2048–141312 for APB_DWIDTH = 8	Number of memory locations when APB_DWIDTH = 32. 0.5k, 1k, 2.5k,.....,34.5k (1k = 1024 location) **Note:** The steps size are in steps of .5k, ranging from .5k to 34.5k

		Number of memory locations when APB_DWIDTH = 16. 1k, 2k,.....69k (1k = 1024 location) **Note:** The steps size are in steps of 1k, ranging from 1k to 69k Number of memory locations when APB_DWIDTH = 08. 2k,4k,6k.....138k (1k = 1024 location) **Note:** The steps size are in steps of 2k, ranging from 2k to 138k **Note:** This **is** valid only for LSRAM memory configuration.
USRAM_NUM_LOCATIONS_ DWIDTH	64–2304 for APB_DWIDTH = 32 64–4608 for APB_DWIDTH = 16 128–9216 for APB_DWIDTH = 8	Number of memory locations when APB_DWIDTH = 32. 64,128,192…….2.3k **Note:** The steps size are in steps of 64, ranging from 64 to 2.3k Number of memory locations when APB_DWIDTH = 16. 64, 128,192,.....4.5k **Note:** The steps size are in steps of 64, ranging from 64 to 4.5k Number of memory locations when APB_DWIDTH = 08. 128,256,384.....9k **Note:** The steps size are in steps of 128, ranging from 128 to 9k **Note:** This is valid only for uSRAM memory configuration.
SEL_SRAM_TYPE	0 or 1	0 – Select LSRAM(RAM1Kx18) memory 1 – Select uSRAM(RAM64x18) memory

Timing Diagrams

APB Interface

The core implements standard APB3 slave interface to provide access to embedded SRAMs. Read and write accesses on the APB slave interface get converted into corresponding transfers on the LSRAM or uSRAM. APB write and read transfers are shown in Figure 2 and Figure 3.

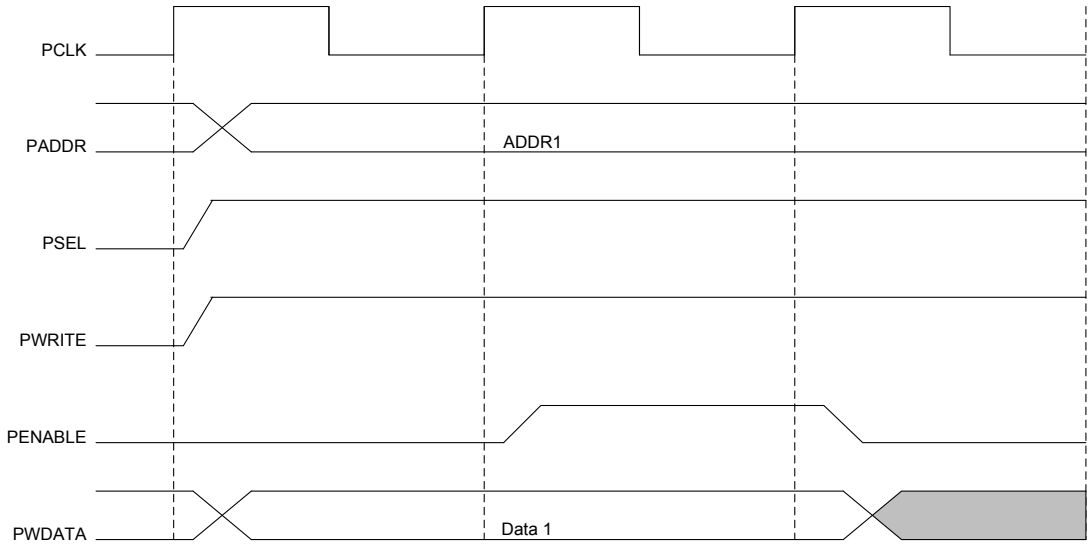

Figure 2 APB Write Transfer

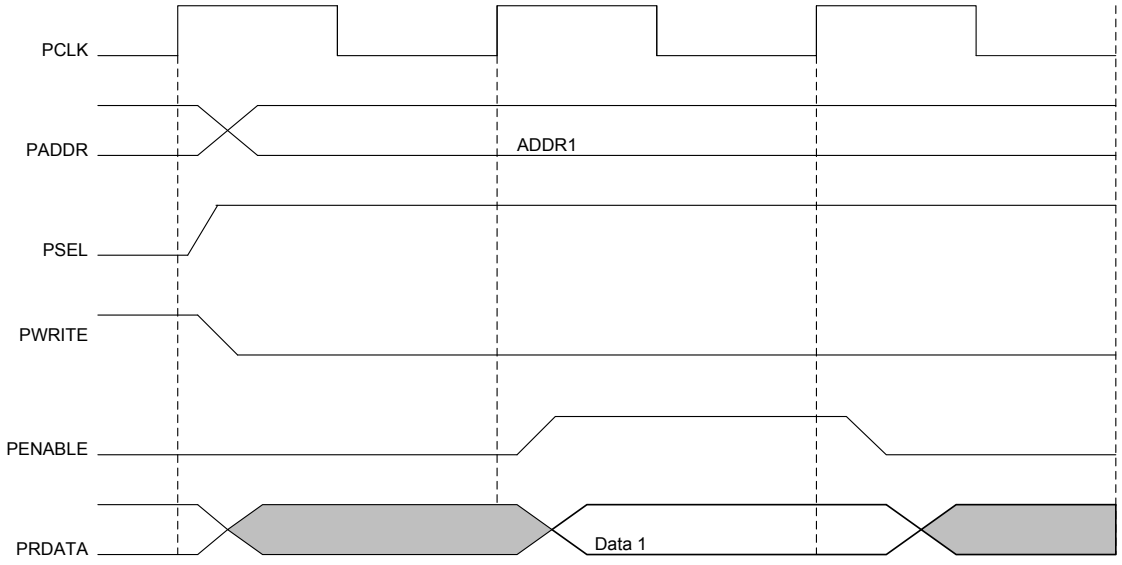

Figure 3 APB Read Transfer

Note: The above transfers consider PREADY as always asserted.

Tool Flows

Licensing

CoreAPBLSRAM is licensed as RTL. Depending on your license tool flow, functionality may be limited. Complete RTL source code is provided for the core and testbenches.

SmartDesign

CoreAPBLSRAM is preinstalled in the SmartDesign IP deployment design environment. An example instantiated view is shown in Figure 4. The core can be configured using the configuration GUI within SmartDesign, as shown in Figure 5.

For information on using SmartDesign to instantiate and generate cores, refer to the *Using DirectCore in Libero® SoC User's Guide*.

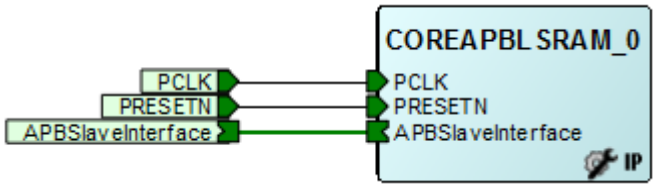

Figure 4 SmartDesign CoreAPBLSRAM Instance View

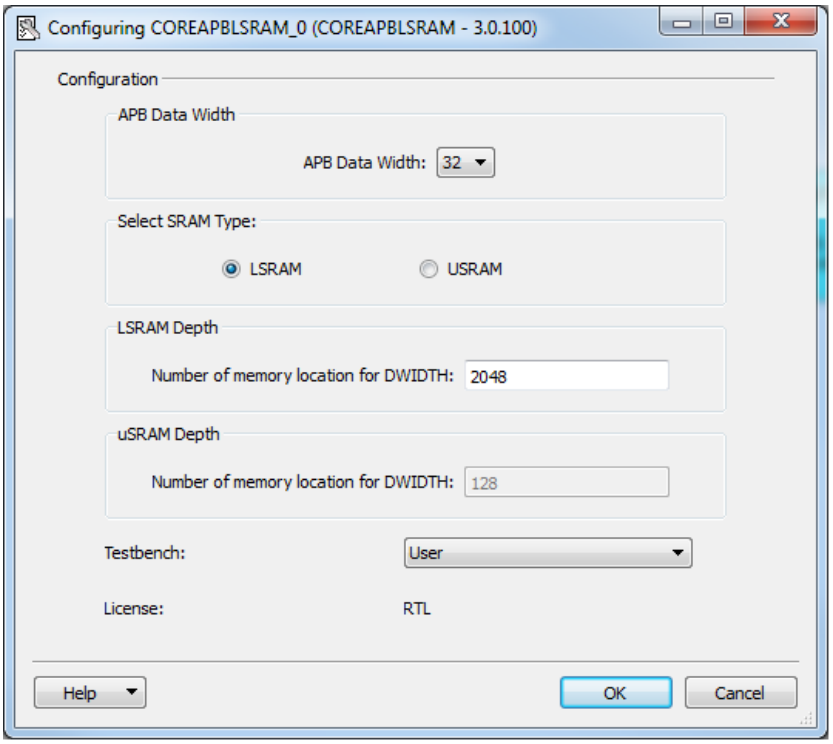

Figure 5 SmartDesign CoreAPBLSRAM Configuration Window

Simulation Flows

The user testbench for CoreAPBLSRAM is included in all releases.

To run simulations, select the **User Testbench** flow within SmartDesign and click **Save & Generate** on the Generate pane. The **User Testbench** is selected through the Core Testbench Configuration GUI.

When SmartDesign generates the Libero SoC project, it installs the user testbench files.

To run the **User Testbench**, set the design root to the CoreAPBLSRAM instantiation in the Libero SoC design hierarchy pane and click the **Simulation** icon on the Libero SoC design flow window. This invokes ModelSim® and automatically runs the simulation.

Synthesis in Libero SoC

Click the **Synthesis** icon in Libero SoC. The Synthesis window appears, displaying the Synplicity® project. Set Synplicity to use the Verilog 2001 standard, if Verilog is being used. To run synthesis, select the **Run** icon.

Place-and-Route in Libero SoC

Click the **Layout** icon in the Libero SoC to invoke Designer. CoreAPBLSRAM requires no special place-and-route settings.

Testbench Operation

An example **User Testbench** is included with CoreAPBLSRAM.

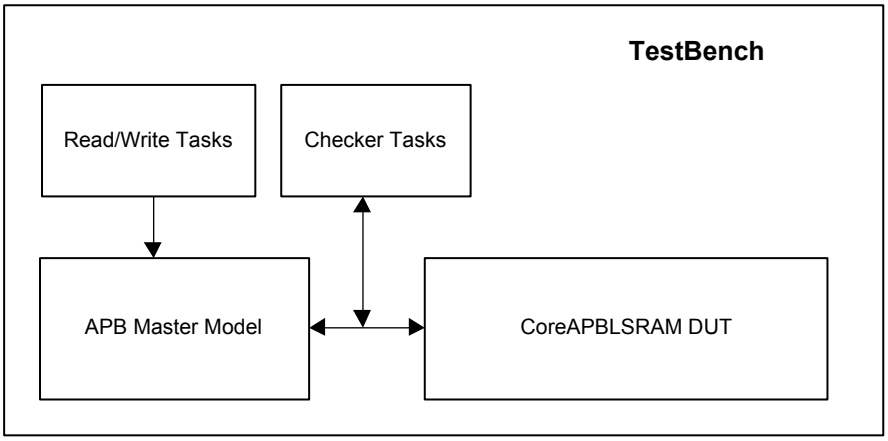

Figure 6 User Testbench

As shown in Figure 6, the User Testbench instantiates a Microsemi® DirectCore CoreAPBLSRAM design-under-test (DUT). The APBLSRAM master model tasks drives write/read transactions to the DUT. The DUT, in turn performs write and read to the SRAM memories, which are instantiated inside the DUT. The checker model tasks check and determine whether the transaction is successful or not and displays the result.

Register Map and Descriptions

CoreAPBLSRAM does not contain any registers.

Ordering Information

Ordering Codes

CoreAPBLSRAM can be ordered through the local sales representative. It must be ordered using the following number scheme: CoreAPBLSRAM-XX, where XX is listed in Table 4.

Table 4 Ordering Codes

XX	Description
RM	RTL for RTL source—multiple use license

List of Changes

The following table shows important changes made in this document for each revision.

Date	Change	Page
November 2015	SAR fixes.	N/A
April 2012	Initial handbook version	N/A

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From the rest of the world, call **650.318.4460**
Fax, from anywhere in the world **408.643.6913**

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Website

You can browse a variety of technical and non-technical information on the Microsemi SoC Products Group home page, at http://www.microsemi.com/products/fpga-soc/fpga-and-soc.

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