CN20016: RT PolarFire Pin Assignment Change

September 10, 2020

Description

This is a Customer Advisory Notification. DDR3 and DDR4 pin assignments of the RTPF500T-CG1509 package have been altered in Libero SoC v12.5. Place and route performed with Libero SoC v12.4 will be invalidated when Libero SoC v12.5 is invoked.

Reason for Change

The change has been made to optimize PCB layout and signal integrity of DDR signals.

Application Impact

Any PCB layout done from a pinout generated in Libero SoC v12.4 will need to change all DDR3 and DDR4 I/Os. These changes will not affect any other I/O assignment.

Action Required

No action is required for RT PolarFire FPGA designs that were started using Libero SoC v12.5 or later releases. The pin assignment change applies only to designs that were started in Libero SoC v12.4.

Action is required for any RTPF500T-CG1509 design developed with Libero SoC v12.4. Open the project in Libero SoC v12.5 or later and rerun P&R. Any DDR assignments in an existing pdc constraints file must be discarded and re-entered through the I/O Editor. Designers should consult the latest version of the RT PolarFire pin assignment table, which is posted on the Microsemi web at *https://www.microsemi.com/document-portal/doc_download/1245009-cg1509-package-pin-assignment-table*.

Products Affected

This change applies only to any RT PolarFire FPGA design that was started using Libero SoC v12.4.

RTPF500T-CG1509

Contact Information

If you have any questions about this subject, contact Microsemi Technical Support department by using the support portal at *https://soc.microsemi.com/Portal/Default.aspx*

Regards,

Microsemi Corporation

Any projected dates in this notification are based on the most current product information at the time this notification is being issued, but they may change due to unforeseen circumstances. For the latest schedule and any other information, please contact your local Microsemi Sales Office, the factory contact shown above, or your local distributor.

Microsemi

2355 W. Chandler Blvd.
Chandler, AZ 85224 USA

Within the USA: +1 (480) 792-7200
Fax: +1 (480) 792-7277

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