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Introduction

Core Overview

CoreAHBtoAPB3 is made up of an advanced high-performance bus (AHB™) slave and advanced microcontroller bus architecture (AMBA®) 3 advanced peripheral bus (APB) master. The CoreAHBtoAPB3 works as a bridge between the AHB and the APB domains. CoreAHBtoAPB3 interfaces with CoreAHB or CoreAHBLite through its AHB interface and with CoreAPB3 through its APB interface. Figure 1 shows an overview of CoreAHBtoAPB3.

Key Features

- Bridges between AHB/AHB-Lite and APB buses
- Connects automatically to CoreAHB/CoreAHBLite and CoreAPB3 in SmartDesign when Auto Connect feature is used
- Compliant with AMBA 3 APB

Supported Microsemi® FPGA Families

The CoreAHBtoAPB3 v3.1 supports the following families:

- SmartFusion®2
- SmartFusion®
- Microsemi Fusion®
- IGLOO®, IGLOO®e, IGLOO PLUS
- ProASIC®3, ProASIC®3E, ProASIC®3L
- ProASIC®PLUS®
- Axcelerator®
- RTAX-S
- IGLOO®2
- RTG4™
Core Version

This handbook supports CoreAHBtoAPB3 version 3.1.

Supported Interfaces

CoreAHBtoAPB3 supports an AHB or AHB-Lite slave interface connected to an AHB or AHB-Lite mirrored slave interface (as found on, for example, CoreAHB or CoreAHBLite), as well as an AMBA 3 APB master interface that connects to an AMBA 3 APB mirrored master interface (as found on, for example, CoreAPB3).

Utilization and Performance

Utilization and performance data for CoreAHBtoAPB3 is given in Table 1.

**Table 1** CoreAHBtoAPB3 Device Utilization and Performance

<table>
<thead>
<tr>
<th>Family</th>
<th>Tiles</th>
<th>Sequential</th>
<th>Combinatorial</th>
<th>Total</th>
<th>Utilization</th>
<th>Performance (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fusion</td>
<td>126</td>
<td>75</td>
<td>201</td>
<td></td>
<td>M1AFS1500</td>
<td>1% 128</td>
</tr>
<tr>
<td>IGLOO</td>
<td>126</td>
<td>80</td>
<td>206</td>
<td></td>
<td>M1AGL1000V2</td>
<td>1% 75</td>
</tr>
<tr>
<td>ProASIC3</td>
<td>126</td>
<td>72</td>
<td>198</td>
<td></td>
<td>M1A3P600</td>
<td>1% 134</td>
</tr>
<tr>
<td>ProASIC</td>
<td>128</td>
<td>192</td>
<td>320</td>
<td></td>
<td>APA600</td>
<td>1% 80</td>
</tr>
<tr>
<td>Accelerator</td>
<td>127</td>
<td>72</td>
<td>199</td>
<td></td>
<td>AX500</td>
<td>2% 145</td>
</tr>
<tr>
<td>RTAX-S</td>
<td>127</td>
<td>72</td>
<td>199</td>
<td></td>
<td>RTAX1000S</td>
<td>1% 97</td>
</tr>
<tr>
<td>SmartFusion2</td>
<td>141</td>
<td>63</td>
<td>204</td>
<td></td>
<td>M2S150T</td>
<td>0.14 250</td>
</tr>
<tr>
<td>IGLOO2</td>
<td>141</td>
<td>63</td>
<td>204</td>
<td></td>
<td>M2GL150T</td>
<td>0.14 250</td>
</tr>
<tr>
<td>RTG4</td>
<td>143</td>
<td>78</td>
<td>221</td>
<td></td>
<td>RT4G150</td>
<td>0.14 242</td>
</tr>
</tbody>
</table>

*Note: Data in this table was gathered based on typical synthesis and layout settings.*
Ports

The ports present on CoreAHBtoAPB3 are listed in Table 2.

Table 2 CoreAHBtoAPB3 Ports

<table>
<thead>
<tr>
<th>Port Name</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>HRESETN</td>
<td>Input</td>
<td>AHB reset, active low asynchronous reset</td>
</tr>
<tr>
<td>HCLK</td>
<td>Input</td>
<td>AHB clock signal</td>
</tr>
<tr>
<td>HSEL</td>
<td>Input</td>
<td>AHB slave select</td>
</tr>
<tr>
<td>HWRITE</td>
<td>Input</td>
<td>APB write indication</td>
</tr>
<tr>
<td>HREADY</td>
<td>Input</td>
<td>AHB ready input</td>
</tr>
<tr>
<td>HTRANS[1:0]</td>
<td>Input</td>
<td>AHB transfer type:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>00: Idle</td>
</tr>
<tr>
<td></td>
<td></td>
<td>01: Busy</td>
</tr>
<tr>
<td></td>
<td></td>
<td>10: Non-sequential</td>
</tr>
<tr>
<td></td>
<td></td>
<td>11: Sequential</td>
</tr>
<tr>
<td>HADDR[31:0]</td>
<td>Input</td>
<td>AHB address bus</td>
</tr>
<tr>
<td>HWDATA[31:0]</td>
<td>Input</td>
<td>AHB write data</td>
</tr>
<tr>
<td>HREADYOUT</td>
<td>Output</td>
<td>AHB ready output</td>
</tr>
<tr>
<td>HRDATA[31:0]</td>
<td>Output</td>
<td>AHB read data</td>
</tr>
<tr>
<td>HRESP</td>
<td>Output</td>
<td>AHB transfer response:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>00: Okay</td>
</tr>
<tr>
<td></td>
<td></td>
<td>01: Error</td>
</tr>
<tr>
<td></td>
<td></td>
<td>10: Retry</td>
</tr>
<tr>
<td></td>
<td></td>
<td>11: Split</td>
</tr>
<tr>
<td>PSEL</td>
<td>Output</td>
<td>APB select</td>
</tr>
<tr>
<td>PENABLE</td>
<td>Output</td>
<td>APB enable</td>
</tr>
<tr>
<td>PWRITE</td>
<td>Output</td>
<td>APB write indication</td>
</tr>
<tr>
<td>PADDR[31:0]</td>
<td>Output</td>
<td>APB address bus</td>
</tr>
<tr>
<td>PWDATA[31:0]</td>
<td>Output</td>
<td>APB write data</td>
</tr>
<tr>
<td>PRDATA[31:0]</td>
<td>Input</td>
<td>APB read data</td>
</tr>
<tr>
<td>PREADY</td>
<td>Input</td>
<td>APB ready indication</td>
</tr>
<tr>
<td>PSLVERR</td>
<td>Input</td>
<td>APB slave error indication</td>
</tr>
</tbody>
</table>

Note: All signals in this table are active high unless otherwise stated.
Design Description

CoreAHBtoAPB3 acts like a bridge between an AHB/AHB-Lite bus and an APB bus. Read and write transfers on the AHB bus are converted to corresponding transfers on the APB bus. High bandwidth peripherals, such as memory controllers, are typically connected to the AHB bus, whereas the APB bus is used for less demanding peripherals such as general purpose Input/Output (GPIO). Unlike the AHB bus, transfers on the APB bus are not pipelined.

AHB Interface Timing

Figure 2 and Figure 3 illustrate the AHB transfer timing. An AHB transfer can be described in terms of an address phase and a data phase. The data relevant to the address of interest follows in the clock cycle(s) after the address. The data phase can extend over a number of cycles if the HREADY signal is held low. Figure 2 shows a basic AHB transfer with no wait states as HREADY is high during the transfer. Figure 3 shows an AHB transfer with one wait state. HREADY is low for one cycle during the data phase in the waited transfer.

![Figure 2 Basic AHB Transfer](image)

![Figure 3 AHB Transfer with One Wait State](image)
Figure 4 and Figure 5 show the timing of APB write and read transfers with no wait states. Figure 6 and Figure 7 show APB write and read transfers with one wait state.

---

**Figure 4 APB Write Transfer, No Wait States**

**Figure 5 APB Read Transfer, No Wait States**

**Figure 6 APB Write Transfer with One State**
<table>
<thead>
<tr>
<th>Signal</th>
<th>Timing</th>
<th>Action</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCLK</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PADDR</td>
<td></td>
<td>read addr</td>
</tr>
<tr>
<td>PWRITE</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PSEL</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PENABLE</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PWDATA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PRDATA</td>
<td></td>
<td>read data</td>
</tr>
<tr>
<td>PREady</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Figure 7** APB Read Transfer with One State
Licensing

CoreAHBtoAPB3 is licensed in two ways, Obfuscated or register transfer level (RTL).

Obfuscated

Complete RTL code is provided for the core, allowing the core to be instantiated with SmartDesign. Simulation, synthesis, and layout can be performed within Libero® System-on-Chip (SoC). The RTL code for the core is obfuscated and some of the testbench source files are not provided; instead, they are precompiled into the compiled simulation library.

RTL

Complete RTL source code is provided for the core and testbenches.

SmartDesign

CoreAHBtoAPB3 is available for downloading to the SmartDesign IP Catalog through the Libero SoC web repository. For information on using SmartDesign to instantiate, configure, connect, and generate cores, refer to the Libero SoC online help.

The only configuration option available for CoreAHBtoAPB3 allows you to choose whether or not to create a testbench for CoreAHBtoAPB3 when generating a design including CoreAHBtoAPB3 from SmartDesign. Figure 8 shows the configuration GUI for CoreAHBtoAPB3. Figure 9 shows how the symbol for CoreAHBtoAPB3 appears on the SmartDesign canvas. The AHB and APB signals are grouped into interfaces that appear on the top and bottom of the symbol.
Simulation Flows

The user testbench for CoreAHBtoAPB3 is included in all releases of the core. To run simulations, set the testbench configuration option for CoreAHBtoAPB3 to user before generating your design in SmartDesign. To run the user testbench, set the design root to the CoreAHBtoAPB3 instance in the Libero SoC Design Hierarchy pane and double-click the Simulate command in the Design Flow pane. You can also right-click on Simulate and choose, for example, “Run” or “Open Interactively”. ModelSim is invoked and the simulation runs automatically.

User Testbench

Figure 10 shows the simulation environment that includes instantiation of CoreAHBtoAPB3, an AHB-Lite master bus functional model (BFM), and an APB slave. The AHB-Lite BFM drives the testbench and is itself controlled by the commands in an automatically generated script file. This script file has a “.bfm” extension and is a plain text file that can be modified. Refer to the DirectCore AMBA BFM User’s Guide for more information.
Synthesis in Libero SoC

Having set the design root to the CoreAHBtoAPB3 instance, double-click (or right click and choose an option) the Synthesize command in the Design Flow pane in Libero SoC. The Synplicity synthesis tool will be invoked. Set Synplicity to use the verilog 2001 standard if a verilog flow is being used. To run synthesis, click Run.

Place and Route in Libero SoC

Having set the design root appropriately and after running synthesis, use the Compile command followed by the Place and Route command in the Design Flow pane in Libero SoC to place and route the core.
Ordering Information

Ordering Codes

CoreAHBtoAPB3 can be ordered through your local Sales Representative. It should be ordered using the following number scheme: CoreAHBtoAPB3-XX, where XX is listed in Table 3.

<table>
<thead>
<tr>
<th>XX</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>OM</td>
<td>RTL for Obfuscated RTL—multiple use license</td>
</tr>
<tr>
<td>RM</td>
<td>RTL for RTL source—multiple-use license</td>
</tr>
</tbody>
</table>
### List of Changes

The following table lists critical changes that were made in each revision of the document.

<table>
<thead>
<tr>
<th>Date</th>
<th>Change</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>Revision 2 (November 2014)</td>
<td>Updated to correspond with v4.1 of CoreAPB3.</td>
<td>N/A</td>
</tr>
<tr>
<td>Revision 1 (February 2013)</td>
<td>Updated to suit v3.0 of CoreAHBtoAPB3</td>
<td>N/A</td>
</tr>
</tbody>
</table>
Microsemi SoC Products Group backs its products with various support services, including Customer Service, Customer Technical Support Center, a website, electronic mail, and worldwide sales offices. This appendix contains information about contacting Microsemi SoC Products Group and using these support services.

Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From North America, call **800.262.1060**
From the rest of the world, call **650.318.4460**
Fax, from anywhere in the world **650.318.8044**

Customer Technical Support Center

Microsemi SoC Products Group staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions about Microsemi SoC Products. The Customer Technical Support Center spends a great deal of time creating application notes, answers to common design cycle questions, documentation of known issues and various FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Technical Support

Visit the Microsemi SoC Products Group Customer Support website for more information and support (http://www.microsemi.com/soc/support/search/default.aspx). Many answers available on the searchable web resource include diagrams, illustrations, and links to other resources on website.

Website

You can browse a variety of technical and non-technical information on the Microsemi SoC Products Group home page, at http://www.microsemi.com/soc/.

Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center. The Technical Support Center can be contacted by email or through the Microsemi SoC Products Group website.

Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is soc_tech@microsemi.com.

My Cases

Microsemi SoC Products Group customers may submit and track technical cases online by going to My Cases.
Outside the U.S.
Customers needing assistance outside the US time zones can either contact technical support via email (soc_tech@microsemi.com) or contact a local sales office. Sales office listings can be found at www.microsemi.com/soc/company/contact/default.aspx.

ITAR Technical Support
For technical support on RH and RT FPGAs that are regulated by International Traffic in Arms Regulations (ITAR), contact us via soc_tech_itar@microsemi.com. Alternatively, within My Cases, select Yes in the ITAR drop-down list. For a complete list of ITAR-regulated Microsemi FPGAs, visit the ITAR web page.
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