CoreAHBtoAPB3 v3.1

Handbook

Microsemi

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Introduction

Core Overview

CoreAHBtoAPB3 is made up of an advanced high-performance bus (AHB™) slave and advanced microcontroller bus architecture (AMBA®) 3 advanced peripheral bus (APB) master. The CoreAHBtoAPB3 works as a bridge in between the AHB and the APB domains. CoreAHBtoAPB3 interfaces with CoreAHB or CoreAHBLite through its AHB interface and with CoreAPB3 through its APB interface. Figure 1 shows an overview of CoreAHBtoAPB3.

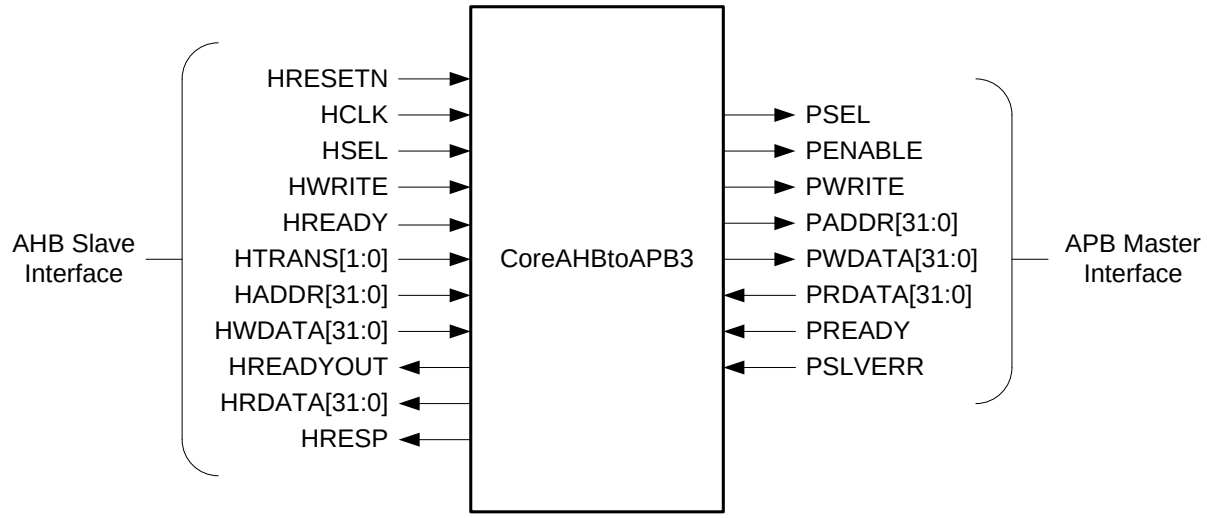

Figure 1 CoreAHBtoAPB3 Overview

Key Features

- Bridges between AHB/AHB-Lite and APB buses
- Connects automatically to CoreAHB/CoreAHBLite and CoreAPB3 in SmartDesign when Auto Connect feature is used
- Compliant with AMBA 3 APB

Supported Microsemi® FPGA Families

The CoreAHBtoAPB3 v3.1 supports the following families:

- SmartFusion®2
- SmartFusion®
- Microsemi Fusion®
- IGLOO®, IGLOO®e, IGLOO PLUS
- ProASIC®3, ProASIC®3E, ProASIC®3L
- ProASIC PLUS®
- Axcelerator®
- RTAX-S
- IGLOO®2
- RTG4™

Core Version

This handbook supports CoreAHBtoAPB3 version 3.1.

Supported Interfaces

CoreAHBtoAPB3 supports an AHB or AHB-Lite slave interface connected to an AHB or AHB-Lite mirrored slave interface (as found on, for example, CoreAHB or CoreAHBLite), as well as an AMBA 3 APB master interface that connects to an AMBA 3 APB mirrored master interface (as found on, for example, CoreAPB3).

Utilization and Performance

Utilization and performance data for CoreAHBtoAPB3 is given in Table 1.

Table 1 CoreAHBtoAPB3 Device Utilization and Performance

Family	Tiles			Utilization		Performance (MHz)
	Sequential	Combinatorial	Total	Device	%	
Fusion	126	75	201	M1AFS1500	1%	128
IGLOO	126	80	206	M1AGL1000V2	1%	75
ProASIC3	126	72	198	M1A3P600	1%	134
ProASIC	128	192	320	APA600	1%	80
Axcelerator	127	72	199	AX500	2%	145
RTAX-S	127	72	199	RTAX1000S	1%	97
SmartFusion2	141	63	204	M2S150T	0.14	250
IGLOO2	141	63	204	M2GL150T	0.14	250
RTG4	143	78	221	RT4G150	0.14	242

Note: Data in this table was gathered based on typical synthesis and layout settings.

Interface Description

Ports

The ports present on CoreAHBtoAPB3 are listed in Table 2.

Table 2 CoreAHBtoAPB3 Ports

Port Name	Type	Description
HRESETN	Input	AHB reset, active low asynchronous reset
HCLK	Input	AHB clock signal
HSEL	Input	AHB slave select
HWRITE	Input	APB write indication
HREADY	Input	AHB ready input
HTRANS[1:0]	Input	AHB transfer type: 00: Idle 01: Busy 10: Non-sequential 11: Sequential
HADDR[31:0]	Input	AHB address bus
HWDATA[31:0]	Input	AHB write data
HREADYOUT	Output	AHB ready output
HRDATA[31:0]	Output	AHB read data
HRESP	Output	AHB transfer response: 00: Okay 01: Error 10: Retry 11: Split
PSEL	Output	APB select
PENABLE	Output	APB enable
PWRITE	Output	APB write indication
PADDR[31:0]	Output	APB address bus
PWDATA[31:0]	Output	APB write data
PRDATA[31:0]	Input	APB read data
PREADY	Input	APB ready indication
PSLVERR	Input	APB slave error indication

Note: All signals in this table are active high unless otherwise stated.

Design Description

CoreAHBtoAPB3 acts like a bridge between an AHB/AHB-Lite bus and an APB bus. Read and write transfers on the AHB bus are converted to corresponding transfers on the APB bus. High bandwidth peripherals, such as memory controllers, are typically connected to the AHB bus, whereas the APB bus is used for less demanding peripherals such as general purpose Input/Output (GPIO). Unlike the AHB bus, transfers on the APB bus are not pipelined.

AHB Interface Timing

Figure 2 and Figure 3 illustrate the AHB transfer timing. An AHB transfer can be described in terms of an address phase and a data phase. The data relevant to the address of interest follows in the clock cycle(s) after the address. The data phase can extend over a number of cycles if the HREADY signal is held low. Figure 2 shows a basic AHB transfer with no wait states as HREADY is high during the transfer. Figure 3 shows an AHB transfer with one wait state. HREADY is low for one cycle during the data phase in the waited transfer.

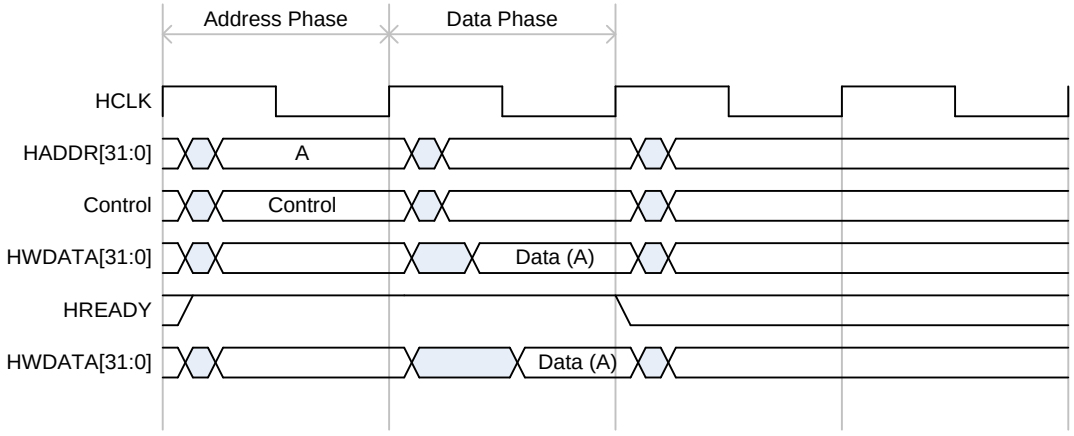

Figure 2 Basic AHB Transfer

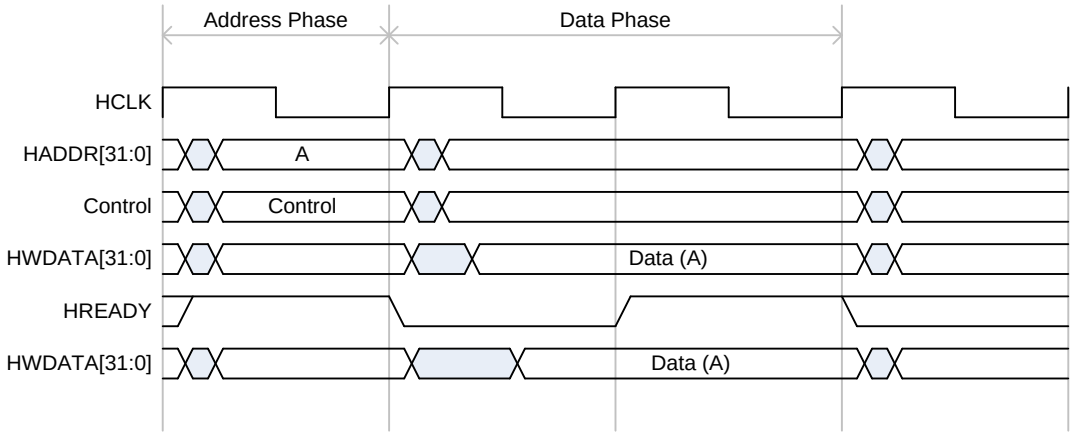

Figure 3 AHB Transfer with One Wait State

APB Interface Timing

Figure 4 and Figure 5 show the timing of APB write and read transfers with no wait states. Figure 6 and Figure 7 show APB write and read transfers with one wait state.

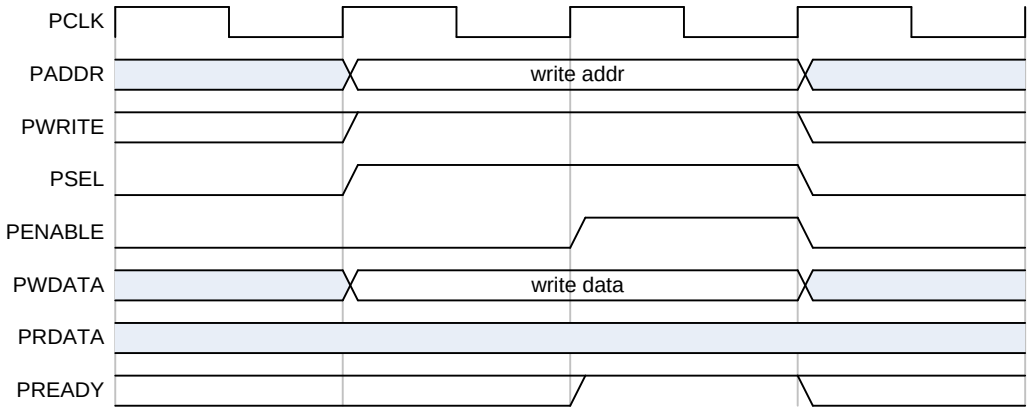

Figure 4 APB Write Transfer, No Wait States

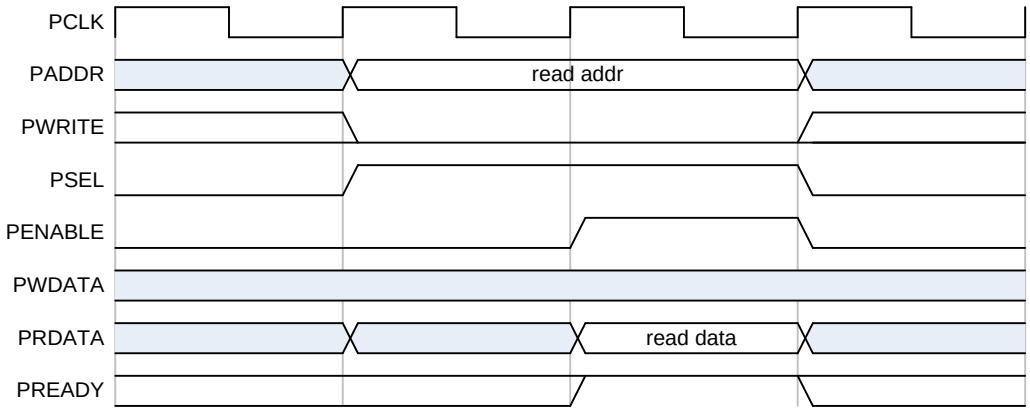

Figure 5 APB Read Transfer, No Wait States

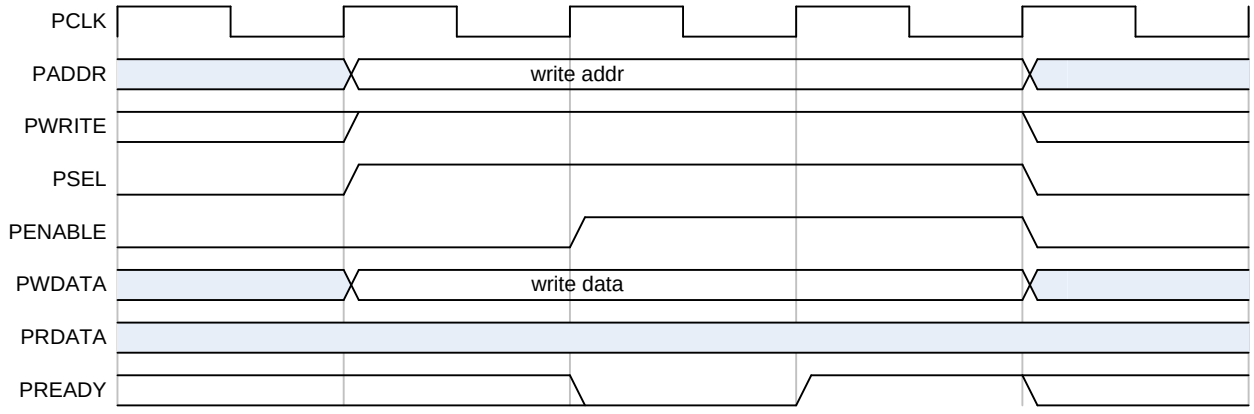

Figure 6 APB Write Transfer with One State

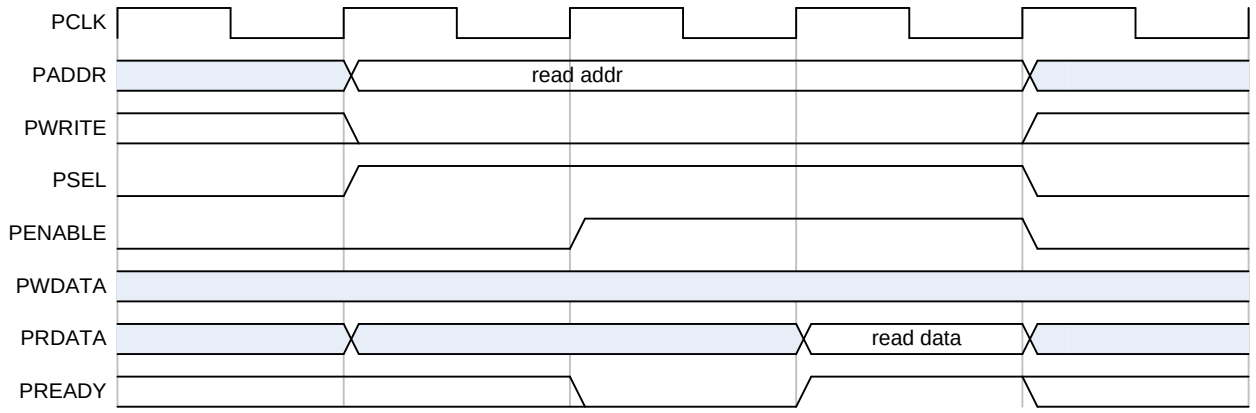

Figure 7 APB Read Transfer with One State

Tool Flows

Licensing

CoreAHBtoAPB3 is licensed in two ways, Obfuscated or register transfer level (RTL).

Obfuscated

Complete RTL code is provided for the core, allowing the core to be instantiated with SmartDesign. Simulation, synthesis, and layout can be performed within Libero® System-on-Chip (SoC). The RTL code for the core is obfuscated and some of the testbench source files are not provided; instead, they are precompiled into the compiled simulation library.

RTL

Complete RTL source code is provided for the core and testbenches.

SmartDesign

CoreAHBtoAPB3 is available for downloading to the SmartDesign IP Catalog through the Libero SoC web repository. For information on using SmartDesign to instantiate, configure, connect, and generate cores, refer to the Libero SoC online help.

The only configuration option available for CoreAHBtoAPB3 allows you to choose whether or not to create a testbench for CoreAHBtoAPB3 when generating a design including CoreAHBtoAPB3 from SmartDesign. Figure 8 shows the configuration GUI for CoreAHBtoAPB3. Figure 9 shows how the symbol for CoreAHBtoAPB3 appears on the SmartDesign canvas. The AHB and APB signals are grouped into interfaces that appear on the top and bottom of the symbol.

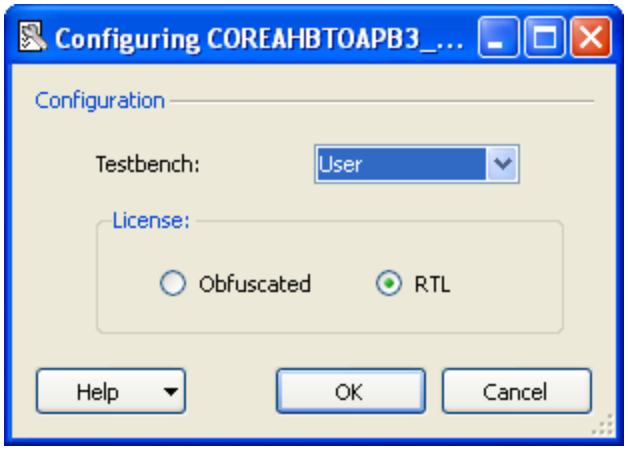

Figure 8 CoreAHBtoAPB3 Configuration GUI

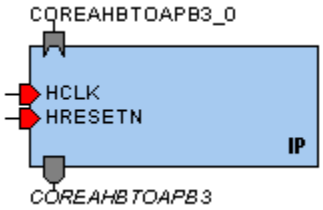

Figure 9 CoreAHBtoAPB3 Symbol

Simulation Flows

The user testbench for CoreAHBtoAPB3 is included in all releases of the core.

To run simulations, set the testbench configuration option for CoreAHBtoAPB3 to user before generating your design in SmartDesign. To run the user testbench, set the design root to the CoreAHBtoAPB3 instance in the Libero SoC Design Hierarchy pane and double-click the **Simulate** command in the Design Flow pane. You can also right-click on **Simulate** and choose, for example, "**Run**" or "**Open Interactively**". ModelSim is invoked and the simulation runs automatically.

User Testbench

Figure 10 shows the simulation environment that includes instantiation of CoreAHBtoAPB3, an AHB-Lite master bus functional model (BFM), and an APB slave. The AHB-Lite BFM drives the testbench and is itself controlled by the commands in an automatically generated script file. This script file has a ".bfm" extension and is a plain text file that can be modified. Refer to the *DirectCore AMBA BFM User's Guide* for more information.

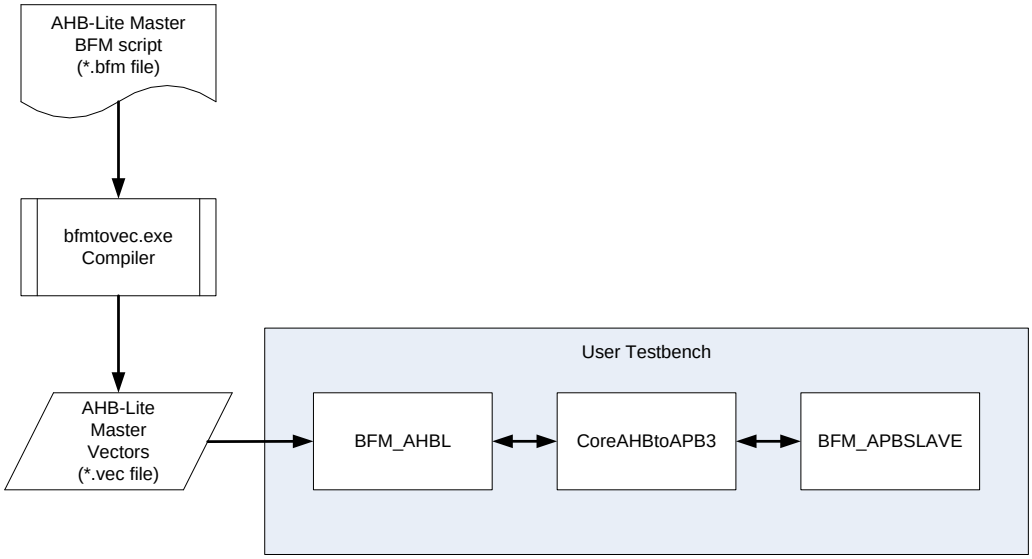

Figure 10 CoreAHBtoAPB3 User Testbench

Synthesis in Libero SoC

Having set the design root to the CoreAHBtoAPB3 instance, double-click (or right click and choose an option) the **Synthesize** command in the Design Flow pane in Libero SoC. The Synplicity synthesis tool will be invoked. Set Synplicity to use the verilog 2001 standard if a verilog flow is being used. To run synthesis, click **Run**.

Place and Route in Libero SoC

Having set the design root appropriately and after running synthesis, use the **Compile** command followed by the Place and Route command in the Design Flow pane in Libero SoC to place and route the core.

Ordering Information

Ordering Codes

CoreAHBtoAPB3 can be ordered through your local Sales Representative. It should be ordered using the following number scheme: CoreAHBtoAPB3-XX, where XX is listed in Table 3.

Table 3 Ordering Codes

XX	Description
OM	RTL for Obfuscated RTL—multiple use license
RM	RTL for RTL source—multiple-use license

List of Changes

The following table lists critical changes that were made in each revision of the document.

Date	Change	Page
Revision 2 (November 2014)	Updated to correspond with v4.1 of CoreAPB3.	N/A
Revision 1 (February 2013)	Updated to suit v3.0 of CoreAHBtoAPB3	N/A

Product Support

Microsemi SoC Products Group backs its products with various support services, including Customer Service, Customer Technical Support Center, a website, electronic mail, and worldwide sales offices. This appendix contains information about contacting Microsemi SoC Products Group and using these support services.

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Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From North America, call **800.262.1060**
From the rest of the world, call **650.318.4460**
Fax, from anywhere in the world **650. 318.8044**

Customer Technical Support Center

Microsemi SoC Products Group staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions about Microsemi SoC Products. The Customer Technical Support Center spends a great deal of time creating application notes, answers to common design cycle questions, documentation of known issues and various FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Technical Support

Visit the Microsemi SoC Products Group Customer Support website for more information and support (http://www.microsemi.com/soc/support/search/default.aspx). Many answers available on the searchable web resource include diagrams, illustrations, and links to other resources on website.

Website

You can browse a variety of technical and non-technical information on the Microsemi SoC Products Group home page, at http://www.microsemi.com/soc/.

Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center. The Technical Support Center can be contacted by email or through the Microsemi SoC Products Group website.

Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is soc_tech@microsemi.com.

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Outside the U.S.

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ITAR Technical Support

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