

V1.0 MSS Configurator (Pre production) Release Notes

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1. Introduction

To provide a seamless experience for both embedded software developers targeting the MSS and the hardware engineers developing a hardware/software solution using the MSS and the FPGA array fabric, the MSS configurator application provides a common tool to configure the PolarFire[™] SoC MSS platform that can be used by both the software engineer and/or the FPGA hardware engineer.

The MSS configurator application can be installed as a stand-alone application or as part of the Libero SoC design tool suite, and provides the following features:

- · Configuration of the MSS clocks
- · Configuration of the MSS interfaces to the FPGA fabric
- Selection and assignment of the MSS peripherals to the MSS dedicated I/Os and/or the FPGA fabric dedicated peripheral interfaces
- · Configuration of the MSS Bank voltages and I/O standards and attributes
- Configuration of the MSS DDR memories (DDR3/L, DDR4, LPDDR3, and LPDDR4)
- · Configuration of the MSS debug features

For details about the high-level MSS architecture and its features, refer to the PolarFire™ SoC product overview.

For details about this tool, refer to the PolarFire SOC Standalone MSS Configuration User Guide.

Download MSS Configurator v1.0 software.

The following are available for download:

- Stand-alone MSS configurator installer (Linux)
- Stand-alone MSS configurator installer (Windows)

Note: Windows installations require administrative privileges.

2. System Requirements

PolarFire SoC MSS Configurator has the following system requirements.

2.1 Supported 64-bit Operating Systems

- Windows 7 or Windows 10 OS
- RHEL 6.6-6.11 and RHEL 7.2-7.6
- CentOS 6.6-6.11 and CentOS 7.2-7.6
- Ubuntu 18.04
- OpenSUSE Leap 42.3 (SLES 12.3 equivalent)

2.2 Random-Access Memory (RAM) Requirements

Minimum of 4 GB RAM

3. References

- · Configuration of the MSS clocks.
 - Refer to the UG0913: PolarFire SoC FPGA Clocking Resources User Guide for detailed information about the MSS clocking features.
- · Configuration of the MSS interfaces to the FPGA fabric.
 - Refer to the UG0880: PolarFire SoC FPGA Microprocessor Subsystem (MSS) User Guide for detailed information about the MSS Fabric Interface Controller (FIC) features.
- Selection and assignment of the MSS peripherals to the MSS dedicated I/Os and/or the FPGA fabric dedicated peripheral interfaces.
 - Refer to the UG0886: PolarFire SoC FPGA Peripherals User Guide for detailed information about the MSS Peripherals features.
- Configuration of the MSS Bank voltages and I/O standards and attributes.
 - Refer to the UG0916: PolarFire SoC FPGA IO User Guide for detailed information about the MSS Banks and I/Os features.
- Configuration of the MSS DDR memories (DDR3/L, DDR4, LPDDR3, and LPDDR4).
 - Refer to the UG0906: PolarFire SoC FPGA DDR Memory Controller User Guide for detailed information about the MSS DDR4, DDR3, LPDDR3, and LPDDR4 features.
- · Configuration of the MSS debug features.
 - Refer to the UG0888: PolarFire SoC FPGA Trace and Debug User Guide for detailed information about the MSS debug features.

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