Core10100 v5.1 Release Notes

This is the production release for the Core10100 IP core. This release notes describe the Core10100 IP for the SmartFusion®2 and IGLOO®2 supports. It also contains information about system requirements, supported families, implementations, and known issues and workarounds.

Features

Core10100 supports the following:

1. Ethernet media access controller
2. IEEE™ 802.3a CSMA/CD
3. Synchronous interface
4. 8, 16, and 32-bit host interface
5. Reduced media independent interface (RMII) or MII PHY interface

Interfaces

Legacy interface with simple synchronous register and memory interfaces.

Delivery Types

Core10100 is licensed in two ways: Obfuscated and register transfer level (RTL).

Obfuscated

Complete RTL code is provided for the core, enabling the core to be instantiated with SmartDesign. Simulation, Synthesis, and Layout can be performed with Libero® integrated design environment (IDE) and Libero System-on-Chip (SoC). The RTL code for the core is obfuscated, and some of the testbench source files are not provided. They are precompiled into the compiled simulation library instead.

RTL

Complete RTL source code is provided for the core and testbenches.

Supported Families

- SmartFusion2
- IGLOO2
- IGLOO
- IGLOOe
- ProASIC3
- ProASIC3E
- ProASIC®3L
- Fusion
- ProASIC PLUS®
- Axcelerator®
- RTAX-S™

Supported Tool Flows

Use Libero IDE v9.2 or later with this Core10100 release.

Installation Instructions

The Core10100 CPZ must be installed into Libero software. This is done automatically through the Catalog update function in Libero, or the CPZ file can be manually added using the Add Core catalog feature. Once the CPZ file is installed in Libero, the core can be configured, generated, and instantiated within SmartDesign for inclusion in the Libero project.

Refer to the *Using DirectCore in Libero IDE User Guide* or *Libero SoC online help* for further instructions on core installation, licensing, and general use.

Documentation

The release contains a copy of the *Core10100 Handbook*. The handbook describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, as well as implementation suggestions (refer to "Known Limitations and Workarounds" section).

For updates and additional information about the software, devices, and hardware, visit the Intellectual Property pages on the Microsemi SoC Products Group website: www.microsemi.com/soc.

Supported Test Environments

The following test environments are supported:

- VHDL User testbench
- Verilog User testbench

Release History

Table 1 lists the release history for this document.

Table 1. Release History

Version	Date	Changes
5.1	September 2014	Various issues resolved as listed in Table 2.

Resolved Issues in the v5.1 Release

Table 2 lists the software action requests (SARs) that were resolved in the Core10100 v5.1 release.

Table 2. Resolved Issues in the v5.1 Release

SAR	Description
33396 34032 34787 11700	Handbook updated.
34354	Family parameter issue Resolved.
14845	Core10100 v5.1 Fixed the configuration issue.
14846	For RSTC module CLKR/CLKT are same.

SAR	Description
14847	The PCLK and CLKCSR are the same. RSTCSR and CLKCSR are of the same clock domain, So the double synchronization is not required.
18972	RMII_CLK for RMII generic to 1 which is RMII mode. CLKT for RMII generic to 0 which is MII mode.
25073	Core10100 v5.1 Fixed the missing files issue.
27123	Core10100 v5.1. Fixed the issue of I/O ports not connected to the internal logic after synthesis.
34231	Compiling Core10100 v5.1 IP core for a ProASIC3L device issue fixed.
49585	SmartFusion2 and IGLOO2 supported.

Discontinued Features and Devices

Core10100 v5.1 does not support the advanced microcontroller bus architecture (AMBA®) high-performance bus (AHB) master memory interface and AMBA peripheral bus (APB) register interfaces.

Known Limitations and Workarounds

Table 3 lists the known issues and the associated SARs.

Table 3. Known Issues and Workarounds

SAR	Description
59797	During testing at the University of New Hampshire IEEE Fast Ethernet Interoperability Lab, it was identified that the re-transmit timing on the 11th attempt of the half-duplex backoff algorithm is more aggressive than a uniform distribution. This does not affect the core operation. All other tests passed.
60235	In the *Core10100 v5.1 handbook*, data interface timing diagrams that show the assertion of DATAACK in the clock cycle after DATAREQ is asserted are incorrect. The minimum delay between the assertion of DATAREQ and the assertion of DATAACK is two clock cycles. Refer to the user testbench simulation waveforms for correct data interface timing.

Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo CA 92656 USA
Within the USA: +1(949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996
E-mail: sales.support@microsemi.com

Microsemi Corporation (Nasdaq: MSCC) offers a comprehensive portfolio of semiconductor and system solutions for communications, defense and security, aerospace, and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices, and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; security technologies and scalable anti-tamper products; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, Calif. and has approximately 3,400 employees globally. Learn more at **www.microsemi.com**.

51300013 -1/09.14