RN0114
Release Notes
CoreRGMII v2.1

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About Microsemi

Microsemi Corporation (Nasdaq: MSCC) offers a comprehensive portfolio of semiconductor and system solutions for aerospace & defense, communications, data center and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; enterprise storage and communication solutions, security technologies and scalable anti-tamper products; Ethernet solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, California, and has approximately 4,800 employees globally. Learn more at www.microsemi.com.

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 2.1

The following is a summary of the changes in revision 2.1 of this document.

- The document was updated for v2.1.
- Removed configurable parameter information in Features section. See Key Features, page 2.
- Added testbench to Delivery Types. See Delivery Types, page 2.
- Updated Installation Instructions. See Installation Instructions, page 2.
- Updated Supported Test Environments. See Supported Test Environments, page 2.
- Updated Release History, See Release History, page 3.
- Added Resolved Issues in v2.1 Release. See Resolved Issues in v2.1 Release, page 3.

1.2 Revision 2.0

Revision 1.0 was the first publication of this document.

1 CoreRGMII V2.1 Release Notes

These release notes accompany the production release of CoreRGMII v2.1 IP core. This document provides details about the features, enhancements, system requirements, supported families, implementations, and known issues and workarounds.

1.1 Key Features

CoreRGMII is a configurable core with the following features:

- Reduced pin-count interface for Ethernet physical layers (PHYs)
- Gigabit media independent interface (GMII) towards the microcontroller subsystem (MSS)-side and reduced GMII (RGMII) on the PHY-side
- 10/100/1000 Mbps mode operation
- Configurable parameter for core management interface address
- Full-duplex operation at 10/100/1000 Mbps and half-duplex operation at 10/100 Mbps

1.2 Delivery Types

CoreRGMII is licensed as clear RTL.

1.2.1 RTL

Complete RTL source code is provided for the core and testbench.

1.3 Supported Families

- SmartFusion®2

1.4 Supported Tool Flows

CoreRGMII v2.1 requires Libero® System-on-Chip (SoC) v11.0 or later.

1.5 Installation Instructions

The CoreRGMII `.CPZ` file must be installed in the Libero software. This is automatically installed through the **Catalog** update function in the Libero software, or the `.CPZ` file can be manually added using the **Add Core** catalog feature. Once installed in the Libero catalog, the core can be instantiated and configured.

For more information and instructions on core installation, licensing, and general use, see the Using DirectCore section in *Libero SoC for Classic Constraint Flow User Guide* or *Libero SoC Online Help*.

1.6 Documentation

This release contains a copy of the *CoreRGMII Handbook*. This handbook describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and also provides implementation suggestions. For instructions on obtaining Intellectual Property (IP) documentation, see the *Libero SoC Online Help*.

For more information about IP, see http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores. For updates and additional information about software, FPGAs, and hardware, see http://www.microsemi.com.

1.7 Supported Test Environments

- Verilog user testbench
- VHDL user testbench

1.8 Discontinued Features and Devices

The `DEF_SPD` parameter to select the default line speed on reset is removed in CoreRGMII v2.1.

1.9 Known Issues and Workarounds

There are no known issues and workarounds for CoreRGMII v2.1.

1.10 Release History

The following table lists the release history of CoreRGMII.

Table 1 • **Release History**

Version	Date	Changes
2.0	December 2014	Initial release
2.1	February 2017	As listed in the following table.

1.11 Resolved Issues in the v2.0 Release

There were no unresolved SARs for CoreRGMII v2.0. This was the first production release.

1.12 Resolved Issues in v2.1 Release

The following table lists the SARs that are resolved in CoreRGMII v2.1 release.

Table 2 • **Resolved SARs in CoreRGMII v2.1 release**

SAR#	Description
79470	Compilation failing with syntax errors in the VHDL RTL code.
85569	Need to license lock core as per marketing requirement.
86185	Need user testbench for verification.
86686	MDIO read operation not happening.