HB0569

CoreRGMII v2.1 Handbook

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Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA
Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996
E-mail: **sales.support@microsemi.com**
www.microsemi.com

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 2.0

Updated changes related to CoreRGMII v2.1.

1.2 Revision 1.0

Revision 1.0 was the first publication of this document. Created for CoreRGMII v2.0.

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2 Preface

2.1 About this Document

This handbook provides details about the CoreRGMII DirectCore IP, and how to use it.

2.2 Intended Audience

FPGA designers using Libero® System-on-Chip (SoC).

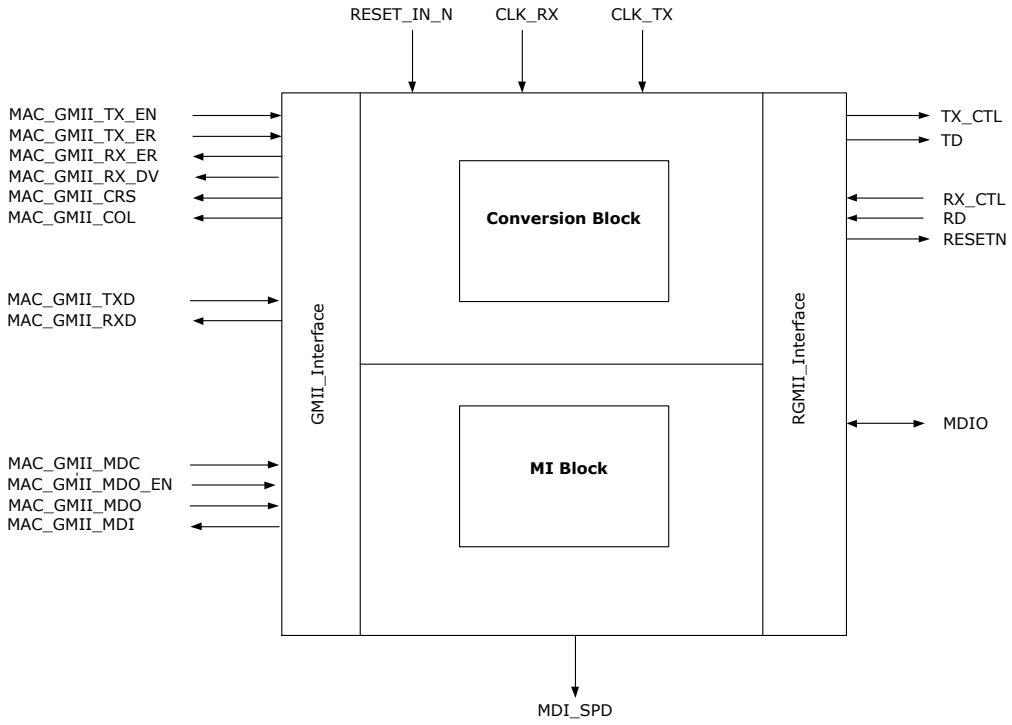
3 Introduction

3.1 Overview

Reduced gigabit media independent interface (RGMII) is a standard interface, which helps in reducing the number of signals required to connect a PHY to a MAC. CoreRGMII is responsible for providing the interface between a standard gigabit media independent interface (GMII) to RGMII conversion. The fifteen-signal GMII interface is converted into six-signal RGMII interface by using both edges of the clock.

The IP core is compatible with the RGMII specification v2.0 that is designed to support the SmartFusion®2 system-on-chip (SoC) field programmable gate array (FPGA) device family. The SmartFusion2 Ethernet MAC (EMAC) supports IEEE 802.3 10/100/1000 Mbps Ethernet operation.

Figure 1 CoreRGMII Block Diagram



3.2 Features

CoreRGMII is a configurable core and has the following features:

- Provides reduced pin-count interface for Ethernet PHYs
- Provides GMII interface towards the microcontroller subsystem (MSS)-side and RGMII interface on the PHY-side
- Supports 10/100/1000 Mbps mode operation
- Configurable parameter for Core Management Interface Address
- Supports full-duplex operation at 10/100/1000 Mbps and half-duplex at 10/100 Mbps

3.3 Core Version

This handbook is for CoreRGMII version 2.1.

3.4 Supported Families

- SmartFusion®2

3.5 Device Utilization and Performance

A summary of the utilization data of CoreRGMII is listed in Table 1. It provides the utilization and performance data for the SmartFusion2 (M2S050T) device family. The provided data is only indicative. The overall device utilization and performance of the core is system dependent.

Table 1 CoreRGMII Device Utilization and Performance

FPGA Family	TRANSFER_SPEED	Logic Elements				Performance (MHz)
		DFF	4LUT	Total	%	
SmartFusion2 (M2S050T)	10/100/1000	123	103	226	0.40	REFCLK = 125

Note: The data in this table was achieved using typical synthesis and layout settings. Frequency (in MHz) was set to 125 and speed grade of -1.

4 Functional Description

CoreRGMII consists of two functional blocks - the Conversion block and the Management Interface (MI) block, refer to Figure 1.

4.1 Management Interface Block

The MI block decodes the MAC <-> CORE MDIO transactions and is used to select an appropriate clock conditioning circuitry (CCC) output for the negotiated line speed.

The Core has a default address of 28(0x1C), but can be set from 0 to 31.

4.2 Conversion Block

The conversion block converts GMII into RGMII using DDRIO and must connect to FPGA ports at the top-level.

4.3 Protocol Boundaries

The MSS Ethernet MAC operates in GMII mode and the PHY operates in RGMII mode. Hence, MAC_GMII_TX_CLK does not get generated by the PHY, but gets generated by Core controlled clock conditioning circuit. MAC_GMII_TX_CLK and MAC_GMII_GTX_CLK are supplied to the MSS by the same clock generated by the CCC.

5 Interface

Signal descriptions for CoreRGMII are provided in Table 2.

Table 2 I/O Signal Description

Name	Direction	Description	
Clock and Reset Signals			
CLK_RX	Input	RGMII Receive Clock from PHY	From PHY to Core
CLK_TX	Input	RGMII Transmit Clock	From CCC to Core
RESET_IN_N	Input	System reset. Active low asynchronous reset	System Level Reset
MSS Interface			
MAC_GMII_TXD [7:0]	Input	GMII transmit data	From MSS to Core
MAC_GMII_TX_EN	Input	Transmit enable	From MSS to Core
MAC_GMII_TX_ER	Input	Transmit Error	From MSS to Core
MAC_GMII_RXD[7:0]	Output	MII Receive data	From Core to MSS
MAC_GMII_RX_DV	Output	Receive data valid	From Core to MSS
MAC_GMII_RX_ER	Output	Receive error	From Core to MSS
MAC_GMII_COL	Output	Collision, considered asynchronous	From Core to MSS
MAC_GMII_CRS	Output	Carrier Sense, considered asynchronous	From Core to MSS
PHY Interface			
TD[3:0]	Output	Transmit Data to PHY	From Core to PHY
TX_CTL	Output	Transmit Control To PHY. The TX_CTL signal carries: • MAC_GMII_TX_EN on the rising edge • (MAC_GMII_TX_EN xor MAC_GMII_TX_ER) on the falling edge	From Core to PHY
RD[3:0]	Input	Receive Data from PHY	From PHY to Core
RX_CTL	Input	Receive Control from PHY. The RX_CTL signal carries: • mac_gmii_rx_dv (data valid) on the rising edge • (mac_gmii_rx_dv xor mac_gmii_rx_er) on the falling edge	From PHY to Core
RESETN	Output	Reset Output to PHY	From Core to PHY
MDIO	Inout	Management Interface	Between Core and PHY
MSS GMII Interface			
MDI_SPD[1:0]	Output	CCC Clock Speed selection signals	From Core to CCC
MAC_GMII_MDC	Input	MII Clock	From MSS to Core and PHY
MAC_GMII_MDO_EN	Input	MII Output enable for Tristating BIBUF	From MSS to Core
MAC_GMII_MDO	Input	MII Data from MSS to Core/PHY	From MSS to Core and PHY
MAC_GMII_MDI	Output	MII Data(muxed between PHY & Core)	From Core to MSS

5.1 Configuration Parameters

CoreRGMII configuration options are listed in Table 3. Use Configuration dialog box in SmartDesign to configure CoreRGMII.

Table 3 CoreRGMII Configuration Parameters

Name	Valid Range	Default	Description
FAMILY	19	19	19: SmartFusion2
COR_ADDR	0 - 31	28	Address of the core on the management interface. **Note:** MSS Hard MAC user to avoid the address 30.

6 Timing Diagrams

Figure 2 represents timing diagram of the packet transmitted. CoreRGMII takes 8-bit GMII data on rising edge of the transmit clock and generates 4-bit RGMII data on both edges of transmit clock.

Figure 2 CoreRGMII Timing Diagram of Packet Transmitted

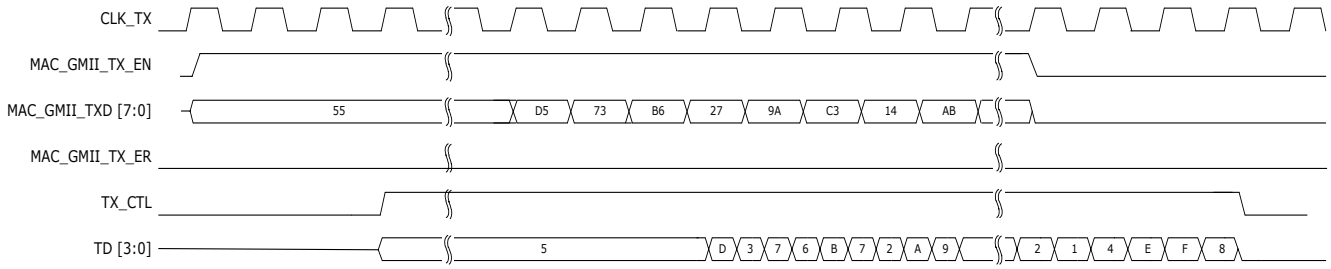
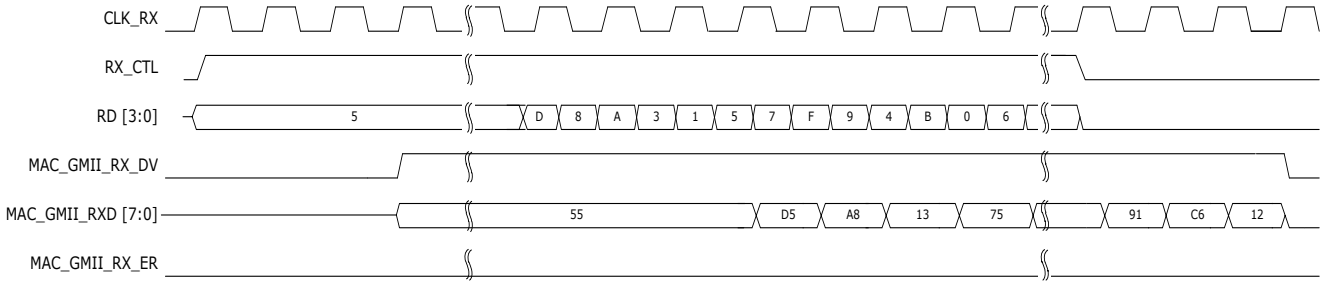


Figure 3 represents timing diagram of the packet received. CoreRGMII takes 4-bit RGMII data on both edges of the receive clock and generates 8-bit GMII data on rising edges of receive clock.

Figure 3 CoreRGMII Timing Diagram of Packet Received



7 Tool Flow

7.1 License

CoreRGMII is licensed as clear RTL.

7.2 RTL

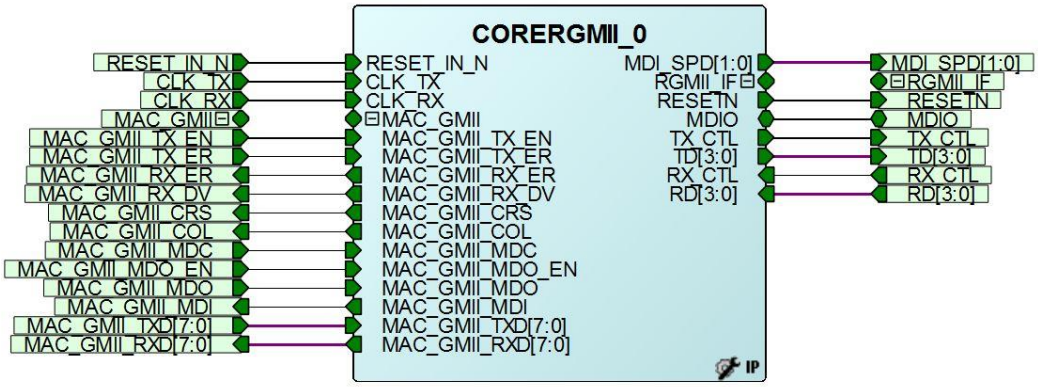
Complete RTL source code is provided for the core and testbench.

7.3 SmartDesign

CoreRGMII is pre-installed in the SmartDesign IP deployment design environment or downloaded from the online repository. Figure 4 shows an example instantiated. The core can be configured using the configuration GUI within SmartDesign, as shown in Figure 5.

For more information on using SmartDesign to instantiate and generate cores, refer to the Using DirectCore in Libero® System-on-Chip (SoC) User Guide.

Figure 4 SmartDesign CoreRGMII Instance View



7.4 Configuring CoreRGMII in SmartDesign

Figure 5 Configuring CoreRGMII in SmartDesign

7.5 Simulation Flows

User testbench for CoreRGMII is added in this version.

To run simulations, select User Testbench in core configuration window. When SmartDesign generates the Libero project, it installs the user testbench files.

To run the user testbench, the design root must be set to the CoreRGMII instantiation in Libero design hierarchy pane. Modelsim® can be invoked by clicking Simulation in Libero design flow pane. This runs simulations automatically.

7.6 Synthesis in Libero

To run synthesis on the CoreRGMII, set the design root to the IP component instance and run the synthesis tool from the Libero design flow pane.

7.7 Place-and-Route in Libero

After the design is synthesized, run the compilation and then place-and-route tool from the Libero design flow pane. Run the place-and-route tool with the Timing Driven and High Effort Layout options enabled.

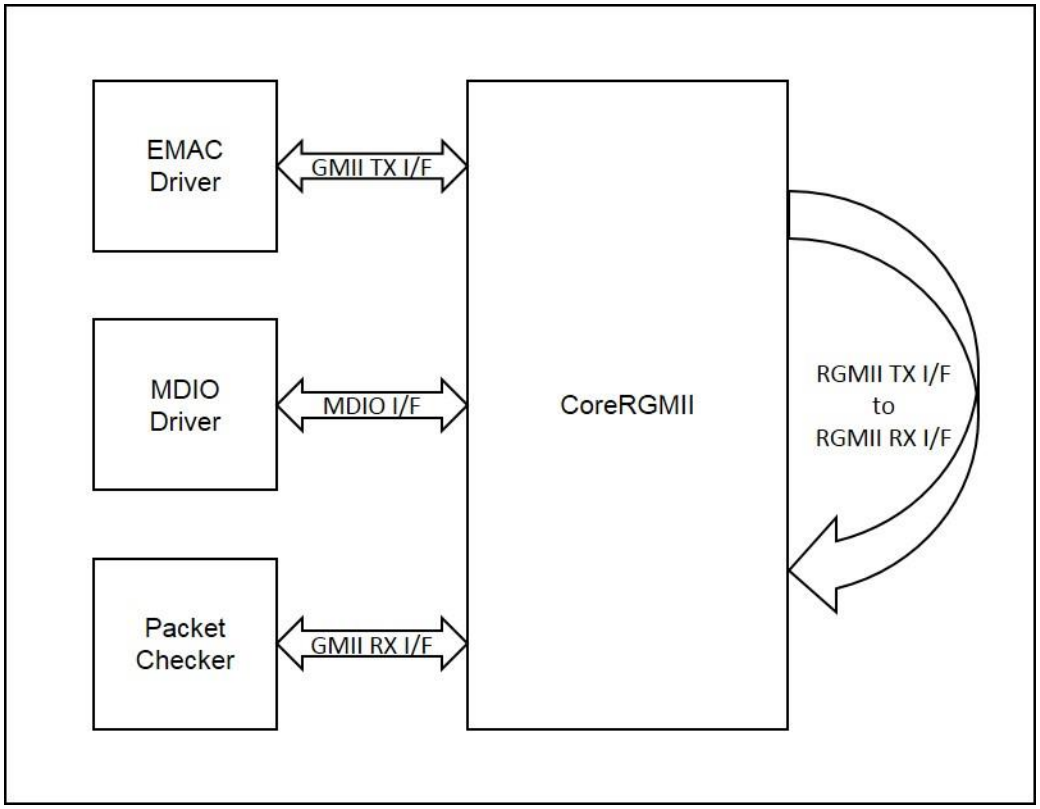
8 Testbench

A unified test-bench is used to verify and test CoreRGMII called as user test-bench.

8.1 User Test-bench

An example user testbench is included in CoreRGMII which performs simple loopback tests for speeds 10/100/1000 Mbit/s. A simplified block diagram of user testbench is shown in Figure 6.

Figure 6 CoreRGMII User Test-bench



The user testbench instantiates CoreRGMII design under test (DUT). MDIO driver tasks configures MDIO registers of CoreRGMII for 10/100/1000 Mbit/s link speed. The EMAC driver tasks drives the transmit signals (Ethernet packet) to the GMII interface of CoreRGMII. CoreRGMII converts these transmit signals into corresponding transmit signals on RGMII interface. The RGMII transmit data and control signals are connected to RGMII receive data and control signals through loopback connection. CoreRGMII converts receive signals into corresponding receive signals on GMII interface. The packet checker compares the GMII received data with the GMII transmit data and displays the result of the tests performed.

9 System Integration

The example design implements CoreRGMII with the Webserver application.

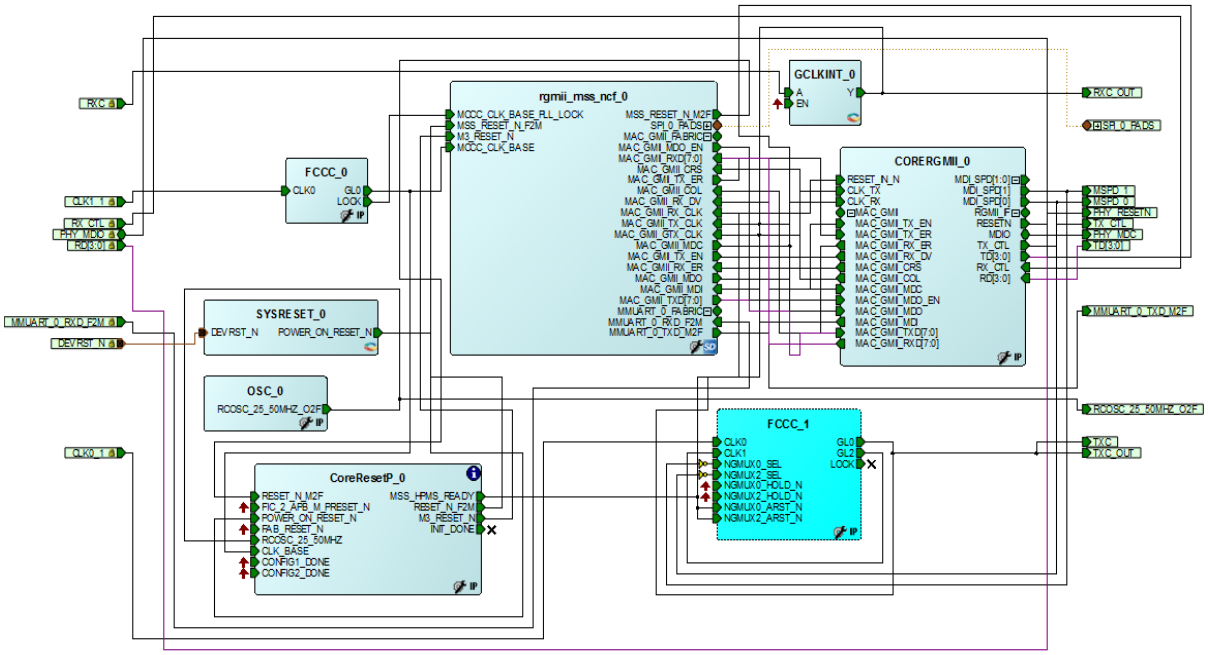
This example design describes the following:

- Use of SmartFusion2 Ethernet MAC connected to an independent interface (GMII) PHY through CORERGMII.
- Integration of the SmartFusion2 MAC driver with the lwIP TCP/IP stack and the FreeRTOS operating system.

The microcontroller subsystem (MSS) of the SmartFusion2 device has an instance of the MAC peripheral that can be configured between the host PC and the Ethernet network at the 10/100/1000 Mbps data transfer rates.

For more information on the MAC interface for the SmartFusion2 devices, refer to the *SmartFusion2 Microcontroller Subsystem User Guide*

Figure 7 CoreRGMII Example Design



- FABRIC RESET (SYSRESET_0) is used for all resets.
- The CORERGMII has CLK_TX, CLK_RX, and MAC_GMII_MDC clocks.
- The MAC_GMII_MDC clock input to CoreRGMII is being generated by MSS MAC.
- CLK_TX and CLK_RX are 2.5, 25, and 125 MHz are generated from FCCC_1 depending on 10/100/1000 Mbps respectively based on MDI_SPD.

Note: The example design is tested on Microsemi internal platform and design can be obtained from the Microsemi technical support team.

10 Register Map and Descriptions

CoreRGMII has one RW register at address 0 accessed through the management interface.

- Bit 13 controls the selection between 25 MHz and 2.5 MHz
- Bit 6 controls the selection between 125 MHz and either 25 MHz or 2.5 MHz

Default reset speed is set to 10 Mbps; otherwise the speed is set as listed in Table 4.

Table 4 Speed Settings for Register Bit 6 and Bit 13

Bit 6	Bit 13	Description
1	1	Reserved
1	0	1000 Mbps
0	1	100 Mbps
0	0	10 Mbps

11 Ordering Information

11.1 Ordering Codes

CoreRGMII can be ordered through your local sales representatives. It must be ordered using the following number scheme: CoreRGMII-XX, where XX is listed in Table 5.

Table 5·Ordering Codes

XX	Description
RM	RTL source multi-use license. **Note:** CoreRGMII is licensed.