RN0174

Core10GMAC v2.2 Release Notes

Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA
Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996
E-mail: sales.support@microsemi.com
www.microsemi.com

About Microsemi

Microsemi Corporation (Nasdaq: MSCC) offers a comprehensive portfolio of semiconductor and system solutions for aerospace & defense, communications, data center and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; enterprise storage and communication solutions, security technologies and scalable anti-tamper products; Ethernet solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, Calif., and has approximately 4,800 employees globally. Learn more at www.microsemi.com.

51300174-3/12.18

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 3.0

Updated for Core10GMAC v2.2.

1.2 Revision 2.0

Updated for Core10GMAC v2.1.

1.3 Revision 1.0

Revision 1.0 was the first publication of this document. Created for Core10GMAC v2.0.

Contents

2 Core10GMAC v2.2 Release Notes

2.1 Overview

These release notes accompany the production release of Core10GMAC v2.2. This document provides details about the features, enhancements, system requirements, supported families, implementations, and known issues and workarounds.

2.2 Features

Core10GMAC has the following features:

- Ethernet MAC / RS / PAUSE
- Link Training
- Auto-Negotiation

2.3 Delivery Types

Core10GMAC is licensed with evaluation and obfuscated RTL.

2.3.1 Obfuscated

Complete RTL code is provided for the core, enabling the core to be instantiated with SmartDesign. Simulation, Synthesis, and Layout can be performed with Libero software. The RTL code for the core is obfuscated using the IP encryption (encryptP1735.pl) solution.

2.3.2 Evaluation

Complete RTL code is provided for the core, enabling the core to be instantiated with SmartDesign. Simulation, Synthesis, and Layout can be performed with Libero software. The RTL code for the core is obfuscated using the IP encryption (encryptP1735.pl) solution and has a time bomb feature which will stop functioning after 4 or 8 hours time at 10Gbps data rate using 64bit at 156.25MHz or 32bit at 312.5MHz clock respectively.

2.4 Supported Families

- PolarFire®

2.5 Supported Tool Flows

Core10GMAC v2.2 requires Libero SoC PolarFire.

2.6 Installation Instructions

The Core10GMAC CPZ file must be installed into Libero software. This is done automatically through the Catalog update function in Libero, or the CPZ file can be manually added using the **Add Core** catalog feature. Once the CPZ file is installed in Libero, the core can be configured, generated, and instantiated within SmartDesign for inclusion in the Libero project.

Refer to the *Libero SoC Online Help* for further instructions on core installation, licensing, and general use.

2.7 Documentation

This release contains a copy of the *Core10GMAC Handbook*. The handbook, describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and also implementation suggestions. Refer to the *Libero SoC Online Help* for instructions on obtaining IP documentation.

For updates and additional information about the software, devices, and hardware, visit the Intellectual Property pages on the Microsemi SoC Products Group website: visit:

http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores.

2.8 Supported Test Environments

No testbench is provided with Core10GMAC.

2.9 Resolved Issues in v2.2 Release

Table 1 • **Resolved SARs in Core10GMAC v2.2 Release**

SAR	Description
99952	Accessing C73 and C72 rx registers through AHB when no Rx signal present causes crash.
98848	Shim layer for AN needs to be updated.

2.10 Known Limitations and Workarounds

There are no known limitations and workarounds for Core10GMAC.