RN0113

CoreCIC v2.1 Release Notes

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 2.0

Updated changes related to CoreCIC v2.1.

1.2 Revision 1.0

Revision 1.0 was the first publication of this document. Created for CoreCIC v2.0

Contents

2 CoreCIC v2.1 Release Notes

2.1 Overview

These release notes accompany the production release of CoreCIC v2.1. This document provides details about the features, enhancements, system requirements, supported families, implementations, and known issues and workarounds.

2.2 Features

- Fixed or programmable rate change from 2 to 1024
- One to eight integrator-comb stages
- Comb differential delay of one or two
- Signed 2's complement input data
- Input data width from 1 to 32 bits
- Output data width up to 100 bits
- Choice of output data truncation and two rounding types
- Optional Hogenauer pruning
- Support for up to 64 channels

2.3 Interfaces

No standard interface is available.

2.4 Delivery Types

CoreCIC is licensed for register transfer level (RTL). Complete HDL source code is provided for the core and testbenches.

2.5 Supported Families

- PolarFire®
- RTG4™
- IGLOO®2
- SmartFusion®2

2.6 Supported Tool Flows

- CoreCIC v2.1 requires Libero v11.3 or later
- Supports Windows and Linux operating systems

2.7 Installation Instructions

The CoreCIC CPZ file must be installed into Libero software. This is done automatically through the Catalog update function in Libero, or the CPZ file can be manually added using the **Add Core** catalog feature. Once the CPZ file is installed in Libero, the core can be configured, generated, and instantiated within SmartDesign for inclusion in the Libero project.

Refer to the *Libero SoC Online Help* for further instructions on core installation, licensing, and general use.

2.8 Documentation

This release contains a copy of the *CoreCIC Handbook*. The handbook, describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and also implementation suggestions. Refer to the *Libero SoC Online Help* for instructions on obtaining IP documentation.

For updates and additional information about the software, devices, and hardware, visit the Intellectual Property pages on the Microsemi SoC Products Group website: visit:

http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores.

2.9 Supported Test Environments

- Verilog user testbench
- VHDL user testbench

2.10 Discontinued Features and Devices

There are no discontinued features for this release of CoreCIC v2.1.

2.11 Known Limitations and Workarounds

There are no known limitations or workarounds.

2.12 Resolved History

Table 1 lists the release history for CoreCIC.

Table 1 • **Release History**

Version	Date	Changes
2.1	January 2018	Resolved SARs listed in Table 2.
2.0	August 2014	First Production release.

2.12.1 Resolved Issues in the v2.1 Release

Table 2 lists the Software Action Requests (SARS) that were resolved in the CoreCIC v2.1 release.

Table 2 • **Resolved Issues in the v2.1 Release**

SAR Number	Description
92001	Added PolarFire support.