Core1553BRM v4.2 Release Notes

These release notes accompany the production release for Core1553BRM. This document provides details about the features, enhancements, system requirements, supported families, implementations, and known issues and workarounds.

Features

Core1553BRM has the following features:

- MIL-STD-1553B-compliant bus controller, remote terminal, and bus monitor
- Software compatible with legacy 1553 devices
- RT function tested to MIL-1553-HDBK

Interfaces

Core1553BRM supports a simple synchronous backend interface, compatible with earlier versions of Microsemi® peripheral component interconnect (PCI) cores.

Supported Tool Flows

Use Libero® System-on-Chip (SoC) 11.5 or Libero Integrated Design Environment (IDE) v9.2 or later with this Core1553BRM release.

Delivery Types

Core1553BRM is licensed in three ways: Evaluation, Obfuscated, and register transfer level (RTL).

Evaluation

Precompiled simulation libraries provided in Core1553BRM allow the core to be instantiated in SmartDesign and simulated within Libero IDE and SoC software. The design may not be synthesized, as source code is not provided.

Obfuscated

Complete RTL code is provided for the core, enabling the core to be instantiated with SmartDesign. Simulation, synthesis, and layout can be performed with Libero SoC software. The RTL code for the core is obfuscated and some of the testbench source files are not provided. Instead, they are precompiled into the compiled simulation library.

RTL

Complete RTL source code is provided for the core and testbenches.

Supported Families

- RTG™4
- SmartFusion®2
- IGLOO®2
- Fusion®
- SmartFusion®
- IGLOO®
- IGLOOe
- ProASIC®3/E
- ProASIC PLUS®
- Axcelerator®
- RTAX™-S
- SX-A
- RTSX-S

Install Instructions

Core1553BRM is available through the Libero SoC IP Catalog. Within Libero SoC, a local Core1553BRM cpz file can be located and installed in the catalog by clicking **Add Core**, or by using the automatic web update feature. Once the CPZ file is installed in Libero SoC software, the core can be instantiated, configured, and generated within SmartDesign for inclusion in the Libero SoC project.

For RTL and Obfuscated versions of the core, the FlexLM® license must be installed and SmartDesign must be restarted before the core can be exported. Consult Libero SoC online help for the instructions on core installation and licensing.

Documentation

This release contains a copy of the Core1553BRM Handbook, which describes the core functionality, gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and also provides implementation suggestions. The document can be viewed by right-clicking the **Core Selection** window in SmartDesign after the core has been installed.

For more information about Intellectual Property, visit: http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores. For updates and additional information about software, FPGAs, and hardware, visit: www.microsemi.com.

Supported Test Environments

The following test environments are supported:

- VHDL verification testbench
- VHDL user testbench
- Verilog user testbench

Discontinued Features and Devices

No features have been discontinued in the v4.2 Core1553BRM release.

New Features and Devices

The following new features and devices are included in v4.2 release:

- Updated release notes are provided.

Core Versions

The reset value of the lowest eight bits of register six, the built-in test register (BIT), indicates the version of the core. This value can be read through the CPU interface, or the core transmits this in response to Transmit BIT mode code. Table 1 shows how the versions are encoded.

Table 1. Encoding of Core Versions

Version	Bit[7:0]
v1.0	0
v2.0	1
v2.1	2
v2.11	3
v2.12	4
v2.13	5
v2.14/v2.15	7
v2.16	8
v2.17	9
v3.0 / v3.1	10
v3.2	11
v4.0	12
v4.1 / v4.2	13

Resolved Issues in the v4.2 Release

Table 2 lists the software action requests (SARs) that were resolved in Core1553BRM v4.2.

Table 2. Resolved SARs in the Core1553BRM v4.2 Release

SAR No.	Description
78626	Core1553BRM IIW (2.17 Version) is read 0x0000 Occasionally.

Resolved Issues in the v4.1 Release

Table 3 lists the software action requests (SARs) that were resolved in Core1553BRM v4.1.

Table 3. Resolved SARs in the Core1553BRM v4.1 Release

SAR No.	Description
47408	Added RTG4 Support.

Resolved Issues in the v4.0 Release

Table 4 lists the SARs that were resolved in Core1553BRM v4.0.

Table 4. Resolved SARs in the Core1553BRM v4.0 Release

SAR No.	Description
17552	Why does the BC in the BRM read the opcode in state BCILIST and BCGETOPCODE
29111	Please fix RSTOUTn
33037	Typo in "CORE1553BRM_HB.pdf"
35649	1553BRM Reset Mode code doesn't reset internal decoder
41028	Issue applying ACKVALUE when CLKSPD or CPUMEMEN hardwired to fixed value
20928	Unexpected ActSpiritHdl error when generating Core1553BRM v3.0 in VHDL/RTL mode
49905	Doc bug: "The CPU interface signals are internally synchronized to the Core1553BRM master clock" is not correct
51002	Doc: Update recommendations on transceivers.
24477	Double resynchronization to avoid meta-stability issues.
36209	Add option to have state machine with Hamming-2 protection.
46840	VHDL: Add underflow/overflow protection to counters.
46841	VHDL: Incomplete sensitivity list.
46839	VHDL: Use when others instead of explicit unused states.
46837	VHDL: syn_encoding typographical error in code.

Resolved Issues in the v3.2 Release

Table 5 lists the software action requests (SARs) that were resolved in Core1553BRM v3.2.

Table 5. Resolved SARs in the Core1553BRM v3.2 Release

SAR No.	Description
20928	Unexpected ActSpiritHdl error when generating Core1553BRM v3.0 in VHDL/RTL mode.
14285	Obfuscation of VHDL source files removes syn_preserves.
32639	Updated VHDL files for SmartFusion.

Resolved Issues in the v3.1 Release

Table 6 lists the SARs that were resolved in Core1553BRM v3.1.

Table 6. Resolved SARs in the Core1553BRM v3.1 Release

SAR No.	Description
11355	In the handbook, the CPUMEM address signal description is changed to CPUADDR[5:0] instead of CPUADDR[2:0], since there are 33 registers in the core.
11580	Updated the handbook for RSTOUTn. The RSTOUTn is asserted on the RSTINn input or the setting of the internal SRST bit (bit 13 of register 0).
11938	In the handbook, the CPUMEM address signal description is changed to CPUADDR[5:0] to access 33 registers in the core.
14895	Updated handbook for buffer mode selection. EMODE = 00 or 01: Select ping-pong or index mode buffer EMODE = 10: Select circular buffer mode 1 EMODE = 11: Select circular buffer mode 2
14921	Basically before changing bits [15:1], the STEX bit must be zero. So the user reads the bit; if HIGH, change bit 0 to '0' and write, then write to other bits.
21558	Updated handbook so that the Start BIT (SBIT) must be Low to initiate core operation. This bit must be low to start execution.
11703	Used $finish instead of $stop in testbench, so that ModelSim® exits at the point when it sees a $finish.
11763	Now the user can use the Very high speed integrated circuit (VHSIC)-hardware description language (HDL) (known as VHDL), verification environment to verify the Verilog core, but must have simultaneous verilog and VHDL licenses for OEM ModelSim; or must use the production version of ModelSim (not the OEM version shipped with Libero SoC software) to perform mixed language simulation with an appropriate license from Mentor Graphics.
11950	The IGLOOe library is used in ram16x16.vhd, when the project is targeted to an IGLOOe device.
11951	Removed undefined GLOBALBUFF that is instantiated into BRMpc.v.
20277	Now the user can use the VHDL verification environment to verify the Verilog core, but must have simultaneous Verilog and VHDL licenses for OEM ModelSim, or must use the production version of ModelSim (not the OEM version shipped with Libero SoC software) to perform mixed language simulation with an appropriate license from Mentor Graphics.
21059	Core1553BRM is supported on Linux.
12011	CCZ/CPZ verification: Obfuscated version is available in tool/package.
12013	Removed pre-synthesis simulation error.
12016	CCZ/CPZ verification: Issues with Eval Pre-Synthesis Simulation resolved.
12017	Removed undefined GLOBALBUFF.
12018	VHDL verification testbench is working now.
12033	CCZ verification: Verilog Pre-Synthesis Looping resolved.
12034	The synthesis warnings listed here can be ignored.
20276	Inserted GLOBALBUFF.vhd and RAM16X16.vhd files in Axcelerator device.
20892	Verification testbench generation works properly.
20927	Verification testbench is generated in RTL mode.

Resolved Issues in the v3.0 Release

Table 7 lists the SARs that were resolved in the Core1553BRM v3.0 release.

Table 7. Resolved SARs in the Core1553BRM v3.0 Release

SAR No.	Description
59858	Ping Pong mode operation updated to prevent turnoff mid message. When this occurs, the A/B buffer pointer may be incorrect. Core now delays turning ping-pong off until message processing is complete, and signals this using the ping-pong acknowledge bit.
64332	Ping Pong operation updated to indicate last buffer and next buffer to be used.
64328	New generics added to allow user specification of the backend memory access timeouts to allow trade-offs between bus grant and bus wait times.
64329	LOCKFREQ generic added to prevent the operational frequency of the core being changed when the enhanced features are enabled. Setting this generic lowers the tile counts.

Resolved Issues in the v2.17 Release

Table 8 lists the SARs that have been resolved in the Core 1553BRM v2.17 release.

Table 8. Resolved Issues in v2.17

SAR No.	Description
57312	The Bus Monitor may fail to set the parity or Manchester error bits in the Monitor Message Information Word. However, it detects these protocol errors and sets the message error bit. This problem has been resolved and the core now correctly sets these bits.

Resolved Issues in the v2.16 Release

Table 9 lists the SARs that have been resolved in the Core 1553BRM v2.16 release.

Table 9. Resolved Issues in v2.16

SAR No.	Description
56170	When in Bus controller mode, the end of list opcode may not generate the EOL interrupt. This happens when the previous opcode generates an interrupt condition (typically on message error condition) and the CPU has not processed that interrupt. If the previous interrupt has been acknowledged, the EOL interrupt will be generated. v2.16 of the core is corrected so the EOL interrupt is generated.

Resolved Issues in the v2.15 Release

Table 10 lists the SARs that have been resolved in the Core 1553BRM v2.15 release.

Table 10. Resolved Issues in v2.15

SAR No.	Description
55491	Architecture names in the VHDL global buffer source files updated to resolve compiled simulation library refresh issue.
55215	Compiled Simulation Libraries updated to resolve "no debug" error messages when Model*Sim* is invoked to simulate the testbenches (all RTL source files are identical to v2.14).

Resolved Issues in the v2.14 Release

Table 11 lists the SARs that have been resolved in the Core 1553BRM 2.14 release.

Table 11. Resolved Issues in v2.14

SAR No.	Description
52998	RT enhanced Ping Pong enable/disable operation does not function correctly. The core has been updated to allow the PPEN bit to be set to 0 while the RT is operational, with read back of the bit available in bit 9 of the control register. If PPEN is set to 0 (when STEX = 1), the RT remains in Ping Pong mode but does not switch between the A and B buffers. It always accesses the next buffer as indicated by the A/B bit in the descriptor control word.

Resolved Issues in the v2.13 Release

Table 12 lists the SARs that have been resolved in the Core1553BRM v2.13 release.

Table 12. Resolved Issues in v2.13

SAR No.	Description
49744	The core does not detect a loopback error in the last word of a message; the loopback failure is reported on the following message instead. The core has been updated to resolve this issue and the datasheet now specifies a maximum loopback delay.
48095	Legalization registers do not support byte accesses when RAM cells are used. The core has been updated to allow byte accesses when ProASIC^{PLUS} (APA) RAMs are used or registers are used (LEDREGS = 1 or 3).
49745	The core now supports an internal loopback feature enabled by bit 6 of the enhancements register.
49759	The TEXTIO package used in the testbench does not format integers correctly when printed as bit values, and an internal loop generates a simulation fatal error if the coverage option is enabled in Model*Sim* v6.0. Both issues have been fixed.

Resolved Issues in the v2.12 Release

Table 13 lists the SARs that have been resolved in the Core1553BRM 2.12 release.

Table 13. Resolved Issues in v2.12

SAR No.	Description
44392	In RT mode, the core may burst 7 cycles, not 6 cycles as expected. When configured in Circular mode 2, the RT can burst write up to 7 words to memory. The backend timing parameters assumed that the maximum burst size was 6 words, and that this, along with the 4-word burst read, had to complete in 22 µs. Actually, the core has only 19 µs to complete message processing before the next command word is detected when broadcast mode code with no data messages is being received with minimum inter-message gaps. To guarantee that the memory cycles complete in the maximum backend bus request, grant times have been reduced to allow the 4-word read and 7-word write bursts to be completed in 19 µs.
44473	The RT may generate incorrect message log interrupts. Under normal operation, all interrupts are generated correctly. If the core receives a second legal command word on the alternative bus just as it is completing message processing and generating the interrupt log, then it may not generate the interrupt log for the first message. When the log entry is generated for the second message, it may include interrupt status bits for the first message. For example, the broadcast received interrupt may be set incorrectly if the first message is a broadcast and the second message is not. The core now clears the internal interrupt status bits at the start of message processing when the interrupt log is enabled.

Resolved Issues in the v2.11 Release

Table 14 lists the SARs that have been resolved in the Core1553BRM v2.11 release.

Table 14. Resolved Issues in v2.11

SAR No.	Description
44066	Maximum backend wait pulse timing increased with addition of the BETIMING parameter.
44067	The core can release MEMACC between RT descriptor and interrupt log writes; it should hold MEMACC active during this period. This results in an additional unexpected bus request cycle. If the backend memory interface delays the MEMREQ to MEMGNT by greater than 4.66 µs and the RT receives Broadcast mode code with no data, and if the interrupt log is enabled and the inter-message gap to the next message to the same RT is between 4 and 9 µs, then the next message will be incorrectly processed. If MEMREQ to MEMGNT delay is less than 4.66 µs or CPUMEMEN = 1 and the MEMREQn to MEMGNTn is less than 2.4 µs, and then no errors will occur. In v2.11, the core now holds MEMACC true until the interrupt log is written, and the core operates correctly

Resolved Issues in the v2.1 Release

Table 15 lists the SARs that have been resolved in the Core1553BRM v2.1 release.

Table 15. Resolved Issues in v2.1

SAR No.	Description
42857	Asynchronous message support added.

Resolved Issues in the v2.01 Release

Table 16 lists the SARs that have been resolved in the Core1553BRM v2.01 release.

Table 16. Resolved Issues in v2.01

SAR No.	Description
42196	The simulation libraries included in the v2.0 release are not compatible with Model*Sim* v5.8 and above. The simulation libraries have been recompiled with the latest version of Model*Sim*.

Known Issues and Workarounds

Table 17 lists the known issues and the associated SARs.

Table 17. Known Issues and Associated SARs

SAR No.	Description
64326	When the legalization registers are implemented using RAM in Axcelerator, RTAX-S, and ProASIC3/E-based families, the CPU must write to these registers using WORD transfers. Byte writes are not supported. Byte operations are supported when the legalization registers are implemented using registers or ProASIC^{PLUS} memory blocks. If byte accesses are required when using Axcelerator, RTAX-S, or ProASIC3/E-based families, the legalization registers should be implemented using registers.

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