

PolarFire[®] SoC MSS Configurator User Guide

Introduction

The PolarFire SoC MSS Configurator provides a graphical user interface that allows embedded software engineers to quickly define the MSS startup state. It exports an XML file that is consumed by the embedded software flow that converts the XML into initialization constructs. Additionally, the tool outputs a CXZ file for inclusion into your Libero design flow. The CXZ file contains information about metadata and port needed by the FPGA designer to complete the connectivity between the MSS and the FPGA fabric.

MSS configurator is available as a standalone application and as part of the Libero[®] SoC design tool suite. The information in this user guide applies to both.

References

- Configuration of the MSS clocks.
 - For detailed information about the MSS clocking features, see UG0913: PolarFire SoC FPGA Clocking Resources User Guide.
- Configuration of the MSS interfaces to the FPGA fabric.
 - For detailed information about the MSS Fabric Interface Controller (FIC) features, see UG0880: PolarFire SoC FPGA Microprocessor Subsystem (MSS) User Guide.
- Selection and assignment of the MSS peripherals to the MSS dedicated I/Os and/or the FPGA fabric dedicated peripheral interfaces.
 - For detailed information about the MSS Peripherals features, see UG0886: PolarFire SoC FPGA Peripherals User Guide.
- · Configuration of the MSS Bank voltages and I/O standards and attributes.
 - For detailed information about the MSS Banks and I/Os features, see UG0916: PolarFire SoC FPGA IO User Guide.
- Configuration of the MSS DDR memories (DDR3/L, DDR4, LPDDR3, and LPDDR4).
 - For detailed information about the MSS DDR4, DDR3, LPDDR3, and LPDDR4 features, see UG0906: PolarFire SoC FPGA DDR Memory Controller User Guide.
- Configuration of the MSS debug features.
 - For detailed information about the MSS debug features, see UG0888: PolarFire SoC FPGA Trace and Debug User Guide.

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1. Installing the PolarFire SoC MSS Configurator

The PolarFire SoC MSS Configurator bundled with Libero is available at the following location in the Libero installation section:

- Windows: <\$Installation_Directory>\Microsemi\Libero_SoC_vX.X\Designer \bin64\pfsoc_mss.exe
- Linux: <\$Installation_Directory>\Microsemi\Libero_SoC_vX.X\bin64\pfsoc_mss

The PolarFire SoC MSS Configurator can also be installed as a standalone application.

For information about how to install Libero, see www.microsemi.com/product-directory/design-resources/1750-libero-soc#documents.

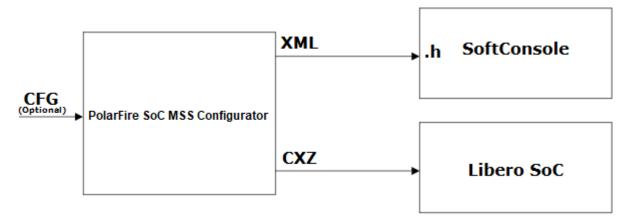
1.1 Input and Output Files

1.1.1 Output Files

The PolarFire SoC MSS Configurator generates the output file formats shown in the following figure.

- XML Configuration File Contains the MSS memory map, clock, DDR memory controller, and peripheral configuration. The XML file is used to generate hardware files required for building the firmware project.
- CXZ File Encapsulates the hardware design of the MSS block and can be imported into Libero SoC project.

Figure 1-1. PolarFire SoC MSS Configurator Block Diagram



1.1.2 Input files

The PolarFire SoC MSS Configurator can be invoked without any input files. A configuration file (.cfg) from an earlier MSS configurator session, can be optionally provided to the PolarFire SoC MSS Configurator.

2. Running the PolarFire SoC MSS Configurator

You can run the PolarFire SoC MSS Configurator in Batch mode or Interactive mode.

2.1 Batch Mode

The PolarFire SoC MSS Configurator application can be executed in the Batch mode for scripted execution as follows:

Windows:

```
<Libero SoC or Standalone MSS Configurator installation area>\bin64\pfsoc_mss.exe -
CONFIGURATION_FILE:<absolute path for configuration file name (.cfg)> -
OUTPUT_DIR:<absolute path for output directory>
```

Linux:

```
<Libero SoC or Standalone MSS Configurator installation area>/bin64/pfsoc_mss -
CONFIGURATION_FILE:<absolute path for configuration file name (.cfg)> -
OUTPUT_DIR:<absolute path for output directory>
```

2.2 Interactive Mode

In the Interactive (GUI) mode, the PolarFire SoC MSS Configurator provides the following high-level options. **Table 2-1. Configurator-Project Menu Options**

Option	Description
New	Starts configuring a new MSS subsystem.
Open	Opens a configuration (.cfg) file.
Save/Save As	Saves the current configuration of the MSS subsystem to a configuration (.cfg) file.
Generate	Generates MSS configuration (.xml) and component (.cxz) files after configuring the MSS subsystem.
Close	Closes the current configuration (.cfg) file.

2.3 Using the PolarFire SoC MSS Configurator GUI

The following section provides information about the MSS Configurator GUI.

2.3.1 Configuration Tabs

The PolarFire SoC MSS Configurator includes the following tabs.

- Clocks
- Fabric Interface Controllers
- I/O Configuration
- I/O REFCLK
- I/O Bank4 and Bank2
- DDR Memory
- Misc

2.3.1.1 Clocks

Use the **Clocks** tab to configure the MSS PLL clock frequency and clock sources. For more information, see UG0913: Microsemi_PolarFire_SoC_FPGA_Clocking_Resources_User_Guide.

The following options are provided.

Option	Description
MSS Reference Clock Input Source	MSS can be clocked from either dedicated I/O from Bank 5 (REFCLK) or from North West PLL output. You can select the NW PLL ports or dedicated I/Os from Bank 5 (REFCLK) to source from an off-chip oscillator.
MSS PLL Clock Frequency	Maximum supported frequency for the CPU cores is 625 MHz. You can set the frequency value of up to 625 MHz. All MSS clock frequencies are derived from this setting.
MSS CPU cores clock frequency Divider	The MSS CPU clock frequency is based off the MSS PLL clock frequency and is set using the divider values of /1, /2, /4, or /8. The frequency must be greater or equal to the MSS AXI clock, and can have a maximum value of 625 MHz.
MSS AXI clock frequency Divider	The MSS AXI clock frequency is based off the MSS CPU clock frequency and is set using the divider values of /1, /2, /4, or /8. The frequency must be greater or equal to MSS AHB/APB clock, and can be a maximum value of 312.5 MHz.
MSS AHB/APB clock frequency Divider	The MSS AHB/APB clock frequency is based off the MSS CPU clock frequency and is set using the divider values of /1, /2, /4, or /8.The maximum supported frequency is 156.25 MHz.
DDR Reference Clock Input Source	You can select the NW PLL ports or I/Os from Bank 5 to source from an off-chip oscillator.

Note: The **DDR Reference Clock Input Source** option appears only when the DDR Memory type is selected from the **DDR Memory** tab.

The following figure shows the **Clocks** tab in the PolarFire SoC MSS Configurator. In this example, the following configuration is used:

- Dedicated I/Os from Bank 5 (REFCLK) are selected as the reference clock input source for the MSS. The MSS PLL clock frequency is set to 625 MHz.
- Dedicated I/Os from Bank 5 (REFCLK) are used to source the reference clock input frequency for the DDR subsystem.
- The DDR clock source and MSS clock source are set to 125 MHz.

Figure 2-1. Clocks Tab

MSS				
MSS Reference Clock Input Source	Dedicated I/O from Bank5 (REFCLK)	•	MSS PLL dock frequency (MHz)	625.000
MSS CPU cores clock frequency Divider	/1	•	MSS CPU cores clock frequency (MHz)	625.000
MSS AXI dock frequency Divider	/2	•	MSS AXI clock frequency (MHz)	312.500
MSS AHB/APB clock frequency Divider	[/4	•	MSS AHB/APB clock frequency (MHz)	156.250
DDR				
DDR Reference Clock Input Source De	dicated I/O from Bank5 (REFCLK)	•		
Clock Sources Frequency				
Dedicated I/O from Bank5 (REFCLK) freq	uency (MHz) 125			

For more information about configuring the MSS DDR subsystem, see DDR Memory.

2.3.1.2 Fabric Interface Controllers

Using the Fabric Interface Controllers tab, any combination of FIC_0, FIC_1, FIC_2, FIC_3 can be enabled and configured to support Master and Slave interfaces. For more information, see UG0880: PolarFire_SoC_FPGA_MSS User Guide

FIC_0, FIC_1 and FIC_2 support AXI4 interfaces, while FIC_3 supports APB.

FIC_0 and FIC_1 have both master and slave interfaces to and from the FPGA fabric, while FIC_2 and FIC_3 support slave or master interfaces, respectively.

The following figure shows all FIC options available and enabled. By default, the DLLs of all the FICs are enabled.

Figure 2-2. Fabric Interface Controllers Tab

Clocks Fabric Interface Controllers I/O C	Configuration
□ FIC_0 (AXI4)	
Use Master interface 🔽 Use Slave inter	face 🔽
Use Embedded DLL	
□ FIC_1 (AXI4)	
Use Master interface 🔽 Use Slave inter	face 🔽
Use Embedded DLL	
□ FIC_2 (AXI4)	
Use Slave interface	
Use Embedded DLL	
□ FIC_3 (APB)	
Use Master interface	
Use Embedded DLL	

Note: The FIC interface can operate up to 250 MHz. The FIC clock is independent of the MSS clock. If the frequency of the FIC block is greater than or equal to 125 MHz, the embedded DLL must be enabled for removing clock insertion delay. If the frequency of the FIC block is less than 125 MHz, the embedded DLL must be bypassed.

When a master interface is enabled for a FIC, that master interface must be connected to a slave in the fabric. When a slave interface is enabled for a FIC, that slave interface must be connected to a master in the fabric.

There is clock domain crossing logic in the FIC block to address the asynchronous MSS and Fabric clocks.

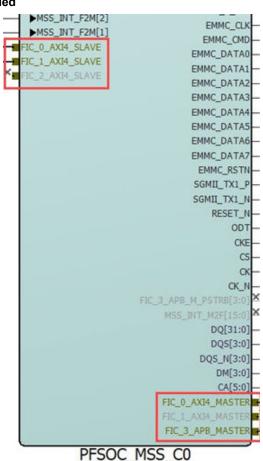


Figure 2-3. FIC Interfaces Enabled

Note: The MSS SmartDesign component is visible only after importing the MSS CXZ file.

2.3.1.3 I/O Configuration

Using the I/O Configuration tab, you can select the following I/Os for the peripherals:

- GPIOs from Bank 2 and Bank 4, which are dedicated to the MSS.
- Fabric I/Os if the dedicated I/Os from Bank 2 and Bank 4 are not available.
- GPIOs from Bank 5 are dedicated to SGMII but can be routed to GMII or MII fabric I/Os. GPIO from Bank 5 are displayed only when Gigabit Ethernet MAC_0 or Gigabit Ethernet MAC_1 is selected.

Note: I/Os from the DDR bank are dedicated to the DDR Controller in the MSS.

For more information, see UG0880: PolarFire_SoC_FPGA_MSS User Guide

The following figure shows the **I/O Configuration** tab on the PolarFire SoC MSS Configurator.

Figure 2-4. I/O Configuration Tab

eMMC 🔺	eMMC			BATK	10 10.1	Turkage Pile	400	118		MAC	QIN	101	MARART	DC	645	6710
USB	eMMC	Unused					BAR, SK		10,04			SHARE.				1000
SD/SDIO	eren,	Inunsea	- 1		1	80	marrian.		10,040				101047,1,000	00,0,90		6000,0,
		-	-		1	80	pater, pater		82,2404					01(3,)04		400.3
Gigabit Ethernet MAC_0	DATA 4 to 7	Unused	-			24	0.010,0400		RD_DADA1				100.487,4,502		COULTON	4000,1
Gigabit Ethernet MAC_1					4	KA	8101,24242		10,500al				MARANY, A, YOD		DOLUMER.	400.0
QSPI						17	0.010,0400		ND, DADAJ				MM/AP7,3,302 (4)		CROCKTORE Y	4000,1
SPI_0							PART, STAR		8,0				MARCAN, A, TID (A)			400.3
							BAR, MTV		10,19	MR.1,500				05,1,80.		6000,3
SPI_1							BURNEL DATE:		10,349	MM_3_MRE	000,000			00,1,004		100.3
MMUART_0							BBE, NOV		ND, VOLT, ME	HMC-LMDC	000,0404		1041497,1,530-81			4893,3
MMUART 1					28		NOW, DOW		10,510,7,81	MACONTRA	dos'bran		MARANT, CTID-IN			100.3
MMUART 2						80	neer per-		10,1017,010,288		finition of		MICHT, LKD		CAULTINE	6000,3
					u	-			10,111,114,5		00/3420	10.1.10	MARANT, LTD		COLUMBIA	100.3
MMUART_3				_	10				10, VET, 28, L1		STORE FLIX CO.			_	CALL TR. BIL H	6890.3
MMUART 4					38	60 13		118,118		MACL SECON			MARANT, AND			5000,3,1
12C_0						68		118,107		MAC & MERCIN			MILLIPE & TO			6070_1. 6070_1.
						64		118,117		and constant			INCAST & KID-M			100.3
12C_1					38	82		LOB DATE:					MERGARY & TID (4)			1000.0
CAN_0						-		USE DATE:					MEARLIND			1070.3
CAN_1						60		UNE DATE:						100 0 X23.040		1000.5
GPIO_0 (Bank4 I/Os)						25		URB_DADA					MALARY 1 KID	DC 8 104-140	CARLOCTION LA DR	
					31	24		128 Sec. 14					Mariatt 1 710		DAY, 5, THRUS, 44	(and a)
GPIO_0 (Bank4 I/Os) Reset S 🔶					33	80		USB_Daffad				NUCE	100.071,000		CARLA REPORTED	1000.3
I → []					34	25		(AR DATES		MAC, A SHOLLAND		BUUR I	hitser, J. Yill	10,000,00		400.53
				- A .				own month				one a new				

By default, all peripherals are marked as unused. To include peripherals that are required in the design, select the peripheral from the left-hand side of the window and use the corresponding drop-down to assign MSS I/Os or fabric I/Os.

The I/Os associated with the following peripherals are dedicated and cannot be assigned to fabric I/Os:

- USB peripherals are dedicated in Bank 2.
- eMMC peripherals are dedicated in Bank 4.
- SD/SDIO peripherals are dedicated in Bank 4.

Note: If the I/Os for a peripheral are selected in a bank, you cannot select the same I/Os for another peripheral from the same bank. If you try, the tool generates the following warning message in the log window:

Figure 2-5. Error Message

Log Window III Messages S Errors 🗼 Warnings 🚯 Info

SERROR: IO placement errors detected in IO Configuration Tab please resolve IO overlaps highlighted in red color before running Generate.

For example, eMMC and SD cannot be used simultaneously as shown in the following figure.

Figure 2-6. Overlapping I/O Warning

eMMC	SD/SDIO			BANK	IO MUX	Package Pin	ADAC	USB	SD	٦
USB	SD	MSS I/Os Bank4	-			л	ENDIC_CLK		1D_CLE	
SD/SDIO	30	1955 1/05 Dalik4	-		1	K5	ID.04C_CMD		10,010	
Gigabit Ethernet MAC_0	VOLT PORTS	Unused	-1		2	н	EMINC_DATAB		SD_DATA0	
	VOLTPORTS	Jonuseu	-		3	14	EMDSC_DATA1	_	1D_DATA1	4
Gigabit Ethernet MAC_1	VOLT SEL is inverted	E			4	K4 J7	EDDAC_DATA3 EDDAC_DATA3		SD_DATA2 SD_DATA3	-
QSPI	VOL1_SEL is inverted	1		A 1	6	K3	ENDAC_STRB	-	1D_CD	4
SPI_0	VOLT EN is inverted	Г		N K	-	H4	ENDAC RETN		ED_WP	
SPI_1	Vocr_cris intered					36	EMDAC_DATA4		sp_pow.	۲
MMUART 0	VOLT CMD is inverted	Г				216	ENDIC_DATAS		SD_VOLT_SEL	1
MMUART 1					39	33	EMDAC_DATAS		SD_VOLT_EN	
	VOLT_DIR_0 is inverted	E			11	H2	EMDAC_DATA7		SD_VOLT_CMD_DB	R.
MMUART_2					12	HS			SD_VOLT_DIR_0	
MMUART 3	VOLT_DIR_1 is inverted	Г			10	п			1D_VOLT_DOL_1	
MANUART A					- 14	G2		USB_CLK		

2.3.1.4 I/O REFCLK

Using the **I/O REFCLK** tab, you can select electrical characteristics of the Bank 5 I/Os, as shown in the following figure. The tool generates a warning in the log window for unsupported selections.

Figure 2-7. I/O REFCLK Tab	
Clocks Fabric Interface Controllers I/O Configuration	I/O REFCLK I/O Bank4 I/O Bank2
 Bank5 Settings Bank5 Voltage VDDI = 3.3V 	
Refclk I/O Setting	
I/O Standard	LVDS25
On Die Termination for LVDS25/LVPECL33 I/O Standards	100 💌
Thevenin Termination for SSTL I/O Standards	Off 🔄
Enable Schmitt Trigger for LVTTL/LVCMOS I/O Standards	
Enable Pull Up for LVTTL/LVCMOS I/O Standards	

2.3.1.5 I/O Bank4 and Bank2

The MSS I/Os are available across Bank 4 and Bank 2. The I/O Bank4 and I/O Bank2 tabs allow you to select the electrical characteristics of the MSS I/Os.

Figure 2-8. I/O Bank4 Tab

Bank4 Settings				
and the second second second		_		
Bank4 Voltage VDD	I = 3.3V, VDDAUX=3.3 (PCI, LVTTL/LVCMOS33 IOSTD)	-		
MSSIO_0	MSSIO_0			
MSSIO_1	Persist	Г	Schmitt Trigger for 2.5 and 3.3V (Always ON for 1.2, 1.5 and 1.8V)	Г
MSSIO_2		-		-
MSSIO_3	Clamp Diode	1 c	Lock Down	10
MSSIO_4	Enable Low power mode input receiver	F	Enable Low power mode output buffer	E
MSSIO_5				-
MSSIO_6	Enable analog test port	1	Enable input receiver	٣
MSSIO_7	Output Drive (mA)	8 .	Resistor Pull	Up •
ASSIO_8				100 -
ASSIO_9				
MSSIO_10				
MSSIO_11				
MSSIO_12				
MSSIO_13				

2.3.1.6 DDR Memory

You first select the required DDR type from the **DDR Memory Type** pulldown. The DDR configuration options are available on the **DDR Topology**, **DDR Controller**, **DDR Memory Initialization**, and **DDR Memory Timing** tabs (see the following Figure 2-9).

For more information, see UG0906: PolarFire SoC FPGA DDR Memory Controller User Guide.

The **DDR Topology** tab, in the Figure 2-9 figure, controls the physical aspects of the memory, such as data and address widths, enabling of ECC and DM, and setting the clock frequency.

- For DDR3 and DDR4, the COMPONENT, UDIMM, RDIMM, LRDIMM, and SODIMM memory formats are supported.
- For LPDDR3/4, only the **COMPONENT** memory format is supported.

<u>a</u>	DDR Topology DI	DR Controller DDR Memory Initialization DDR Memory Timing
JEDEC	Topology	
# 2Gbx16		
# 2Gbx32	DQ Width	32 *
3Gbx16		
3Gbx32	Enable DM	OM +
III-4Gbx16		
8-4Gbx32	Enable ECC	Г
 6Gbx16 		
8 6Gbx32	Memory Format	COMPONENT ·
8-8Gbx16	and the second second	
8-8Gbx32	Row Address Width	16
LPDDR4-1333_8Gbx32		
LPDDR4-1600_8Gbx32 Apply	Column Address Width	10
View		1.e
Apply Delete	Bank Address Width	3
	Balik Augi ess vingui	p.
eset for module using 8Gb x 32 compone-	Clock	
DEC LPDDR4-1333 timing	C CRCA	
n DDR clock frequency 10.0	Memory Clock Frequer	(MUR) (800
ax DDR clock frequency 666.666	memory clock Prequer	ra (wurs) 1000

Figure 2-9. DDR Memory Tab

Note: Configure the DDR parameters according to the datasheet from the DDR vendor.

The **DDR Controller** tab controls the DQS Drive, ODT, Precharge look-ahead, and address ordering. **Figure 2-10. DDR Controller Tab**

I/O Bank4 I/O Bank2 DDR Memory Misc
DDR Topology DDR Controller DDR Memory Initialization DDR Memory Timing
Drive
DQ Drive 40 DQS Drive 40
ADD/CMD Drive 34 Clock Drive 34
D ODT
DQ ODT 40 -
DQS ODT 40 -
Efficiency
Enable Activate/Precharge look-ahead
Address Ordering Chip-Row-Bank-Col 💌

The **DDR Memory Initialization** tab controls the DDR mode register configuration according to the JEDEC specification. In the PolarFire SoC FPGA DDR architecture, these parameters are passed to the start-up code running on the E51 monitor core, which then performs the DDR initialization sequence and configures the mode registers.

The following figure shows the memory initialization configuration. Figure 2-11. DDR Memory Initialization
I/O Bank4 I/O Bank2 DDR Memory Misc
DDR Topology DDR Controller DDR Memory Initialization DDR Memory Timing
□ Mode Register 1
RD Pre-amble Type Static -
RD Post-amble Length 0.5*tCK
Mode Register 2
Read Latency (#RL, #nRTP) RL=14, nRTP = 8
Write Latency WL=8
Mode Register 3
Pull-up Calibration Point VDDQ/3 WR Post-amble Length 0.5*tCK

The **DDR Memory Timing** tab controls the timing parameters, which are translated to the appropriate configuration values for the DDR subsystem IP.

Figure 2-12. DDR Memory Timing	Figure	2-12.	DDR	Memory	Timing
--------------------------------	--------	-------	-----	--------	--------

DDR Topology	DDR Controller	DDR Memory Initialization	DDR Memory Timing
Timing param	eters dependent on sp	eed bin	
tRAS (ns)	42		
tRCD (ns)	18		
tRP (ns)	21		
tRC (ns)	63		
tWR (ns)	18		
tMRR (cycles)	8		
tMRW (cycles)	10		

2.3.1.7 Misc

Use the **Misc** tab to enable the following options:

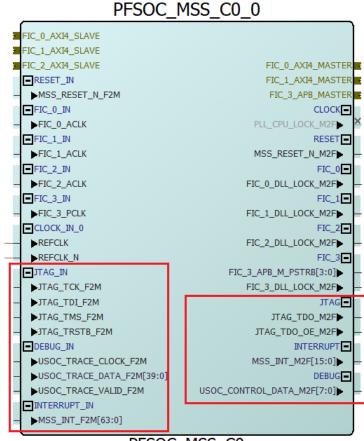
- Trace functionality
- JTAG (Debug) functionality
- Interrupts to/from MSS
- Lock down of Bank 2 and Bank 4 I/Os
- Lock down of DDR and SGMII I/Os

Figur	re 2-13.	Misc Tab						
	Clocks	Fabric Interface Controllers I/	O Configuration	I/O REFCLK	I/O Bank4	I/O Bank2	DDR Memory	Misc
E	Debug	g Trace						
	Expos	e MSS UltraSoc block to trace ports	to Fabric 🥅					
	Expos	e JTAG Trace/Debug ports to Fabri	ic 🗆					
	JTAG	Trace/Debug Control via Fabric	Г					
E	Interr	upt						
	Expos	e Interrupt ports to Fabric 🗔						
E	IOs Lo	ock Down						
	Lock [Down Bank2 IOs						
	Lock (Down Bank4 IOs						
	Lock [Down SGMII IOs						
	Lock (Down DDR IOs						

For more information, see UG0888:PolarFire_SoC_FPGA_Trace_and_Debug User Guide.

By default, these options are marked as unused. When any of the options are enabled, the corresponding ports are exposed on the MSS block (see the following figure).

Figure 2-14. PFSOC_MSS_C0_0 Jtag Trace Enabled



PFSOC_MSS_C0

3. Creating a Project and Configuring MSS

To create a project and configure MSS:

- 1. Launch the PolarFire SoC MSS Configurator (pfsoc_mss) in one of the following ways:
 - Libero SoC installation directory
 - Standalone MSS installation area
 - Windows Start menu
- 2. Create a new project using **Project > New**.
- 3. Enter a module name (for example PFSOC_MSS_C0), and then select the appropriate die and package.

Figure 3-1. MSS - Module Name Dialog Box

🔳 MSS - Mo	dule Name	?	\times
Module Name	PFSOC_MSS_C0		
Die	MPFS250T_ES		•
Package	FCVG484		•
	ОК	Can	cel

Notes: The module name you enter in this dialog box appears in the following places:

- File names of the PolarFire SoC MSS Configurator generated outputs at the specified output/generation directory.
- MSS component file(<module_name>.cxz)
- MSS XML configuration file (<module name> mss cfg.xml)
- MSS configuration file corresponding to the current MSS configuration that is generated (<module_name>.cfg)
- MSS configuration report file (<module_name>_Report.html)
- Component/module name of the MSS component (cxz) that can be imported to a Libero SoC project.

The MSS configurator tabs appear (see the following figure).

Figure 3-2. MSS Configurator Tabs

Pol	arFireSoC MSS Configurator (Pre-proc	duction)				
Projec	t Edit Help					
	i 🚰 🔚 🔂					
Clo	cks Fabric Interface Controllers I/	O Configuration I/O REFCLK I/O Bank4	I/O Ba	nk2 DDR Memory Misc		
⊟	MSS					
	MSS Reference Clock Input Source	Dedicated I/O from Bank5 (REFCLK)	•	MSS PLL clock frequency (MHz)	600.000	
	MSS CPU cores clock frequency Divider	/1	•	MSS CPU cores clock frequency (MHz)	600.000	
	MSS AXI clock frequency Divider	/2	•	MSS AXI clock frequency (MHz)	300.000	
	MSS AHB/APB clock frequency Divider	/4	•	MSS AHB/APB clock frequency (MHz)	150.000	
	Clock Sources Frequency					
	Dedicated I/O from Bank5 (REFCLK) freq	uency (MHz) 100 💌				

4. Configure Clocks, Fabric Interface Controllers, I/O Configuration, DDR Memory, and Misc settings.

- 5. Click the **Save** option to save the MSS configuration to a .cfg file.
- 6. From the Save MSS Configuration dialog box:
 - Browse to a directory and create a folder. For example, create C:\Microsemi \PFSOC_MSS_Configuration.
 - Enter a file name (for example PFSOC_MSS_C0) and click Save.
 Note: The file name you enter is for the standalone MSS project only and is not used as the component name.

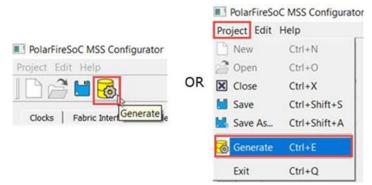
The MSS Configuration is created and saved to the file specified and the Log window shows the following message: INFO: Successfully saved MSS configuration in C:/Microsemi/PFSOC MSS Configuration/

PFSOC MSS CO.cfg file

4. Generating, Importing, and Exporting the MSS Component

4.1 Generating the MSS Component

To generate the MSS component, use the **Generate** option (see the following figure). **Figure 4-1. Generate Option**



The configuration file (module_name.xml) required for the firmware project and the configuration report file (module name.html) are also generated at this time.

The Log window shows the following messages indicating the generated files:

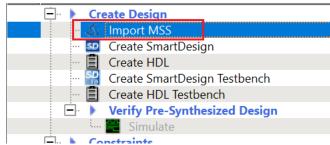
INFO: Successfully generated MSS configuration report to <code>'C:/Microsemi/PFSOC_MSS_Configuration \PFSOC_MSS_CO_Report.html'</code>

INFO: Successfully generated MSS component file to 'C:/Microsemi/PFSOC_MSS_Configuration/ PFSOC_MSS_C0.cxz'

4.2 Importing the MSS CXZ File to Libero SoC

To import the PFSOC_MSS_C0.cxz file:

Use the Import MSS option shown in the following figure.
 Figure 4-2. Import MSS to Libero



- 2. From Design Hierarchy, drag the MSS component to SmartDesign canvas.
- 3. Build the hierarchy.

Note: Any changes required in the MSS configuration must be performed in the PolarFire SoC MSS Configurator, and the updated MSS CXZ file must be re-imported and used in Libero SmartDesign.

4.3 Importing the MSS XML File to SoftConsole

Copy the XML file from:

<\$Directory>:/Microsemi/PFSOC_MSS_Configuration/PFSOC_MSS_C0_mss_cfg.xml

to:

<\$Installation Directory>:\Microchip\<\$SoftConsole_Workspace>\Project_Name\src\platform\config \xml

Note: This step can also be performed using the Import option from SoftConsole.

4.4 Exporting the FPGA Design Hardware Platform Information

When using PolarFire SoC, the overall application runs an embedded software application on the RISC-V cores that may use the FPGA fabric to expand the number of I/O peripherals, accelerate software functions using FPGA logic, or control FPGA fabric functions. In these cases, the processor communicates with the FPGA fabric via the MSS Fabric Interface Controllers (FIC) and interrupt ports. The embedded software application must contain the following information to establish this communication properly:

- Fabric blocks like LSRAM, DMA Controller, and PCIe are connected to the AXI interconnect IP on the Fabric side. MSS communicates with these fabric blocks via Fabric Interface Controllers, which connects to the AXI Interconnect IP. The memory addresses of these fabric blocks are specified in the AXI Interconnect IP Configurator. These memory addresses must be specified in the software application.
- In the Libero SoC design, the user must enable the required MSS interrupt ports and other interrupts can be grounded. The corresponding Interrupt Request (IRQ) handler routines must be invoked in the software application for interrupt handling.

Libero SoC v12.5 does not export the FPGA fabric peripheral memory map, interrupt mapping, or peripheral clock frequencies. Therefore, add this information manually in your embedded software projects. For example, if fabric blocks such as LSRAM and DMA Controller are used in the design and interfaced with the MSS through a FIC, then the memory addresses of these fabric blocks must be specified in the user application code for accessing them from MSS.

5. Simulating an FPGA Design Interacting with MSS

The MSS simulation model has been designed to verify the connectivity to the MSS has been properly established with the FPGA fabric logic.

The MSS Simulation model can be used to verify:

- The Fabric—MSS connectivity using the Fabric Interface Controllers (FICs).
- The Fabric—MSS interrupt (M2F and F2M) interface.

For information about how to set up and run the simulation for the PolarFire SoC MSS, see UG0926 User Guide PolarFire SoC FPGA MSS Simulation.

6. Programming the Application Bitstream

To program the application bitstream:

- 1. Use Libero SoC or FlashProExpress to program the FPGA fabric array, sNVM, eNVM and any security settings.
- 2. Use Libero SoC to program any eNVM client.

Note: SoftConsole must be used to program the Boot mode.

Alternatively, you can also perform the following steps:

- 1. Use SoftConsole to program the eNVM with the First Stage Boot image.
 - 1.1. Select the project you want programmed to eNVM in SoftConsole's **Project Explorer** pane.
 - 1.2. Click the **PolarFire SoC Boot Mode 1** external tool.

Programming progress messages appear in the Console.

For more information, see *PolarFire SoC Software Development and Tool Flow User Guide*.

7. Sample Project

To view a sample project, see AC489: Building the PolarFire SoC MSS Design .

8. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision	Date	Description
А	09/2020	Initial Revision

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