CN20006: RTG4 Family Important Changes

May 6. 2020

This document describes the following three changes to the RTG4 product family.

Notification	Description	Required Action
CN20006.1	“Configure I/O States During JTAG Programming” Libero Tool Causes Loss of Programming Configurations for RTG4 FPGAs	Upgrade to Libero SoC v12.4.
CN20006.2	RTG4 New Global Net Clock Jitter	Read CN20006.2 details.
CN20006.3	RTG4 FPGA Datasheet Updates	Upgrade to Libero SoC v12.4 and review the latest RTG4 datasheet.

CN20006.1: “Configure I/O States During JTAG Programming” Libero Tool Causes Loss of Programming Configurations for RTG4 FPGAs

Description

Specific Libero SoC configuration options can result in a loss of user programming settings. Libero SoC v12.4 (April 2020 release) includes an update to prevent the I/O states during programming the tool from corrupting the bitstream and programming settings.

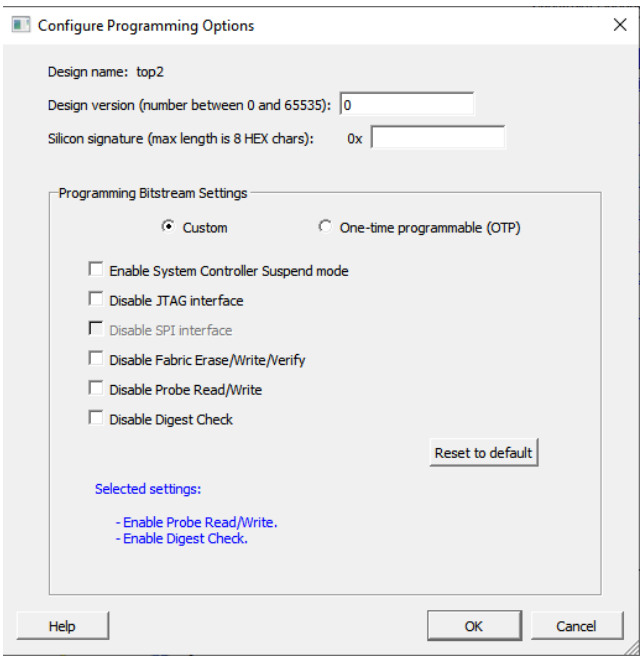
In Libero SoC v12.0 to v12.3, using the configuration tool to “Configure I/O States During JTAG Programming” can cause a loss of user programming settings selected via “Configure Programming Options”, “Configure Action/Procedure” for the “Run Programming Action” step, and “Generate Bitstream” options.

When operating an RTG4 device, if System Controller Suspend mode is selected, this issue could permanently prevent the device from exiting System Controller Suspend mode, and permanently lose the capability of reprogramming the device. We recommend upgrading to Libero SoC v12.4.

Application Impact

- Issue only exists in Libero SoC v12.0 to v12.3, and does not exist in 11.x versions of Libero SoC.
- User settings for the programming options and bitstream options could be corrupted.
- If System Controller Suspend Mode (SCSM) is enabled (which automatically disables the JTAG interface), the bitstream generated after configuring I/O states during programing can prevent all further JTAG access, and thus permanently prevent further device programming with Scan Chain failure and "TDO stuck at {0,1}" msg.
- If Fabric Erase/Write/Verify is disabled, the bitstream generated after configuring I/O states during programing can permanently prevent further JTAG programming with the “Operation has been disabled by programming bitstream settings” message.
- If Probe Read/Write is disabled, the bitstream generated after configuring I/O state during programming can prevent fabric (probe and SRAM) debug using SmartDebug, causing the following messages:
    - "Live probe is locked by security or array is not programmed.", when using LiveProbe.
    - "Active probe is locked by security or array is not programmed.", when using ActiveProbe.
    - "Operation failed due to active security protection.", when access Fabric SRAM.
- If Digest Check is disabled, the bitstream generated after configuring I/O state during programming can cause Digest Check operation to fail with the “Fabric digest check is disabled.” message.
- For RTG4, this issue only occurs if running “Configure I/O States During JTAG Programming” in Graphical User Interface (GUI) mode.
- There is no issue if the “Configure I/O States During JTAG Programming” GUI is not used, no issues in Tcl scripted mode.

Figure 1 • RTG4 Programming Options GUI



Required Action

Do not program any further RTG4 devices with programming files (Libero SoC v12.0 to v12.3) using I/O states during programming GUI combined with the programming options listed above. Upgrade to Libero SoC v12.4, observe that all "Generate" and "Export" programming steps in the design flow will be invalidated, then re-run I/O States GUI and re-configure Programming/Bitstream options prior to Generating and Exporting new bitstreams.

Part Numbers Affected

For list of affected part numbers, see Appendix A.

CN20006.2: RTG4 New Global Net Clock Jitter Specification

Description

The SET-mitigated global clocking resources on RTG4 FPGAs are susceptible to clock jitter. The maximum period jitter for RTG4 global nets will be updated in *RTG4 FPGA Datasheet (DS0131)* revision 7 and *RTG4 Clocking Resources User Guide (UG0586)* revision 9 to include information on the global clock net jitter.

Two distinct factors contribute to increased global clock net jitter. Only one of these effects is present at any time. These are:

- Clock jitter induced by large amounts of logic simultaneously toggling at the resonant frequency of the Power Delivery Network (PDN), which can be in the range of 10 MHz to 40 MHz, depending on the board design.
- Clock jitter introduced by the response of the PDN to large transient currents under extreme design toggle rates, regardless of clock frequency.
- Flip-flop toggle rate is measured as a percentage of the 151,824 total flip-flops in the RTG4 FPGAs that are switching simultaneously at a given clock edge. Typically flip-flop toggle rates are less than 25%.

The effect of toggle rate on max clock jitter period is shown in the following table.

Table 1 • RTG4 Global Network—Max Period Jitter (Peak-to-Peak) Specification

Speed Grade	FF Toggle % (of Total FFs in Device)			Units
	15%	25%	50%	
–1	200	250	400	ps
STD	300	400	650	ps

Note: The 50% FF Toggle % datapoint is only shown to illustrate the impact to the global net clock jitter. 50% simultaneous FF toggle rate per clock edge (out of the 151,825 FFs in the device) is considered extreme and not typical FPGA design behavior.

Application Impact

If the RTG4 user design has successfully passed functional and system testing over full operating conditions, then there is no application impact. Furthermore, if the design's FF toggle rate is low and the Static Timing Analysis (STA) performed already accounts for sufficient clock jitter, then there is no application impact.

Designs with high flip-flop toggle rates could see higher than expected clock jitter. If the clock jitter is not factored into the static timing analysis of the design, then there is a potential for inadequate STA leading to uncaught timing violations and possible design malfunction.

Required Action

For designs that have already successfully completed functional and system testing over full operating conditions, no action is required.

For designs that have not yet successfully completed functional and system testing over full operating conditions, customers are advised to perform the following steps.

- Review the updated documentation—*RTG4 FPGA Datasheet (DS0131)* revision 7 and *RTG4 Clocking Resources User Guide (UG0586)* revision 9, once published.
- Re-run static timing analysis after accounting for clock jitter from all sources to ensure timing closure. Use the following table to determine how to factor clock jitter into STA.

Table 2 • How to Factor Clock Jitter into STA

Clock Domain Flip-Flop Toggle Rate	CCC/PLL Used	Jitter to Use in STA
50% or less	Yes	Whichever is largest of global net clock jitter or CCC/PLL output clock jitter.
	No	Whichever is larger of global net clock jitter or input buffer clock jitter.
Greater than 50%	Yes	We do not recommend operating the device with total simultaneous FF toggle rate >50%.
	No	

- If flip-flop toggle percentage is 25% or greater then measure V_{DD} ripple and clock jitter directly, at package pins.
- Ensure that the RTG4 V_{DD} supply is maintained within ±5% of 1.2 V, including DC variation and V_{DD} ripple during design operation.

Part Numbers Affected

For list of affected part numbers, see Appendix A.

CN20006.3: RTG4 FPGA Datasheet Updates

Description

The *RTG4 FPGA Datasheet (DS0131)* will be updated to revision 7. Customers need to review the following changes and adhere to updated specifications:

- SERDES specification tables have been expanded to include generic specifications and protocol specific characteristics.
- RTG4 global net clock jitter specification has been added.
- List maximum operating frequency of APB configuration interface for fabric components such as FDDR, SerDes, and Dynamic CCC.

Application Impact

There will be no application impact if Microchip's customers adhere to the updated specifications. Furthermore, there is no impact to designs that have successfully completed full functional and environmental qualification testing with previously existing datasheet clock jitter values entered into SmartTime Static Timing Analyzer using appropriate SDC constraints.

Required Action

- Customers must review changes and assess whether designs adhere to the updated specifications.
- Upgrade to the latest version of Libero SoC available.
- Microchip recommends conducting a design review to ensure the design timing analysis accounts for clock jitter and the design adheres to the latest specifications of *RTG4 FPGA Datasheet (DS0131)* revision 7 and *RTG4 Clocking Resources User Guide (UG0586)* revision 9 and later.

Part Numbers Affected

For list of affected part numbers, see Appendix A.

Appendix A

The following table lists the affected part numbers.

Microsemi Part Number	DLA SMD Number
RT4G150-CG1657B	5962-1620801QXF
RT4G150-1CG1657B	5962-1620802QXF
RT4G150-LG1657B	5962-1620803QZC
RT4G150-1LG1657B	5962-1620804QZC
RT4G150-CG1657E	5962-1620805QXF
RT4G150-1CG1657E	5962-1620806QXF
RT4G150-LG1657E	5962-1620807QZC
RT4G150-1LG1657E	5962-1620808QZC
RT4G150-CG1657V	5962-1620809VXF
RT4G150-1CG1657V	5962-1620810VXF
RT4G150-LG1657V	5962-1620811VZC
RT4G150-1LG1657V	5962-1620812VZC
RT4G150-CQ352B	5962-1620813QYC
RT4G150-1CQ352B	5962-1620814QYC
RT4G150L-CG1657B	5962-1620815QXF
RT4G150L-LG1657B	5962-1620816QZC
RT4G150L-CQ352B	5962-1620817QYC
RT4G150L-CG1657E	5962-1620818QXF
RT4G150L-LG1657E	5962-1620819QZC
RT4G150L-CG1657V	5962-1620820VXF
RT4G150L-LG1657V	5962-1620821VZC
RT4G150-1CB1657PROTO	
RT4G150-1CG1657PROTO	
RT4G150-1CQ352PROTO	
RT4G150-1LG1657PROTO	

Microsemi Part Number	DLA SMD Number
RT4G150-CB1657PROTO	
RT4G150-CG1657PROTO	
RT4G150-CQ352PROTO	
RT4G150-LG1657PROTO	
RT4G150-1CG1657R	
RT4G150-1CQ352R	
RT4G150-1LG1657R	
RT4G150-CG1657R	
RT4G150-CQ352R	
RT4G150-LG1657R	
RT4G150-1CG1657M	
RT4G150-1CQ352M	
RT4G150-1LG1657M	
RT4G150-CG1657M	
RT4G150-CQ352M	
RT4G150-LG1657M	
RT4G150-FCG1657M	
RT4G150-1FCG1657M	
RT4G150-FCG1657ES	
RT4G150-1FCG1657ES	

Contact Information

If you have any questions about this subject, contact Microsemi Technical Support department by using the support portal at *https://soc.microsemi.com/Portal/Default.aspx*.

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