Synopsys®, Inc.
690 East Middlefield Road
Mountain View, CA 94043 USA
Website: www.synopsys.com

Synopsys® FPGA Design Microsemi Edition Release Notes

Includes Synplify Pro® and Identify®
Version P-2019.03M-SP1-1, January 2020

Release Note Topics

About the Release

This P-2019.03M-SP1-1 release includes software features and enhancements for the Synplify Pro® and Identify Microsemi Edition products. For the complete summary of features and enhancements supported in this release, see Feature and Enhancement Highlights below.

Feature and Enhancement Highlights

The following table summarizes the supported features and enhancements:

Feature	Description
Features in the P-2019.03M-SP1 Release	
FlashPro-6 Programmer Support in Identify	Identify now supports FlashPro-6 Programmer (ID: FFFFFFFF), along with FlashPro-3/4/5, on Windows as well as Linux platforms.
Asymmetric RAM	Asymmetric RAM inference is supported for the PolarFire RAM1K20 macro. See *Reference->Designing with Microsemi->Microsemi RAM Implementations->PolarFire Asymmetric RAM Support*
Features in the P-2019.03 Release	
VHDL 2019 Conditional Analysis *Beta*	Support for conditional analysis of the VHDL code, using the VHDL 2019 language updates (VHDL 2019 LRM, section 24.2). The following keywords are currently supported: ‘if, ‘else, ‘elsif, and ‘end. See *Command Reference->User Interface Commands ->Implementation Options Command->VHDL Panel*

Identify Tool Device Support

The Identify tool supports the device families shown in the table below. You must select devices from the synthesis tool, which get passed to the Identify Instrumentor in the synthesis project file. If you specify a library from the synthesis tool that is not supported in the Identify tool, then this results in a device not supported message when launching the Identify Instrumentor.

Microsemi
IGLOO2
PolarFire
RTG4
SmartFusion2

Recommended Versions of Compatible Tools

The FPGA design tools are tested with specific versions of other compatible Synopsys and third-party tools. The recommended versions of these tools are listed below.

Compatible Versions of Synopsys Tools

The table lists the recommended version for VCS:

Tool	Recommended Version
VCS	O-2018.09

Platforms

The software is supported on the platforms listed below:

Windows[1]	• Windows 10 Professional or Enterprise (64-bit) • Windows 8.1 Professional or Enterprise (64-bit) • Windows 7 Professional or Enterprise (64-bit) • Windows Server 2016 (64-bit) • Windows Server 2012 R2 (64-bit) • Windows Server 2008 R2 (64-bit)
Linux	All Linux platforms require 32-bit compatible libraries. • CentOS 6.6 or later/7.1 or later (64-bit) • Red Hat Enterprise Linux 6.6 or later/7.1 or later (64-bit) • SUSE Linux Enterprise 11-SP4/12 or later (64-bit)[2]

1. This is the final release that supports Windows 8.1 platform.
2. The final release supporting SUSE Linux Enterprise 11-SP4 is September 2019.

Documentation

The following documents are included with the Synopsys FPGA synthesis product.

Document	Access
User Guide	Online help, PDF
Reference Manual	Online help, PDF
Attribute Reference Manual	Online help, PDF
Command Reference Manual	Online help, PDF
Language Support Reference Manual	Online help, PDF
Messages Reference Manual	Online help
Identify Instrumentor User Guide	Online help, PDF
Identify Debugger User Guide	Online help, PDF
Identify Debugging Environment Reference Manual	Online help, PDF

Known Problems and Solutions

The current known problems in the tool are divided into the following categories:

- FPGA Synthesis Known Problems and Solutions, on page 4
- FPGA and Identify Platform-Specific Known Problems and Solutions, on page 6
- Identify Tool Known Problems and Solutions, on page 7

FPGA Synthesis Known Problems and Solutions

The following problem applies to supported features in the Synplify Pro product.

Windows Certificate Installer Message

A Synopsys Common Licensing (SCL) change was issued by Synopsys in December 2018, that contained Tamper Resistant Licensing (TRL) cryptography. This change was implemented as part of the ongoing process of enhancing the security of the Synopsys software. The Installer checks if the required certificates are installed and issues a message if an update is needed.

Solution: Go to the link below and follow the instructions to update the required certificates: https://www.synopsys.com/certificates

Software Does Not Open After Installation

If your software does not open after installation, check if you need to update your SCL certificates. A Synopsys Common Licensing (SCL) change was issued by Synopsys in December 2018, that contained Tamper Resistant Licensing (TRL) cryptography. This change was implemented as part of the ongoing process of enhancing the security of the Synopsys software.

Solution: To find out if you are missing any required certificates, go to the /bin directory of your installation and run the following:

```
whatscl.exe  --check-cert
```

If certificates are listed as missing, go to the link below and follow the instructions to update the required certificates.
https://www.synopsys.com/certificates

Change in Behavior for Sequential Optimizations

In the N-2018.03-SP1 release, the default behavior changed in the RAM implementation. If sequential optimizations are disabled (set_option no_sequential_opt 1), you may see Block RAM utilization increase (LUT utilization may decrease) in area estimation and in FPGA synthesis.

Default Behavior:

Version	RAMs with read address registered	RAMs with output registered
N-2018.03 or older	Block RAM	LUT RAM (select RAM)
N-2018.03-SP1 or later	Block RAM	Block RAM

Solution: A new option has been added to control the behavior of Block RAM packing when disable sequential optimization is ON.

```
set_option no_sequential_opt_bram_mapping inreg|both
```

inreg - Read address registered RAMs will be packed to Block RAMs (prior default behavior).

both - (Default) Both read address registered and output registered RAMs will be packed to Block RAMs.

The following is a list of what is impacted by disabling sequential optimization. Use `no_sequential_opt 1` understanding its impact.

- If you are disabling sequential optimizations with GSV to obtain better naming correlation, you may not see RAM output registers that were seen in the GSV database in prior versions.
- No gated clock conversion and no ICG latch removal
- May increase area
- Limited design performance
- May increase congestion

Error when Implementing Safe FSM on Microsemi RTG4 Designs

You get a DE108 error in Microsemi RTG4 designs when safe FSMs are specified by setting the syn_encoding=safe or syn_safe_case=true attributes, or by enabling the Preserve and Decode Unreachable States option in the Implementation Options->High Reliability dialog box.

Solution: You do not need to implement safe FSMs with this family, because it already has TMR on registers. You can downgrade the error to a warning with the message_override -warning DE108 Tcl command. Once the error is downgraded, the tool continues with synthesis and implements safe logic for FSMs on RTG4.

Compiler is unable to extract a state machine (CL317)

In rare cases, if the compiler is unable to extract a safe state machine then the tool issues the following warning message:

@W:CL317 : debounce.vhd(50) | State machine with safe encoding was not inferred as requested. Check the state machine logic.

This occurs when the syn_encoding directive is set to safe and the VHDL Default Enum Encoding option is set to onehot.

Solution: Verify the state machine logic and use one of the following options:

- Select a different safe encoding option or let the tool set a default option. To choose a different or default encoding option:

  From the GUI, go to Implementation Options -> VHDL-> Default Enum Encoding.
  Using TCL script:

  ```
  set_option -default_enum_encoding default
  ```

- Enable the Preserve and Decode Unreachable States option in the High-Reliability tab.
- Make sure the state machine has when others clause specified in the VHDL case statements.

Locked FSMs

FSMs are locked in an illegal state.

Solution: If you have uninitialized FSMs, turn off the FSM compiler throughout the synthesis flow.

FPGA and Identify Platform-Specific Known Problems and Solutions

The following platform-specific problems apply to supported features in the Synplify Pro and Identify tools.

False Flagging of Product Executables as Malware

On Microsoft Windows, some endpoint protection systems could flag executables as similar to malware threats. These are false positives, as Synopsys thoroughly scans all released files.

Solution: If your endpoint system blocks a Synopsys file, white-list it so that it is not flagged. Also, open a CASE so that Synopsys can investigate.

The encryptP1735.pl script is Incompatible with Windows DOS or PowerShell

If the encryptP1735.pl encryption script is run on Windows from DOS or PowerShell, it might fail.

Solution: Run the script on Linux. To run it on Windows, use a UNIX-like environment such as Cygwin.

Adobe Reader Error About Opening PDF Files (Linux)

Random links in the document PDFs on the Linux platform do not work. Adobe Reader generates an error message about not being able to find the appropriate PDF file. This does not happen on Windows platforms.

Solution: This is a problem with Adobe Reader on Linux. Work around it by first opening all the PDFs, and then trying the link again.

GUI Processing Can Fail on Windows 7 for the Synthesis Tool

The synthesis tool GUI might intermittently stop responding on Windows 7.

Solution: To resolve this issue, apply the hotfix from Microsoft by going to support.microsoft.com/kb/2718841/.

Identify Tool Known Problems and Solutions

The following problems are specific to the Identify instrumentor and Identify debugger tools.

No DRC Check for Technology-Specific Primitive Instances

If instantiated technology-specific primitives have instrumented ports or signals, the tool adds a fanout to that port or signal and does not run DRC (design rule check) for that technology. This may result in a rule violation and a consequent error during synthesis, placement, or routing. Avoid the error by ensuring that the design is instrumented in accordance with the DRC rules for that technology.

Solution: Users must ensure that the design is instrumented in such a way that it does not violate the DRC rule for that technology.

Incremental Debug Points from Previous Release Cannot be Used

Attempting to open an incremental debug specification created from a previous Identify release results in an assertion error.

Solution: The incremental debug points from the previous release cannot be used, and new debug points must be defined using this release.

Context-Sensitive Help May not Display Correct Help Page on Linux

When using context-sensitive help (F1) for the Identify tool on Linux, help does not open to the expected page.

Solution: Use the table of contents, global index, or the online help search mechanism to access the correct help page.

Limitations

The current limitations in the tool are divided into the following categories:

FPGA Synthesis Limitations

The following limitations apply to supported features in the Synplify Pro product.

Fault Injection Feature for Mixed HDL Designs

When using fault injection techniques for mixed HDL designs, RTL instrumentation is not supported. Only SRS instrumentation is supported for mixed HDL designs.

Page Could Not Be Found Message When Invoking Online Help

When online help is first invoked, it creates a cached version of the compiled help file in a local hierarchy to allow you to save preferences, bookmarks, and full-text search information. This cached version records the path to the installed version. If the same product version is subsequently re-installed in a new directory, invoking online help displays a message, "*The page could not be found*," because the cached version does not recognize the path to the re-installed product.

Solution: Go to the platform-specific directory with the cached help files:

Windows:
C:\Users*username*\AppData\Local\assistant\Synopsys\Synplify\product

Linux:
~/.local/share/data/assistant/Synopsys/Synplify/

- Delete any/all directories named “online*” directories from the cache directory.
- Restart help. This creates a new cache, and correctly displays the online help.

Online Search Does Not Handle Hyphens as Expected

If the search term includes a hyphen (for example, *byte-enable*), online help does not produce the search hits you expect, because it searches for *byte* and *enable*. This limitation does not affect underscores. It is limited to online help search and does not affect search in PDF documents.

It is also limited to online help search and does not affect search in PDF documents.

Solution: Here are some workarounds:

- Basic Search—Use the \ character before the hyphen to escape the hyphen
- Try the index
- Basic Search—Try using the * wildcard
- Basic Search, and Advanced Search with exact term—Try the term with a space in place of the hyphen

Crossprobing Source Code Files Created with Third-Party Editors

When using source code files created with third-party editors, you sometimes cannot crossprobe to the correct line number in the source file.

Solution: Open the file in the FPGA synthesis tool text editor.

Editing Externally Created Project (prj) Files

If Tcl commands or script files were used to build your project, you might not be able to save the project file from the synthesis GUI in downstream tools, because they contain hard-coded file paths.

Solution: Generally, use the same method to save a project as you did to create the project. In this case, save the project file to an external text editor and not in the project GUI.

Identify Tool Limitations

The following limitations are specific to the Identify tools.

Verilog/SystemVerilog Limitations with Imported Verdi Signals

There are some Verilog/SystemVerilog limitations when signals are imported directly from the Verdi® platform:

- Enums with syn_enum_encoding attribute are not supported for debug selection. If present, they can impact data expansion.
- Conditional expression settings for unions are represented either as a serialized bit vector or as hex/integer, with the bit width representing the maximum available bit width among all union members. A future enhancement will make it possible for expressions to target individual union members.
- SystemVerilog interface constructs are not supported.

VHDL Limitations with Imported Verdi Signals

There are some VHDL limitations when the essential signals are imported from the Verdi platform:

- Boolean vector representation in the Identify-generated FSDB is different from the VCS-generated FSDB, but does not have any known impact during the data expansion.
- Record elements are represented in reverse order in the Identify-generated FSDB. This reversal does not have any known impact during data expansion.
- Generate statements are not supported.