LX4580

24 Channel Data Acquisition System with Synchronized Motor Control Interface

Description

The LX4580 Actuation System Manager AFE contains a combination of functions for monitoring sensors, and for controlling motion. The LX4580 interfaces with a microprocessor system or an FPGA to execute digital control system algorithms in real time. The robust sensor interfaces are designed to operate in a DO-160 aircraft environment. The microprocessor / FPGA interface is based on an ECC code over a redundant slave SPI or UART interface. The LX4580 is typically powered from +15V and generates its own intermediate power rails.

The LX4580 offers a register file model to read / write information.

Five temperature sensor monitors, a voltage monitor and three pressure sensor monitors are provided. Each sensor has a dedicated instrumentation amplifier. Each temperature sensor has a programmable current source and each pressure sensor has a power off switch. All nine amplifiers use a common MUX and a set of two SAR ADCs.

Up to four LVDT/resolver sensor outputs and 5 current sense channels can be monitored using the LX4580; each of these two types of sensors have a dedicated second order sigma delta modulator with a sample rate up to 2MHz. The LVDT channels can additionally provide the RMS value of the respective input signal. Two efficient full bridge drivers are provided to drive two independent LVDT primaries. These can be used to drive a PWM modulated sine wave with external filtering or any desired waveform from a DDS-type table

There are several digital IOs that are used to signal fault conditions, to synchronize the external control with the PWM switching cycles and LVDT driver programmed waveform and to read other digital output sensors such as Hall effect sensor outputs. There are 8 PWM outputs used to drive upper and lower MOSFET gate drivers in a four half-bridge application (e.g. motor and solenoid drive). The LX4580 default configuration (calibration data and communications parameters) is stored into an internal OTP memory and is loaded at power-up into the configuration registers. The configuration can be loaded via the SPI or UART interface by the external processing.

The analog inputs, LVDT drivers and the PWM outputs can be cold spared allowing two LX4580s to operate in a redundant configuration with one powered on while the other is off (with RESET asserted).

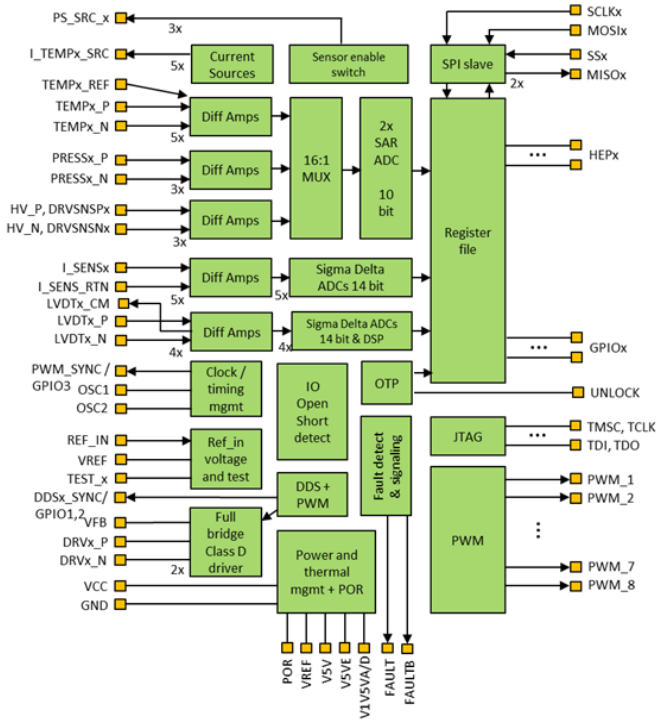
The package is a 144-pin LQFP. The chip operates over a -55°C to 110°C temperature range. Consult factory for higher temperature operation.

Features

- Redundant dual-SPI or dual-UART serial interfaces
- 5 PRT100 or PRT1k temperature sensor interfaces
- 3 pressure sensor (or other 4-20mA) interfaces
- 2 LVDT drivers and driver monitors
- 4 LVDT monitor differential pairs with instantaneous and RMS outputs
- 5 current sense interfaces
- 1 differential voltage measurement interface
- 3 Hall effect proximity sensor inputs
- 8 PWM outputs
- Integrated regulators for internal circuits and sensors
- 9 register programmable GPIOs
- Advanced fault detection and signaling
- JTAG scan and test interface
- Small 144 pin LQFP pin package

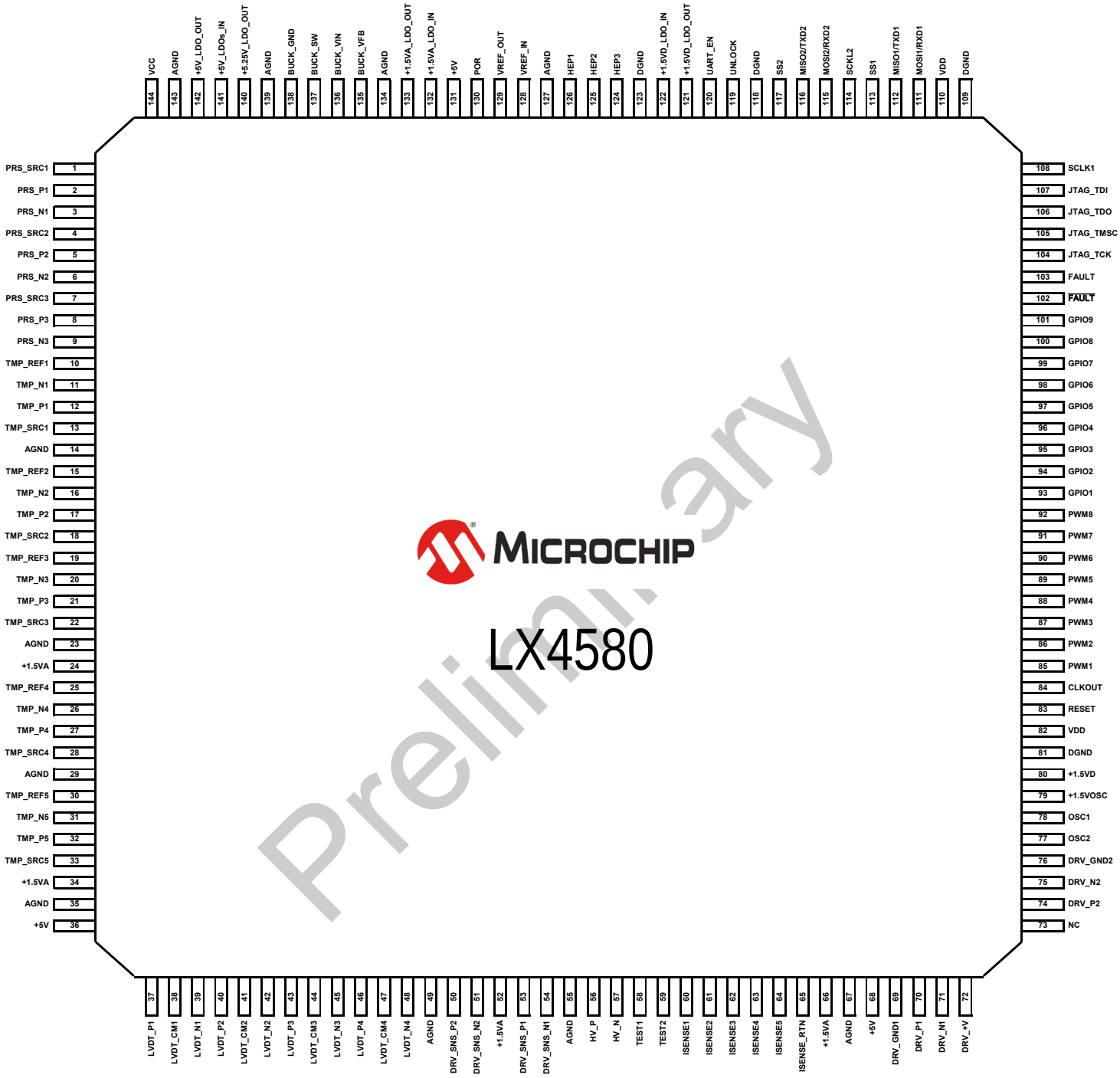
Applications

- Motor and actuator servo control for industrial, aviation, and guidance systems



Top-Level Block Diagram

1 LQFP-144 Pin Configuration and Pinout



Notes

- The LX4580 has an exposed pad

2 Ordering Information

Operating Temperature	Package Type	Package	Part Number	Flow	Shipping Type
-55°C to 110°C	Quad Flat Pack	LQFP-144	LX4580	JEDEC	Tray

3 Pin Numbering and Pin Descriptions

Pin	Name	Pin Type	Pin Function	Description
1	PRS_SRC1	Power Output	Pressure Sensor 1 Voltage Source	Protected, register-enabled VCC power to pressure sensor 1
2	PRS_P1	Analog Input	Pressure Sensor 1 Amplifier +ve Input	Non-inverting input for pressure sensor 1 differential amplifier
3	PRS_N1	Analog Input	Pressure Sensor 2 Amplifier -ve Input	Inverting input for pressure sensor 1 differential amplifier
4	PRS_SRC2	Power Output	Pressure Sensor 2 Voltage Source	Protected, register-enabled VCC power to pressure sensor 2
5	PRS_P2	Analog Input	Pressure Sensor 1 Amplifier +ve Input	Non-inverting input for pressure sensor 2 differential amplifier
6	PRS_N2	Analog Input	Pressure Sensor 2 Amplifier -ve Input	Inverting input for pressure sensor 2 differential amplifier
7	PRS_SRC3	Power Output	Pressure Sensor 3 Voltage Source	Protected, register-enabled VCC power to pressure sensor 3
8	PRS_P3	Analog Input	Pressure Sensor 1 Amplifier +ve Input	Non-inverting input for pressure sensor 3 differential amplifier
9	PRS_N3	Analog Input	Pressure Sensor 2 Amplifier -ve Input	Inverting input for pressure sensor 3 differential amplifier
10	TMP_REF1	Analog Input	Temperature Sensor 1 external reference resistor	Connect a precision reference resistor from TMP_REF1 to AGND pin 14 to develop the positive measurement voltage for temperature sensor 1. The current set by the I_TEMP1_SRC current DAC passes from the TMP_SRC1 pin through the remote resistive temperature sensor and back through the resistor at TMP_REF1 to AGND
11	TMP_N1	Analog Input	Temp Sensor 1 Amplifier -ve Input	Inverting input for temperature sensor 1 differential amplifier. Connect to one end of the remote resistive temperature sensor and to TMP_REF1 either locally or at the temperature sensor for 2-wire or 4-wire measurement respectively
12	TMP_P1	Analog Input	Temp Sensor 1 Amplifier +ve Input	Non-inverting input for temperature sensor 1 differential amplifier Connect to one end of the remote resistive temperature sensor and to TMP_SRC1 either locally or at the temperature sensor for 2-wire or 4-wire measurement respectively
13	TMP_SRC1	Analog Output	Temperature Sensor 1 Source	Programmable current source for temperature sensor 1 set by the I_TEMP1_SRC current DAC
14	AGND	Power	Temperature Sensor 1 & 2 GND	Connect to analog ground and use as star ground point for the reference resistors at TMP_REF1 and TMP_REF2
15	TMP_REF2	Analog Input	Temperature Sensor 2 external reference resistor	Connect a precision reference resistor from TMP_REF2 to AGND pin 24 to develop the positive measurement voltage for temperature sensor 2. The current set by the I_TEMP2_SRC current DAC passes from the TMP_SRC2 pin through the remote resistive temperature sensor and back through the resistor at TMP_REF2 to AGND
16	TMP_N2	Analog Input	Temp Sensor 2 Amplifier -ve Input	Inverting input for temperature sensor 2 differential amplifier. Connect to one end of the remote resistive temperature sensor and to TMP_REF2 either locally or at the temperature sensor for 2-wire or 4-wire measurement respectively
17	TMP_P2	Analog Input	Temp Sensor 2 Amplifier +ve Input	Non-inverting input for temperature sensor 2 differential amplifier Connect to one end of the remote resistive temperature sensor and to TMP_SRC2 either locally or at the temperature sensor for 2-wire or 4-wire measurement respectively
18	TMP_SRC2	Analog Output	Temperature Sensor 2 Source	Programmable current source for temperature sensor 2 set by the I_TEMP2_SRC current DAC
19	TMP_REF3	Analog Input	Temperature Sensor 3 external reference resistor	Connect a precision reference resistor from TMP_REF3 to AGND pin 34 to develop the positive measurement voltage for temperature sensor 3. The current set by the I_TEMP3_SRC current DAC passes from the TMP_SRC3 pin through the remote resistive temperature sensor and back through the resistor at TMP_REF3 to AGND
20	TMP_N3	Analog Input	Temp Sensor 3 Amplifier -ve Input	Inverting input for temperature sensor 3 differential amplifier. Connect to one end of the remote resistive temperature sensor and to TMP_REF3 either locally or at the temperature sensor for 2-wire or 4-wire measurement respectively
21	TMP_P3	Analog Input	Temp Sensor 3 Amplifier +ve Input	Non-inverting input for temperature sensor 3 differential amplifier Connect to one end of the remote resistive temperature sensor and to TMP_SRC3 either locally or at the temperature sensor for 2-wire or 4-wire measurement respectively
22	TMP_SRC3	Analog Output	Temperature Sensor 3 Source	Programmable current source for temperature sensor 3 set by the I_TEMP3_SRC current DAC
23	AGND	Power	Temperature Sensor 3 & 4 GND	Connect to analog ground and use as star ground point for the reference resistors at TMP_REF3 and TMP_REF4. All AGND and GND pins must be used and connected together
24	+1.5VA	Power	+1.5VA Analog Supply	+1.5V power rail for analog core. Connect this pin and pins 34, 52, 66, and 79 to the output of the internal +1.5V linear regulator at +1.5VA_LDO_OUT pin 133. Bypass close to the pin with a 100nF capacitor to AGND pin 23
25	TMP_REF4	Analog Input	Temperature Sensor 4 external reference resistor	Connect a precision reference resistor from TMP_REF4 to AGND pin 44 to develop the positive measurement voltage for temperature sensor 4. The current set by the I_TEMP4_SRC current DAC passes from the TMP_SRC4 pin through the remote resistive temperature sensor and back through the resistor at TMP_REF4 to AGND

Pin	Name	Pin Type	Pin Function	Description
26	TMP_N4	Analog Input	Temp Sensor 4 Amplifier -ve Input	Inverting input for temperature sensor 4 differential amplifier. Connect to one end of the remote resistive temperature sensor and to TMP_REF4 either locally or at the temperature sensor for 2-wire or 4-wire measurement respectively
27	TMP_P4	Analog Input	Temp Sensor 4 Amplifier +ve Input	Non-inverting input for temperature sensor 4 differential amplifier Connect to one end of the remote resistive temperature sensor and to TMP_SRC4 either locally or at the temperature sensor for 2-wire or 4-wire measurement respectively
28	TMP_SRC4	Analog Output	Temperature Sensor 4 Current Source	Programmable current source for temperature sensor 4 set by the I_TEMP4_SRC current DAC
29	AGND	Power	Temperature Sensor 5 GND	Connect to analog ground and use as star ground point for the reference resistor at TMP_REF5. All AGND and GND pins must be used and connected together
30	TMP_REF5	Analog Input	Temperature Sensor 5 external reference resistor	Connect a precision reference resistor from TMP_REF5 to AGND pin 54 to develop the positive measurement voltage for temperature sensor 5. The current set by the I_TEMP5_SRC current DAC passes from the TMP_SRC5 pin through the remote resistive temperature sensor and back through the resistor at TMP_REF5 to AGND
31	TMP_N5	Analog Input	Temp Sensor 5 Amplifier -ve Input	Inverting input for temperature sensor 5 differential amplifier. Connect to one end of the remote resistive temperature sensor and to TMP_REF5 either locally or at the temperature sensor for 2-wire or 4-wire measurement respectively
32	TMP_P5	Analog Input	Temp Sensor 5 Amplifier +ve Input	Non-inverting input for temperature sensor 5 differential amplifier Connect to one end of the remote resistive temperature sensor and to TMP_SRC5 either locally or at the temperature sensor for 2-wire or 4-wire measurement respectively
33	TMP_SRC5	Analog Output	Temperature Sensor 5 Current Source	Programmable current source for temperature sensor 5 set by the I_TEMP5_SRC current DAC
34	+1.5VA	Power	+1.5VA Analog Supply	+1.5V power rail for analog core. Connect this pin and pins 24, 52, 66, and 79 to the output of the internal +1.5V linear regulator at +1.5VA_LDO_OUT pin 133. Bypass close to the pin with a 100nF capacitor to AGND pin 35
35	AGND	Power	Analog GND	Analog Ground. All AGND and GND pins must be used and connected together
36	+5V	Power	+5V Signal Supply	Connect this pin, pin 68, and pin 131 to the output of the internal +5V linear regulator at +5V_LDO_OUT pin 142. Bypass close to the pin with a 100nF capacitor to AGND pin 67
37	LVDT_P1	Analog Input	LVDT 1 +ve Input	Non-inverting input for LVDT secondary 1 differential amplifier
38	LVDT_CM1	Analog Input	LVDT 1 CM input	Common mode input for LVDT secondary 1 differential amplifier
39	LVDT_N1	Analog Input	LVDT 1 -ve Input	Inverting input for LVDT secondary 1 differential amplifier
40	LVDT_P2	Analog Input	LVDT 2 +ve Input	Non-inverting input for LVDT secondary 2 differential amplifier
41	LVDT_CM2	Analog Input	LVDT 2 CM input	Common mode input for LVDT secondary 2 differential amplifier
42	LVDT_N2	Analog Input	LVDT 2 -ve Input	Inverting input for LVDT secondary 2 differential amplifier
43	LVDT_P3	Analog Input	LVDT 3 +ve Input	Non-inverting input for LVDT secondary 3 differential amplifier
44	LVDT_CM3	Analog Input	LVDT 3 CM input	Common mode input for LVDT secondary 3 differential amplifier
45	LVDT_N3	Analog Input	LVDT 3 -ve Input	Inverting input for LVDT secondary 3 differential amplifier
46	LVDT_P4	Analog Input	LVDT 4 +ve Input	Non-inverting input for LVDT secondary 4 differential amplifier
47	LVDT_CM4	Analog Input	LVDT 4 CM input	Common mode input for LVDT secondary 4 differential amplifier
48	LVDT_N4	Analog Input	LVDT 4 -ve Input	Inverting input for LVDT secondary 4 differential amplifier
49	AGND	Power	Analog GND	Analog Ground. All AGND and GND pins must be used and connected together
50	DRV_SNS_P2	Analog Input	LVDT 2 drive +ve Input	Non-inverting input for differential amplifier typically used for measuring the LC filtered LVDT 2's driver output
51	DRV_SNS_N2	Analog Input	LVDT 2 drive -ve Input	Inverting input for differential amplifier typically used for measuring the LC filtered LVDT 2's driver output
52	+1.5VA	Power	+1.5VA Analog Supply	+1.5V power rail for analog core. Connect this pin and pins 24, 34, 66, and 79 to the output of the internal +1.5V linear regulator at +1.5VA_LDO_OUT pin 133. Bypass close to the pin with a 100nF capacitor to AGND
53	DRV_SNS_P1	Analog Input	LVDT 1 drive +ve Input	Non-inverting input for differential amplifier typically used for measuring the LC filtered LVDT 1's driver output
54	DRV_SNS_N1	Analog Input	LVDT 1 drive -ve Input	Inverting input for differential amplifier typically used for measuring the LC filtered LVDT 1's driver output
55	AGND	Power	Analog GND	Analog Ground. All AGND and GND pins must be used and connected together
56	HV_P	Analog Input	High voltage +ve Input	Non-inverting input for differential amplifier typically used for measuring the motor driver supply voltage
57	HV_N	Analog Input	High voltage -ve Input	Inverting input for differential amplifier typically used for measuring the motor driver supply voltage
58	TEST1	Logic I/O	Test pin 1	Leave open
59	TEST2	Logic I/O	Test pin 2	Leave open
60	ISENSE1	Analog Input	Current Sense Input 1	Output of external isolated current sensor typically for motor phase current
61	ISENSE2	Analog Input	Current Sense Input 2	Output of external isolated current sensor typically for motor phase current
62	ISENSE3	Analog Input	Current Sense	Output of external isolated current sensor typically for motor phase current

Pin	Name	Pin Type	Pin Function	Description
			Input 3	
63	ISENSE4	Analog Input	Current Sense Input 4	Output of external isolated current sensor typically for motor phase current
64	ISENSE5	Analog Input	Current Sense Input 5	Output of external isolated current sensor typically for motor phase current
65	ISENSE_RTN	Analog Input	Current Sense GND Reference	GND reference for all current sense inputs
66	+1.5VA	Power	+1.5VA Analog Supply	+1.5V power rail for analog core. Connect this pin and pins 24, 34, 52, and 79 to the output of the internal +1.5V linear regulator at +1.5VA_LDO_OUT pin 133. Bypass close to the pin with a 100nF capacitor to AGND pin 67
67	AGND	Power	Analog GND	Analog Ground. All AGND and GND pins must be used and connected together
68	+5V	Power	+5V Signal Supply	Connect this pin, pin 36, and pin 131 to the output of the internal +5V linear regulator at +5V_LDO_OUT pin 142. Bypass close to the pin with a 100nF capacitor to AGND pin 67
69	DRV_GND1	Power	LVDT 1 GND	Connect to analog ground and use as star ground point for any LC filter used between the DRV_P1 and DRV_N1 LVDT drive outputs and LVDT 1's primary
70	DRV_P1	Analog Output	LVDT 1 Half bridge driver P	Output of one of the two complementary half bridge drivers working together to provide a full-bridge drive to LVDT 1's primary
71	DRV_N1	Analog Output	LVDT 1 Half bridge driver P	Output of one of the two complementary half bridge drivers working together to provide a full-bridge drive to LVDT 1's primary
72	DRV_+V	Power	LVDT Drivers Supply	Connect to the LVDT bridge drivers power supply (10V to 30V). Bypass close to the pin with a 2.2µF capacitor to AGND
73	NC	-		Pin not connected
74	DRV_P2	Analog Output	LVDT 2 Half bridge driver P	Output of one of the two complementary half bridge drivers working together to provide a full-bridge drive to LVDT 2's primary
75	DRV_N2	Analog Output	LVDT 2 Half bridge driver P	Output of one of the two complementary half bridge drivers working together to provide a full-bridge drive to LVDT 2's primary
76	DRV_GND2	Power	LVDT 2 GND	Connect to analog ground and use as star ground point for any LC filter used between the DRV_P2 and DRV_N2 LVDT drive outputs and LVDT 2's primary
77	OSC2	Analog Input	Crystal Oscillator	Connect to a crystal/capacitor network to set the system clock frequency in the range 20MHz to 30MHz, or drive OSC1 with an external clock and leave OSC2 open
78	OSC1	Analog Input	Crystal Oscillator	
79	+1.5VOSC	Power	+1.5VA Analog Supply	+1.5V power rail for the crystal oscillator. Connect this pin and pins 24, 34, 52, and 66 to the output of the internal +1.5V linear regulator at +1.5VA_LDO_OUT pin 133. Bypass close to the pin with a 100nF capacitor to AGND
80	+1.5VD	Power	+1.5VD Digital Supply	+1.5V power rail for digital core. Connect this pin to the output of the internal +1.5V linear regulator at +1.5VD_LDO_OUT pin 131. Bypass close to the pin with a 100nF capacitor to DGND pin 81
81	DGND	Power	Digital GND	Digital ground. All AGND and GND pins must be used and connected together
82	VDD	Power	I/O Supply	Connect this pin and pin 110 to the external controller's I/O power supply (2.25V to 5.5V) to set the I/O logic level for all logic I/Os. Bypass close to the pin with a 1µF capacitor to GND
83	RESET	Logic Input (tbdΩ to VDD)	Reset Input	Active high input resets the internal settings to a known state
84	CLKOUT	Logic Output	Clock Output	Buffered clock output of frequency defined at teh OSC1 and OSC2 pins
85	PWM1	Logic Output	PWM Output 1	Pulse width modulated output 1 intended for a motor phase or solenoid driver
86	PWM2	Logic Output	PWM Output 2	Pulse width modulated output 2 intended for a motor phase or solenoid driver
87	PWM3	Logic Output	PWM Output 3	Pulse width modulated output 3 intended for a motor phase or solenoid driver
88	PWM4	Logic Output	PWM Output 4	Pulse width modulated output 4 intended for a motor phase or solenoid driver
89	PWM5	Logic Output	PWM Output 5	Pulse width modulated output 5 intended for a motor phase or solenoid driver
90	PWM6	Logic Output	PWM Output 6	Pulse width modulated output 6 intended for a motor phase or solenoid driver
91	PWM7	Logic Output	PWM Output 7	Pulse width modulated output 7 intended for a motor phase or solenoid driver
92	PWM8	Logic Output	PWM Output 8	Pulse width modulated output 8 intended for a motor phase or solenoid driver
93	GPIO1	Logic I/O	GPIO 1	General purpose logic I/O port 1
94	GPIO2	Logic I/O	GPIO 2	General purpose logic I/O port 2
95	GPIO3	Logic I/O	GPIO 3	General purpose logic I/O port 3
96	GPIO4	Logic I/O	GPIO 4	General purpose logic I/O port 4
97	GPIO5	Logic I/O	GPIO 5	General purpose logic I/O port 5
98	GPIO6	Logic I/O	GPIO 6	General purpose logic I/O port 6
99	GPIO7	Logic I/O	GPIO 7	General purpose logic I/O port 7
100	GPIO8	Logic I/O	GPIO 8	General purpose logic I/O port 8
101	GPIO9	Logic I/O	GPIO 9	General purpose logic I/O port 9
102	$\overline{\text{FAULT}}$	Logic Output	$\overline{\text{Fault}}$ Alert	Active low fault alert
103	FAULT	Logic Output	Fault Alert	Active high fault alert
104	JTAG_TCK	Logic Input	JTAG Clock	JTAG Clock
105	JTAG_TMSC	Logic Input	JTAG Mode Select	JTAG Mode Select

Pin	Name	Pin Type	Pin Function	Description
106	JTAG_TDO	Logic Output	JTAG Data Output	JTAG Data Output
107	JTAG_TDI	Logic Input	JTAG Data Input	JTAG Data Input
108	SCLK1	Logic Input	SPI Clock 1	Clock input for SPI channel 1 interface
109	DGND	Power	Digital GND	Digital ground. All AGND and GND pins must be used and connected together
110	VDD	Power	I/O Supply	Connect this pin and pin 82 to the external controller's I/O power supply (2.25V to 5.5V) to set the I/O logic level for all logic I/Os. Bypass close to the pin with a 1µF capacitor to GND
111	MOSI1/RXD1	Logic Input	SPI MOSI 1, or UART RXD 1	Data input for SPI channel 1 or UART channel 1 interface
112	MISO1/TXD1	Logic Output	SPI MISO 1, or UART TXD 2	Data output for SPI channel 1 or UART channel 1 interface
113	SS1	Logic Input	SPI Select 1	Active low SPI select for SPI channel 1 interface
114	SCKL2	Logic Input	SPI Clock 2	Clock input for SPI channel 2 interface
115	MOSI2/RXD2	Logic Input	SPI MOSI 2, or UART RXD 2	Data input for SPI channel 2 or UART channel 2 interface
116	MISO2/TXD2	Logic Output	SPI MISO 2, or UART TXD 2	Data output for SPI channel 2 or UART channel 2 interface
117	SS2	Logic Input	SPI Select 2	Active low SPI select for SPI channel 2 interface
118	DGND	Power	Digital GND	Digital ground. All AGND and GND pins must be used and connected together
119	UNLOCK	Logic Input (tbdΩ to GND)	OTP Programming Enable	Connect to logic high to enable enable OTP programming
120	UART_EN	Logic Input	UART/SPI Mode	Connect to VDD or logic high to enable dual UART serial interfaces. Connect to DGND to enable dual SPI serial interfaces
121	+1.5VD_LDO_OUT	Power	+1.5VD Regulator Output	+1.5V linear regulator output. Connect this pin to pin 80. Bypass close to the pin with a 1µF capacitor to DGND pin 123
122	+1.5VD_LDO_IN	Power	+1.5VD Regulator Input	+1.5V linear regulator input. Connect this pin a 1.85V to 5.5V supply. Bypass close to the pin with a 2.2µF capacitor to DGND pin 123
123	DGND	Power	Digital GND	Connect to digital ground and use as star ground point for the +1.5VD regulator bypass capacitors. All AGND and GND pins must be used and connected together
124	HEP3	Logic Input	Hall Effect Input 3	Hall Effect or other sensor comparator input. 5V logic input with 2V hysteresis
125	HEP2	Logic Input	Hall Effect Input 2	Hall Effect or other sensor comparator input. 5V logic input with 2V hysteresis
126	HEP1	Logic Input	Hall Effect Input 1	Hall Effect or other sensor comparator input. 5V logic input with 2V hysteresis
127	AGND	Power	VREF GND	Connect to analog ground and use as star ground point for the VREF pin bypass capacitor(s). All AGND and GND pins must be used and connected together
128	VREF_IN	Analog Input	External VREF Input	To use the internal +1.235V reference ±2mV reference voltage, connect VREF_IN to VREF_OUT pin 129. To use an external reference voltage up to tbdV, connect the external reference to VREF_IN and bypass with a 100nF capacitor from VREF_IN to AGND pin 127
129	VREF_OUT	Analog Output	Internal VREF Output	+1.235V internal reference voltage. Bypass with a 100nF capacitor from VREF_OUT to AGND pin 127, even if an external reference voltage is used at VREF_IN
130	POR	Logic Input	POR Delay	Fit a 10nF capacitor from POR to AGND to set the power on reset delay
131	+5V	Power	+5V Signal Supply	Connect this pin, pin 36, and pin 68 to the output of the internal +5V linear regulator at +5V_LDO_OUT pin 142. Bypass close to the pin with a 100nF capacitor to AGND pin 67
132	+1.5VA_LDO_IN	Power	+1.5VA Regulator Input	+1.5V linear regulator input. Connect this pin a 1.85V to 5.5V supply. Bypass close to the pin with a 2.2µF capacitor to AGND pin 134
133	+1.5VA_LDO_OUT	Power	+1.5VA Regulator Output	+1.5V linear regulator output. Connect this pin to pins 24, 34, 52, 66, and 79. Bypass close to the pin with a 1µF capacitor to AGND pin 134
134	AGND	Power	+1.5VA GND	Connect to analog ground and use as star ground point for the +1.5VA regulator bypass capacitors. All AGND and GND pins must be used and connected together
135	BUCK_VFB	Analog Input	Buck voltage sense	The buck converter regulates its output to maintain the voltage at this pin to the voltage at VREF_IN pin 128 (typically 1.235V)
136	BUCK_VIN	Power	Buck supply	Buck converter, normally connected to +15V.
137	BUCK_SW	Analog Output	Buck SW output	Buck converter switching node. Connect to external inductor and Schottky diode
138	BUCK_GND	Power	Buck GND	Buck converter GND pin. Connect to AGND pin 139
139	AGND	Power	Analog GND	Analog Ground. All AGND and GND pins must be used and connected together
140	+5.25V_LDO_OUT	Power	+5.25V Regulator Output	+5.25V linear regulator output. This supply is available for external system loads up to 25mA. Bypass close to the pin with a 1µF capacitor to AGND
141	+5V_LDOs_IN	Power	+5.25 and +5V Regulators Input	+5.25 and +5V linear regulators input. Connect this pin a 6.2V to 16V supply. Bypass close to the pin with a 1µF capacitor to AGND
142	+5V_LDO_OUT	Power	+5V Regulator Output	+5V linear regulator output. Connect this pin to pins 36, 68, and 131. Bypass close to the pin with a 1µF capacitor to AGND
143	AGND	Power	Analog GND	Analog Ground. All AGND and GND pins must be used and connected together
144	VCC	Power	Input Supply	Connect to the main power supply (10V to 30V). Bypass close to the pin with a 2.2µF capacitor to AGND pin 143

4 Absolute Maximum Ratings

Stresses above those listed in ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Parameter	Min	Max	Units
Main Power (VCC) and VFB to GND	-0.5	40	V
Logic IO Supply Voltage (VDD pins to GND)	-0.5	5.5	V
PS_SRC# voltage	-0.5	40	V
1.5V domains (analog and digital core) IO	-0.5	1.7	V
All other 5V domain pins to GND	-0.5	5.75	V
Operating junction temperature	-55	155	ºC
Storage junction temperature	-65	165	ºC
Peak lead solder temperature (10 seconds)		260	ºC

5 Electrostatic Discharge Ratings

JEDEC JEP155 states that 500V HBM allows safe manufacturing with a standard ESD controlled process.
JEDEC JEP157 states that 250V CDM allows safe manufacturing with a standard ESD controlled process.
ESD ratings apply to all pins.

ESD Test	Minimum Capability
HBM: Human Body Model, per MIL-STD-883 TM3015	±2kV
CDM: Charged Device Model, per ANSI/ESDA/JEDEC JS-002	±TBDV

6 Operating Ratings

Performance is generally guaranteed over this range as further detailed below under Electrical Characteristics.

Parameter	Min	Max	Units
Main Power (VCC and VFB to GND)	10	30	V
Digital IO supply (VDD to DGND)	2.25	5.5	V
PS_SRC# voltage		VCC	V
DRV_P, DRV_M voltage	0	VFB	V
DRV_P, DRV_M current	-25	25	mA
5V linear regulators input (V5VIN)	6.2	16	V
1.5V linear regulators inputs (V1V5INA and V1V5IND)	1.85	5.5	V
1.5V analog core supply	1.49	1.56	V
1.5V digital core supply	1.425	1.575	V
5V domains (analog core)	4.5	5.5	V
All other pins to GND	0	5.5	V
Operating Junction Temperature	-55	120	°C

7 Electrical Characteristics

The following specifications apply over the operating ambient temperature of -55°C ≤ T_A ≤ 110°C except where otherwise noted with the following test conditions: VCC = VFB = 15V, VDD = 3.3V; VREF_IN = 1.235V; Crystal frequency = 22.5MHz. Typical parameters refer to T_J = 25°C. Positive currents flow into pins.

Symbol	Parameter	Test Conditions/Comments	Min	Typ	Max	Units
Operating Current						
IVCC	VCC Current	Maximum loading on pressure sensor supplies before current limit			100	mA
IVDD	VDD Current	Depending on the digital IO load			20	mA
IVFB	VFB Current	With 10kΩ between DRV_P and DRV_M			10	mA
IREF_IN	REF_IN Current				0.1	mA
IVCCR	VCC ready current	After reset done and faultb=1			TBD	mA
IVCCO	VCC operating current	Using “use case 1” activity pattern			TBD	mA
IVFBINR	VFB ready current	After reset done and faultb=1			TBD	mA
IVFBINO	VFB operating current	Using “use case 1” activity pattern			TBD	mA
IV5VINR	V5VIN ready current	After reset done and faultb=1			TBD	mA
IV5VINO	V5VIN operating current	Using “use case 1” activity pattern			TBD	mA
IV1V5VINDR	V1V5VIND ready current	After reset done and faultb=1			TBD	mA
IV1V5VINDO	V1V5VIND operating current	Using “use case 1” activity pattern			TBD	mA
IV1V5VINAR	V1V5VINA ready current	After reset done and faultb=1			TBD	mA
IV1V5VINAO	V1V5VINA operating current	Using “use case 1” activity pattern			TBD	mA
Input supplies UV/OV						
OV_VCC/FB	VCC & VFB over-voltage	Applies to both VCC and VFB supplies inputs - VREF = 1.235V	36.75		37.75	V
OV_VCC/FB_hyst	VCC & VFB over-voltage hysteresis	Applies to both VCC and VFB supplies inputs - VREF = 1.235V	0.8		1.8	V
UV_VCC/FB	VCC &VFB under-voltage	Applies to both VCC and VFB supplies inputs - VREF = 1.235V	9.5		10.3	V
UV_VCC/FB_hyst	VCC & VFB under-voltage hysteresis	Applies to both VCC and VFB supplies inputs - VREF = 1.235V		0.30		V
OV_VDD	VDD over-voltage	VREF = 1.235V	5.75		5.95	V
OV_VDD_hyst	VDD over-voltage hysteresis	VREF = 1.235V		0.20		V
UV_VDD	VDD under-voltage	VREF = 1.235V	1.85		2.05	V
UV_VDD_hyst	VDD under-voltage hysteresis	VREF = 1.235V		0.08		V
OV_V5VIN	V5VIN over-voltage	VREF = 1.235V	17.65		18.25	V
OV_V5VIN_hyst	V5VIN over-voltage hysteresis	VREF = 1.235V		0.22		V
UV_V5VIN	V5VIN under-voltage	VREF = 1.235V	5.9		6.05	V
UV_V5VIN_hyst	V5VIN under-voltage hysteresis	VREF = 1.235V		0.09		V
OV_V1V5IN	V1V5IN over-voltage	Applies to both V1V5INA and V1V5IND - VREF = 1.235V	5.75		5.95	V
OV_V1V5IN_hyst	V1V5IN over-voltage hysteresis	Applies to both V1V5INA and V1V5IND - VREF = 1.235V		0.22		V
UV_V1V5IN	V1V5IN under-voltage	Applies to both V1V5INA and V1V5IND - VREF = 1.235V	1.7		1.8	V
UV_V1V5IN_hyst	V1V5IN under-voltage hysteresis	Applies to both V1V5INA and V1V5IND - VREF = 1.235V		0.09		V
Internally Regulated Voltages and Currents						
V5VE	5.25V regulator	(external load of 25mA)	5.15	5.25	5.35	V
V5V	5V regulator	For internal circuits		5.0		V
V1.5VA	1.5V regulator for analog	For internal circuits	1.49	1.525	1.56	V

Symbol	Parameter	Test Conditions/Comments	Min	Typ	Max	Units
V1.5VD	1.5V regulator for digital	For internal circuits	1.425	1.5	1.575	V
VVREF	VREF regulator	Connected to REF_IN	1.233	1.235	1.237	V
I5VE	5.25V regulator	Short Circuit Current			170	mA
I5VE_Reg	5.25V regulator	Maximum current for linear region operation - V5VIN = 6V			100	mA
I5V	5V regulator	Short Circuit Current			170	mA
I5V_Reg	5V regulator	Maximum current for linear region operation - V5VIN = 5.8V			100	mA
I1.5V	1.5V regulator	Short Circuit Current			120	mA
I1.5V_reg	1.5V regulator	Maximum current for linear region operation - V1V5IN = 1.8V			50	mA
IVREF	VREF regulator	Short Circuit Current		2		mA
IV5VE_open	5.25V reg open current detect	Light load	1		8	mA
Regulated outputs UV/OV						
V5VE_ov		VREF = 1.235V	5.60		5.85	V
V5VE_ov_Hyst		VREF = 1.235V		-0.175		V
V5VE_uv		VREF = 1.235V	4.50		4.75	V
V5VE_uv_Hyst		VREF = 1.235V		0.140		V
V5V_ov		VREF = 1.235V	5.40		5.65	V
V5V_ov_Hyst		VREF = 1.235V		-0.17		V
V5V_uv		VREF = 1.235V	4.40		4.60	V
V5V_uv_Hyst		VREF = 1.235V		0.140		V
V1V5VA_ov		VREF = 1.235V	1.575		1.625	V
V1V5VA_ov_Hyst		VREF = 1.235V		-0.06		V
V1V5VA_uv		VREF = 1.235V	1.40		1.49	V
V1V5VA_uv_Hyst		VREF = 1.235V		0.02		V
V1V5VD_ov		VREF = 1.235V	1.575		1.625	V
V1V5VD_ov_Hyst		VREF = 1.235V		-0.06		V
V1V5VD_uv		VREF = 1.235V	1.350		1.425	V
V1V5VD_uv_Hyst		VREF = 1.235V		0.02		V
V1V5VD_Crit_ov		VREF = 1.235V		2.47		V
T LDOS_OT		LDOs V1V5VA, V1V5VD, V5V and V5VE over-temperature shutdown threshold	165		195	°C
T LDOS_OT_hyst		Applies to V1V5VA, V1V5VD, V5V and V5VE over-temperature shutdown hysteresis		20		°C
Clocks						
FOSC	Oscillator frequency	System clock at OSC1 and OSC2 pins	20	22.5	30	MHz
VFosc_ov	Xtal supply V1V5VOSC		1.615		1.665	V
VFosc_ov_Hyst	Xtal supply V1V5VOSC			-0.015		V
VFosc_uv	Xtal supply V1V5VOSC	Disables XTAL	1.345		1.385	V
VFosc_uv_Hyst	Xtal supply V1V5VOSC			0.015		V
FPWM	PWM frequency		5	10	20	kHz
FLVDT_PWM	PWM for LVDT sinewave driver		100	200	300	kHz
FSAMPLE	SD modulator sample clock	As a multiple of crystal frequency		1/12		-
FPLL	Internal PLL	Equals FOSC frequency x4	80	90	120	MHz
FWD	Internal watchdog frequency	After calibration	410		470	kHz
Power on reset						
TPOR	Power on reset delay	With CPOR = 1nF		1.3ms		ms
LVDT Inputs (with sinc3 filter set for OSR = 256)						

Symbol	Parameter	Test Conditions/Comments	Min	Typ	Max	Units
VLVDTx_cm	Regulated VCM for secondary coils	VREFH = 1.3V and VREFL = 0.2V		0.75		V
ILVDTx_cm	Load current range	For a common mode error of 50mV	-1		1	mA
VLVDT#	Diff Input voltage	extrapolated positive full scale	TBD	1.1	TBD	V
V LVDT#	Diff Input voltage	Offset	TBD		TBD	V
V LVDT#	Diff Input voltage	extrapolated negative full scale	TBD	-1.1	TBD	V
V LVDT#	Common mode rejection	DC	TBD			dB
I LVDT#	Pin Leakage Current	Power on and 0.1V< V LVDT# <1.4V	TBD		TBD	nA
I LVDT#	Pin Leakage Current	Power off and 0V< V LVDT# <1.5V	TBD		TBD	nA
AV LVDT#	Linearity rel. to full scale	Gain error from straight line	-100		100	PPM
AV LVDT#	Matching CH to CH	CH1 to CH2 and CH3 to CH4	TBD		TBD	%
RES LVDT#	Resolution	As ratio of digital full scale (OSR=256)			1/214	FS
SNR LVDT#	Signal to Noise Ratio	At TBD ksps output rate (OSR=256) in 1 kHz bandwidth	TBD			dB FS
		At TBD ksps output rate (OSR=32) in 8 kHz bandwidth	50			
C LVDT#	Diff input capacitance				5	pF
R LVDT#	Diff input resistance		1000			kΩ
I_SNS inputs (with sinc3 filter set for OSR = 512)						
VI_SNS#	Diff Input voltage	Extrapolated positive full scale	TBD	1.1	TBD	V
V I_SNS#	Diff Input voltage	Offset	TBD		TBD	V
V I_SNS#	Diff Input voltage	Extrapolated negative full scale	TBD	-1.1	TBD	V
V I_SNS#_RTN	I_SNS_RTN allowed		1.2		3.8	V
V I_SNS#_RTN	Common mode rejection	DC	55			dB
I I_SNS#	Pin Leakage Current	Power on and 0.1V< V I_SNS# <1.4V	TBD		TBD	nA
I I_SNS#	Pin Leakage Current	Power off and 0V< V I_SNS# <1.5V	TBD		TBD	nA
AV I_SNS		Gain of Isense AFE		1		V/V
AV I_SNS	Linearity rel. to full scale	Gain error from straight line	-100		100	PPM
AV I_SNS	Matching CH to CH	CH1 to CH2 and CH3 to CH4	TBD		TBD	%
RES #	Resolution	As ratio of digital full scale (OSR=256)			1/214	FS
SNR I_SNS#	Signal to Noise Ratio	At TBD ksps output rate (OSR=512) in 1 kHz bandwidth	TBD			dB FS
		At TBD ksps output rate (OSR=32) in 8 kHz bandwidth	50			
C I_SNS#	Diff input capacitance			10		pF
R I_SNS#	Diff input resistance			200		kΩ
Internal SARs References						
VREFH	SARs upper reference	REF_IN = 1.235V, after calibration		1.3		V
VREFL	SARs lower reference #1	REF_IN = 1.235V - Used for monitoring PRESSx, PTxxxx, DRVSNSx, VCC, internal average temperature, LVDTx_CM and redundant bandgap		0.2		V
VREFL_GND	SARs lower reference #2	REF_IN = 1.235V - Monitoring HV_P/N, PSx_SRC VDS		0		V
RES SAR#	Resolution	As ratio of digital full scale			1/210	FS
Redundant bandgap						
VBG_red			1.18	1.2	1.22	V
VCC SAR monitoring AFE						
AV	Divider value			1/25		V/V
AV_acc	accuracy		TBD		TBD	%
PSx_SRC switches						
VPSx_SRC	Voltage drop between VCC pin and PSx_SRC pins	20mA load			0.5	V

Symbol	Parameter	Test Conditions/Comments	Min	Typ	Max	Units
AVPSx_SRC	Gain of voltage drop monitoring AFE			2		V/V
	Accuracy	At Vdrop = 0.45V	-2.5		2.5	% FS
PRESS (Pressure Sensor) Inputs						
VPRESS#	Diff Input voltage	full scale output	1.08	1.10	1.12	V
V PRESS#	Diff Input voltage	zero output	-0.02	0	0.02	V
V PRESS#	Input Voltage range	Relative to GND	0.2		1	V
V PRESS#	Common mode rejection		60			dB
I PRESS#	Pin Leakage Current	Power on and 0.1V < V PRESS#< 1.4V	TBD		TBD	nA
I PRESS#	Pin Leakage Current	Power off and 0V < V PRESS#< 1.5V	TBD		TBD	nA
AVPRESS	Gain of PRESS AFE			1		V/V
AVPRESS	Linearity rel. to full scale	Gain error from straight line	-1		1	LSB
SNR AVPRESS	Signal to Noise Ratio	Condition TBD, BW=200Hz	60			dB
C PRESS#	Diff input capacitance			10		pF
R PRESS#	Diff input resistance			870		kΩ
HV inputs						
VHV	Input voltage	full scale output	1.28	1.3	1.32	V
VHV	Input voltage	zero output	-0.02	0	+0.02	V
VHV	Input Voltage range	Relative to GND	0		1.3	V
I VHV	Pin Leakage Current	Power on and 0.1V < VHV < 1.4V	TBD		TBD	nA
I VHV	Pin Leakage Current	Power off and 0V < V HV < 1.5V	TBD		TBD	nA
AVHV	Linearity rel. to full scale	Gain error from straight line	-1		1	LSB
SNR AVHV	Signal to Noise Ratio	Condition TBD BW=1kHz	60			dB FS
I WPU_HV	Weak pull-up current	For floating input detection		5		µA
I SPU_HV	Strong pull-up current	For short detection		400		µA
TEMP (Temperature Sensor) Inputs						
ISRC_PT100	Output current source for PT100 interface	After calibration Selected PT100 mode	0.97	1	1.03	mA
ISRC_PT1000	Output current source for PT1000 interface	After calibration Selected PT1000 mode	0.485	0.5	0.515	mA
ISRC_ACC	Current source accuracy	Over the full temperature range PT100 or PT1000 mode	-3		3	%
AV_PT100	AFE gain for PT100 interface	Selected PT100 mode		18/3.5		V/V
AV_PT1000	AFE gain for PT1000 interface	Selected PT1000 mode		18/17		V/V
VTEMP#_100	Diff Input voltage	full scale output PT100		213.9		mV
V TEMP#_100	Diff Input voltage	zero output		0		mV
VTEMP#_1000	Diff Input voltage	full scale output PT1000		1.039		mV
V TEMP#_1000	Diff Input voltage	zero output		0		mV
V TEMP#	Input Voltage range	Relative to GND	0		1.5	V
V TEMP#	Common mode rejection	CM=0.675V-1.075V for PT1000	57			dB
I TEMP#	Pin Leakage Current	Power on and 0V < V TEMP#< 1.2V	TBD		TBD	nA
I TEMP#	Pin Leakage Current	Power off and 0V < V TEMP#< 1.5V	TBD		TBD	nA
AV TEMP	Linearity	Gain error from straight line	-1		1	LSB
SNR TEMP#	Signal to Noise Ratio	Condition TBD BW=200Hz	60			dB FS
C TEMP#	Diff input capacitance			10		pF
R TEMP#_PT100	Diff input resistance	Selected PT100 mode		100		kΩ
R TEMP#_PT1000	Diff input resistance	Selected PT1000 mode		1000		kΩ
I WPU_TEMP	Weak pull up current	For floating input detection on the four TEMP pins on all temperature channels		14		µA
DRVSNS interface						
AV_drvsns	AFE gain			0.5		V/V
AV_drvsns_acc	AFE gain accuracy		-0.15		0.15	%

Symbol	Parameter	Test Conditions/Comments	Min	Typ	Max	Units
Vos_drvsns	AFE offset		-3		3	mV
Vcm_o_drvsns	AFE output common mode	Output VCM		0.75		V
V drvsns#_p/n	Input Voltage range	Relative to GND	0		1.5	V
V drvsns#_p/n_diff	Diff Input voltage	full scale output		1.1		V
V drvsns#_p/n_diff	Diff Input voltage	half scale output		0		V
V drvsns#_p/n_diff	Diff Input voltage	zero output		-1.1		V
SNR	Signal to Noise Ratio	Condition TBD	TBD			dB FS
C drvsns	Diff input capacitance			10		pF
R drvsns	Diff input resistance		2000			kΩ
IWPU_DRVSNS	Weak pull-up current	For float detection (on DRVSNSx_P/N)		5		uA
ISPU_DRVSNS	Strong pull-up current	For short detection (on DRVSNSx_P/N)		400		uA
Internal junction temperature sensing AFE						
VTJ-60C	SAR output code at cold	-60°C, external reference	TBD	603	TBD	-
VTJ+25C	SAR output code at room	25°C, external reference		470		-
VTJ+115C	SAR output code at hot	115°C	TBD	330	TBD	-
Half Bridge driver						
VDRV	High Level Voltage	Relative to VFB; sourcing 160mA	-650		0	mV
VDRV	Low Level Voltage	Sinking 160mA in the inductive load.	0		650	mV
RDRV	High-Z state Impedance	Output disabled or powered off	42			kΩ
tPHL	Propagation Delay H to L	PWM to DRV		100		ns
tPLH	Propagation Delay L to H	PWM to DRV		100		ns
tPHL,PLH	Propagation Delay	Matching between P and N		5		ns
tR,F	Rise time	10% to 90%		20		ns
tR,F	Fall time	10% to 90%		20		ns
BUCK regulator						
VIN_BUCK	Input voltage range	Depending on application	4		VCC	V
VFB_REG_L	Feedback target	VBG_red = 1.2V	1.130	1.135	1.150	V
VFB_REG_H	Feedback target threshold voltage high	VBG_red = 1.2V	1.150	1.155	1.170	V
Vbk_ov	VSNS_bk over-voltage	VBG_red = 1.2V		1.435		V
Vbk_uv	VSNS_bk under-voltage	VBG_red = 1.2V		1.04		V
LDreg	Load regulation tolerance	L=100uH, C=10uF, Load step = 30mA		10		%
LNreg	Line regulation tolerance	L=100uH, C=10uF, Line step = 1V		10		%
Ilim	Output current limit			500		mA
Tstart	Output ramp-up time			1		ms
GPIO, SPI, PWM, other digital interface pins (VDD domain)						
VLOGIC	Input Logic Threshold	VIH			66	%VDD
		VIL	30			%VDD
		Hysteresis		20		%VDD
VLOGIC	Logic Output Levels	High Logic Level (1mA source)	VDD-0.3		VDD	V
		Low Logic Level (1mA sink)	0		0.3	
ILOGIC	Input currents	0 < VLOGIC< VDD	-1	0	1	µA
UARTBAUD	UART baud rate				1	Mbps
FCLK_SPI	SPI clock frequency	Maximum operating circuit with 10pF maximum on MISO			30	MHz
DSEL_CLK	SSN / to SCLK / minimum delay	FOSC=25MHz, PLL mode			TBD	ns
		FOSC=25MHz, PLL bypass mode			TBD	ns
Hall effect digital interface pins (5V domain)						
VLOGIC	Input Logic Threshold	VIH			4	V
		VIL	1			V

Symbol	Parameter	Test Conditions/Comments	Min	Typ	Max	Units
		Hysteresis	2			V
ILOGIC	Input currents	0V	-1	0	1	µA
ILOGIC	Input currents	5V	5	0	30	µA
Td	Input to output delay	Output GPIO loaded with < 100pF			0.2	µs

8 Thermal Properties

Thermal resistance, θ_{JB}, is provided from die to the back surface of the package. Junction temperature T_J is calculated using $T_J = T_B + (PD \times \theta_{JB})$, where T_B is the temperature maintained on the back surface of the package.

Package	Thermal Resistance	Typ	Units
CFP-28	θ_{JB}	5	°C/W

9 Functional Block Diagram

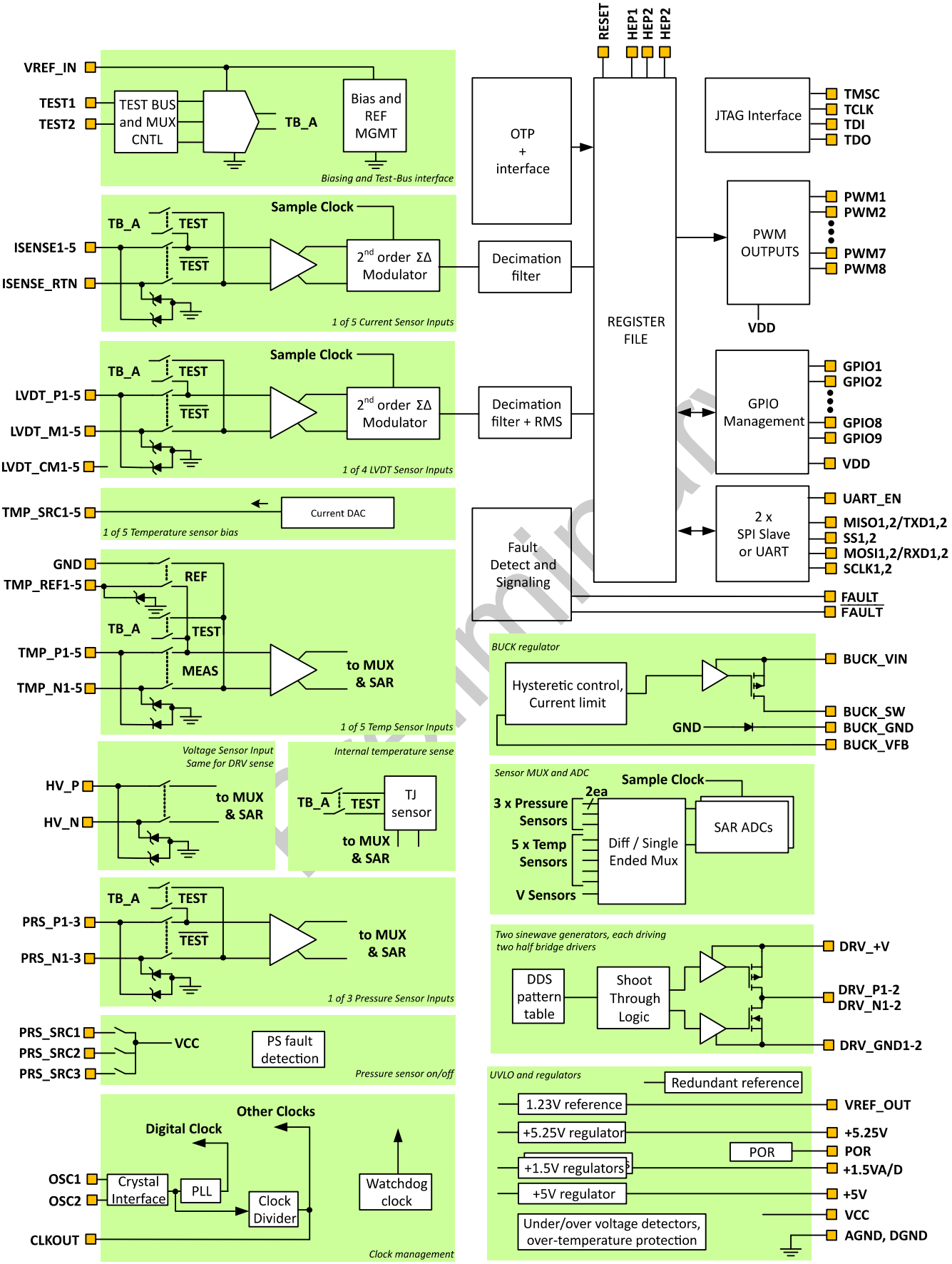


Figure 1. Functional Block Diagram

10 Typical Application

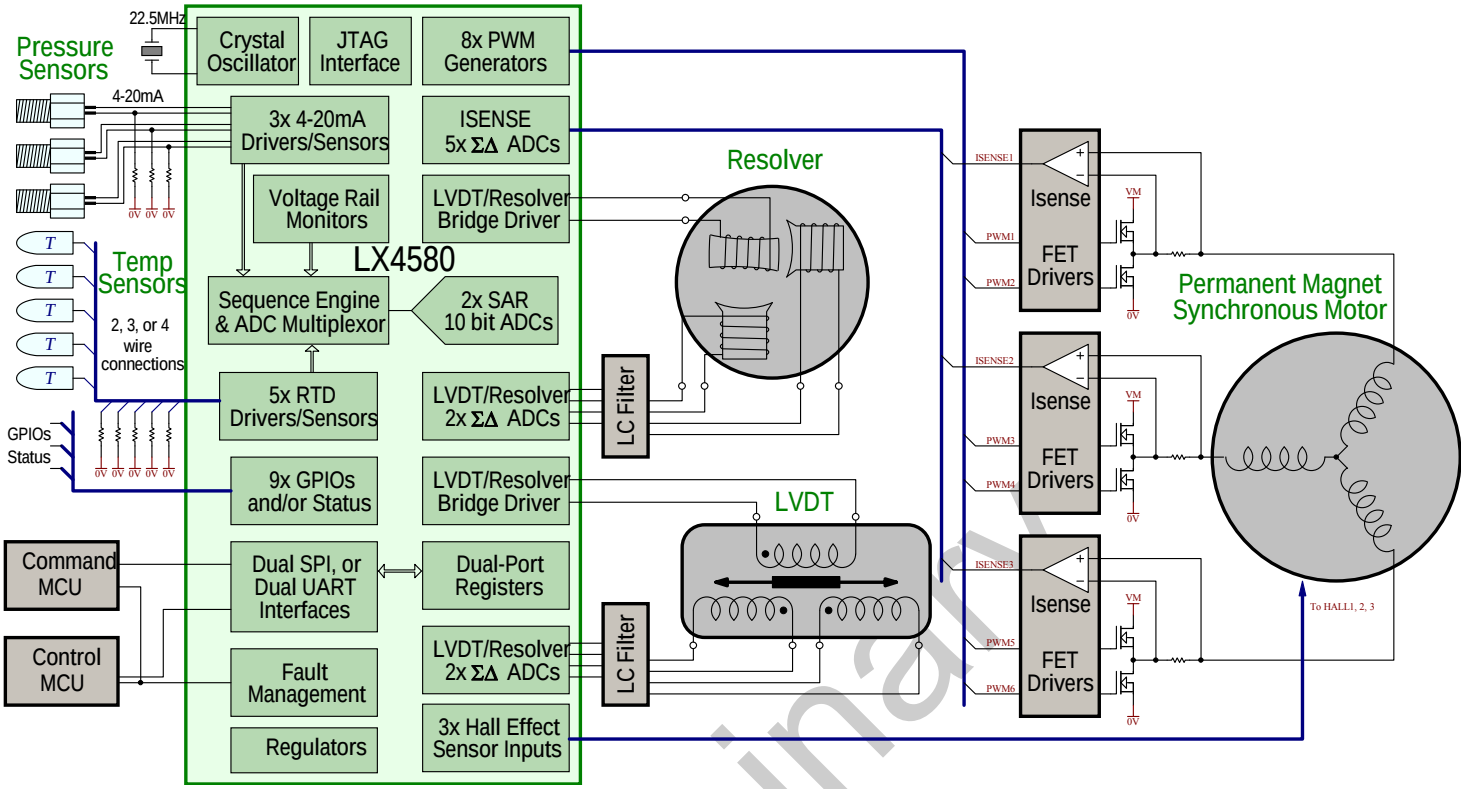


Figure 2. 11 Typical Application

11 LX4580 Operation

11.1 Clock Generator

The LX4580 AFE contains a crystal oscillator interface that is used to generate the necessary clocks for communications, PWM and the sample frequency for the ADCs. The crystal frequency is typically 22.5MHz. The logic is clocked at a rate of 4x the crystal frequency using a PLL. Alternatively, the crystal input OSC1 can be driven by an external clock signal with a 0-1.5V logic levels.

11.2 Analog-to-Digital Converter

The LX4580 contains 9 sigma delta ADCs, 4 for the LVDT sense interfaces, 5 for the current sense channels. Each second order sigma delta modulator can be clocked at or below 2MHz. The ADCs are referenced to the REF_IN input. The resolution of the ADC is a function of the oversampling ratio and can vary from 8 bits to 16bits. Each channel contains pipelined logic that performs the sinc3 filtering. Register values are used to set the oversample rate. The output is stored in a 16 bit register and updated at the decimation rate.

11.3 LVDT interface

There are four LVDT differential inputs which have dedicated sigma delta ADCs. These differential input pairs are designed to interface to an otherwise floating transformer secondary that is referenced to VREF. The LVDT speed and angle algorithm is executed by the user application. Alternatively, the user can read the on-chip logic that calculates the RMS value per channel over one period useful for position calculation at the external application level. This is provided at a rate of one or two samples per exciter input period.

11.4 Current sensing interface

There are five current sensing differential inputs which have dedicated signal delta ADCs. These differential input pairs are designed to interface to a current transformer or isolated current sense amplifier that has a common reference voltage.

11.5 Auxiliary Sensors interface

There are five temperature sensors, three current loop pressure sensors and four voltage sensors (two of which are to be used to sense LVDT exciter outputs). The temperature sensors can be biased with five DAC-programmable current sources. There is a dedicated instrumentation amplifier (IA) for each of the five temperature sensor inputs that can read the temperature sensor voltage and the voltage across the associated reference resistor. This way, the user can implement a ratio-metric measurement. The IA outputs feed into two 16-channel multiplexers along with the three pressure sensor inputs and internal auxiliary inputs used for self-tests. The multiplexers outputs feeds into two 10-bit SAR ADCs. There are three 2-wire 4-20mA current loop pressure sensor inputs designed to measure the output current of the sensor. Each pressure sensor has a dedicated IA as do the three voltage sensors. There is a dedicated 15V power output for each pressure sensor that has a current limit, an over-temperature flag register bit and a register controlled shut off switch.

11.6 Full bridge drivers

Two full bridge circuits are provided to be used to generate a synthesized periodic (sinewave) wave from pulse width modulated output. An internal state machine can be activated via a SPI command for this purpose; the sinewave frequencies and individual waveform pattern are register programmable. An external LC filter can be used to remove the switching ripple. Each half bridge driver is designed to drive 0.5k? impedance in a full bridge configuration with a minimum 10V peak voltage. Separate power supply input, and ground, are designated for providing power to the bridge drivers.

11.7 Pulse width modulated outputs

The LX4580 provides 8 PWM outputs that are register programmable for frequency and duty cycle and initial phase. These PWM outputs control the 4 half bridge circuits for driving a three-phase motor and controlling a park, anti-extension solenoid. The PWM outputs are register controlled. The ADC sampling, PWMs of the periodic LVDT sinewave and the control PWMs are programmable in a harmonic ratio such that an integer number of motor control switching cycles corresponds to any of the other timings and an integer number of ADC samples are taken during any of the two LVDT driver independent sinewaves. In a typical application, the master clock is 22.5MHz, the two LVDT sinewave frequencies are 1.4kHz and 2.0kHz, control PWM frequency is 11kHz, and LVDT sense sigma delta modulator clocks are 1.4MHz and 1.9MHz

11.8 RESET input

The LX4580 provides a RESET input that results in system reset.

11.9 GPIO pins

The LX4580 provides 9 GPIO pins that can be programmed by the application to be either inputs or outputs. (The default setting, if not specified otherwise, is input.) This GPIO pins respond to CMOS logic that is referenced to the VDD pin. Some GPIO pins have pre-defined functions that can be programmed (see Figure 1 for host processor synchronization example). Additionally, there are three dedicated 5V input pins with larger hysteresis that can be used as inputs for Hall effect proximity sensors.

11.10 SPI / UART interfaces

Two slave SPI/UART interfaces are provided to allow the application to read from and write to the register file of LX4580. The two slave SPI/UART interfaces access independently the register file and the user should make sure not to write the same location in the same time via both interfaces. The hardware implements Hamming 16-11 (11 bits of data and 5 parity bits) of ECC encoding / decoding to allow for correcting any single bit error and detecting any two-bit errors in a 16-bit transaction. Out of the 11 bits of data, 8 bits are used for actual data, two are used to define the transaction type (command, address or data) and one bit is used for further extensions of next parts. The commands implemented in LX4580 are register read, register write, continuous register read, continuous register write, register block read, register block write and PWM / LVDT timing reset / synchronization. Examples of generic Python, C and Verilog code are made available to implement the SPI master side of encoding / decoding. In the case of UART, one 16-bit SPI transaction is split in two equivalent 8-bit UART transactions.

11.11 JTAG interface

The JTAG is used for scan testing and debug.

11.12 Power rail regulators

The LX4580 has internal linear regulators to generate +5,25V, +5V and two +1.5V power rails. The 5.25V rail is designed to be used in conjunction with external Hall effect proximity sensors and/or optional external NVM. There is a VREF generator to generate a +1.235V reference. Additionally, a DC/DC hysteretic buck converter is available on chip and can be used to drive the inputs of the lower voltage linear regulators.

11.13 Operating modes

11.13.1 STARTUP MODE

The purpose of Startup mode is to set the LX4580 in a known initial state based on the OTP configuration memory contents and to verify its functional integrity.

Before all internal power supplies reach compliance levels, all registers are held in reset and all functional inputs and outputs are in high impedance mode.

After all power supplies reach compliance levels LX4580 will wait for the crystal oscillator (if present) to stabilize and it will enter self-test. If all the tests check the FAULT output is asserted low and FAULTB is asserted high and LX4580 enters Functional mode.

11.13.2 MANUAL RESET MODE

The purpose of Manual Reset is to allow the host processor to manually reset the LX4580 configuration and re-run the startup tests, this is useful after detecting a fault or a critical fault condition or after manual reset was commanded to the external processing from higher command levels.

When the RESET input pin is high, all registers are held in reset and all functional inputs and outputs are in high impedance mode.

After RESET is de-asserted (transitions from high to low) LX4580 will wait for the crystal oscillator (if present) to stabilize and it will enter self-test. If all the tests check the FAULT output is asserted low and FAULTB is asserted high and LX4580 enters Functional mode.

11.13.3 FUNCTIONAL MODE

The purpose of Functional mode is to provide the host processor to run extended tests on the LX4580 hardware (registers can be tested for stuck-at faults, digital filters can be tested with a known pattern, analog input sense pins can be tested for short or open condition, internal references, bias currents, ADCs can checked for consistency and calibration can be verified, internal voltage regulators can be checked for consistency using the ADCs) and also to provide synchronized filtered ADC data, to allow the host processor to control the 8 PWM drivers and two LVDT driver channels and to signal internally detected fault conditions as they occur. Additionally, during functional mode, the external processing can directly override configuration data.

During this mode both SPI / UART slave interfaces operate concurrently and can read or write registers from LX4580 allowing the external processing to do the following operations:

- Set divider for PWM1-PWM8 timing resolution.
- Set sigma-delta modulator groups divider to clock input
- Set divider determining PWM1-PWM8 cycle period
- Set individual delay for each PWM1-PWM8 with respect to the reference PWM period.
- Set individual duty cycle for PWM1-PWM8
- Set divider determining the two LVDT driver switching cycles
- Set pattern length for each of the two LVDT drivers
- Set pattern data for each of the two LVDT drivers
- Set individual sinc3 oversampling ratio for each delta-sigma modulator
- Set RMS calculation window and post RMS oversampling ratio for each of the two groups of two LVDT sense channels
- Set Critical fault mask register
- Set various digital fault limits for under / over currents and voltages measured.
- Enable self-calibration configurations
- Set GPIO configuration including support for host processor interrupts for PWM and LVDT synchronization

- Re-initialize (reset) timing origin for PWM reference cycle and for LVDT drivers pattern address pointer.
- Read SAR ADC output data for any input (or group of inputs) acquisition channel(s).
- Read delta sigma modulators output after decimation
- Read RMS data for the four LVDT input channels
- Read FAULT register status (that is driven by analog or digital comparators and internal checkers including ECC)

If a fault is identified (ADC value, supply voltage, pin voltage range is out of set bounds, un-corrected error occurs in communications or in the internal logic) the corresponding fault bit is set high. If any FAULT bit is set, then FAULT output is set high and FAULTB is set low. Also, if the FAULT_MASK register has the corresponding bit high, then LX4580 transitions into Critical Fault mode.

11.13.4 CRITICAL FAULT MODE

The purpose of the Critical Fault mode is to set the outputs of LX4580 in a state that makes the system safe. In this mode all functional inputs and outputs are in high impedance / safe mode except for the SPI / UART salve interfaces in order to allow the host processor to diagnose the fault. All fault register file updates are frozen. Exit from this mode is via manual reset or power cycling.

11.13.5 TEST MODE

The purpose of the Test mode is to exercise SCAN test, analog test and other BIST, to allow for analog calibration and testing and for analog and digital debug.

12 Registers

12.1 Master Register Map

Address	Register	Section
0x004	POR_REG1	12.2
0x201	WATCHDOG_REG1	12.3
0x202	WATCHDOG_REG2	
0x203	WATCHDOG_REG3	
0x204	WATCHDOG_REG4	
0x206	WATCHDOG_REG6	
0x207	WATCHDOG_REG7	
0x208	WATCHDOG_REG8	
0x210	CLKGEN_REG0	12.4
0x211	CLKGEN_REG1	
0x212	CLKGEN_REG2	
0x213	CLKGEN_REG3	
0x214	CLKGEN_REG4	
0x220	GLITCH_REG0	12.5
0x221	GLITCH_REG1	
0x222	GLITCH_REG2	
0x223	GLITCH_REG3	
0x224	GLITCH_REG4	
0x225	GLITCH_REG5	
0x226	GLITCH_REG6	
0x227	GLITCH_REG7	
0x228	GLITCH_REG8	
0x229	GLITCH_REG9	
0x22A	GLITCH_REGA	
0x22B	GLITCH_REGB	
0x22C	GLITCH_REGC	
0x22D	GLITCH_REGD	
0x22E	GLITCH_REGE	
0x22F	GLITCH_REGF	
0x230	GLITCH_REG10	
0x100	FAULT_REG0	12.6
0x101	FAULT_REG1	
0x102	FAULT_REG2	
0x103	FAULT_REG3	
0x104	FAULT_REG4	
0x105	FAULT_REG5	
0x106	FAULT_REG6	
0x107	FAULT_REG7	
0x108	FAULT_REG8	
0x109	FAULT_REG9	
0X10A	FAULT_REGA	
0X10B	FAULT_REGB	
0X10C	FAULT_REGC	
0x10D	FAULT_REGD	
0x10E	FAULT_REGE	
0x10F	FAULT_REGF	

Address	Register	Section
0X300	FILTER_CH12_CFG	12.7
0X301	FILTER_CH12_CFG2	
0X302	FILTER_CH12_COR	
0X308	FILTER_CH34_CFG	
0X309	FILTER_CH34_CFG2	
0X30A	FILTER_CH34_COR	
0X310	FILTER_CH1_SINC	
0X311	FILTER_CH2_SINC	
0X312	FILTER_CH3_SINC	
0X313	FILTER_CH4_SINC	
0X314	FILTER_CH1_IIR	
0X315	FILTER_CH2_IIR	
0X316	FILTER_CH3_IIR	
0X317	FILTER_CH4_IIR	
0X318	FILTER_CH1_SQAVRT	
0X319	FILTER_CH2_SQAVRT	
0X31A	FILTER_CH3_SQAVRT	
0X31B	FILTER_CH4_SQAVRT	
0X31C	FILTER_CH1_OUT	
0X31D	FILTER_CH2_OUT	
0X31E	FILTER_CH3_OUT	
0X31F	FILTER_CH4_OUT	
0X321	FILTER_IS1_CFG	
0X322	FILTER_IS2_CFG	
0X323	FILTER_IS3_CFG	
0X324	FILTER_IS4_CFG	
0X325	FILTER_IS5_CFG	
0X331	FILTER_IS1_SINC	
0X332	FILTER_IS2_SINC	
0X333	FILTER_IS3_SINC	
0X334	FILTER_IS4_SINC	
0X335	FILTER_IS5_SINC	
0X336	FILTER_IS1_IIR	
0X337	FILTER_IS2_IIR	
0X338	FILTER_IS3_IIR	
0X339	FILTER_IS4_IIR	
0X33A	FILTER_IS5_IIR	
0x400	CONTROL_REG0	12.8
0x401	CONTROL_REG1	
0x402	CONTROL_REG2	
0x403	CONTROL_REG3	
0x404	CONTROL_REG4	
0x500	STATUS_REG0	12.9
0x501	STATUS_REG1	
0x502	STATUS_REG2	
0x503	STATUS_REG3	
0x504	STATUS_REG4	
0x505	STATUS_REG5	
0x506	STATUS_REG6	

Address	Register	Section
0x600	TRIM_REG0	12.10
0x601	TRIM_REG1	
0x602	TRIM_REG2	
0x603	TRIM_REG3	
0x604	TRIM_REG4	
0x605	TRIM_REG5	
0x606	TRIM_REG6	
0x607	TRIM_REG7	
0x608	TRIM_REG8	
0x700	OTP_REG0	12.11
0x701	OTP_REG1	
0x702	OTP_REG2	
0x703	OTP_REG3	
0x704	OTP_REG4	
0x705	OTP_REG5	
0x706	OTP_REG6	
0x707	OTP_REG7	
0x800	SAR_REG0	12.12
0x801	SAR_REG1	
0x802	SAR_REG2	
0x803	SAR_REG3	
0x804	SAR_REG4	
0x805	SAR_REG5	
0x806	SAR_REG6	
0x807	SAR_REG7	
0x808	SAR_REG8	
0x809	SAR_REG9	
0x80A	SAR_REGA	
0x80B	SAR_REGB	
0x80C	SAR_REGC	
0x80D	SAR_REGD	
0x80E	SAR_REGE	
0x80F	SAR_REGF	
0x810	SAR_REG10	
0x811	SAR_REG11	
0x812	SAR_REG12	

Address	Register	Section
0x813	SAR_REG13	12.12
0x814	SAR_REG14	
0x815	SAR_REG15	
0x816	SAR_REG16	
0x817	SAR_REG17	
0x818	SAR_REG18	
0x819	SAR_REG19	
0x81A	SAR_REG1A	
0x81B	SAR_REG1B	
0x81C	SAR_REG1C	
0x81D	SAR_REG1D	
0x81E	SAR_REG1E	
0x81F	SAR_REG1F	
0x820	SAR_REG20	
0x830	SAR_REG30	
0x838	SAR_REG38	
0x840	SAR_REG40	
0x850	SAR_REG50	
0x858	SAR_REG58	
0x860	SAR_REG60	
0x870	SAR_REG70	
0x880	SAR_REG80	
0x8A0	SAR_REGA0	
0xA00	GPIO_REG0	12.13
0xA01	GPIO_REG1	
0xA02	GPIO_REG2	
0xA03	GPIO_REG3	
0xA04	GPIO_REG4	
0xA05	GPIO_REG5	
0xA06	GPIO_REG6	
0xBxx	LVDT1 registers	12.14
0xCxx	LVDT2 registers	
0xD00	UART_U1_WARN	12.15
0xD01	UART_U1_WARN_RST	
0xD02	UART_U2_WARN	
0xD03	UART_U2_WARN_RST	

12.2 POR Status Register

Address	Name	R/W	Register Contents														
			D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0x004	POR_REG1	R	-	-	-	-	-	-	-	-	-	-	1.5VD over/under-voltage status					

12.2.1 POR_REG1 REGISTER

The LX4580 implements triple comparators for both under-voltage and over-voltage detection on the critical 1.5V digital core supply voltage. Voltage detection follows triple modular redundant voting, being the state of at least two comparators.

Bit	Name	Description
0	v1v5vd_uv1	+1.5VD under-voltage comparator 1 detection state
1	v1v5vd_uv2	+1.5VD under-voltage comparator 2 detection state
2	v1v5vd_uv3	+1.5VD under-voltage comparator 3 detection state
3	v1v5vd_ov1	+1.5VD over-voltage comparator 1 detection state
4	v1v5vd_ov2	+1.5VD over-voltage comparator 2 detection state
5	v1v5vd_ov3	+1.5VD over-voltage comparator 3 detection state

12.3 Watchdog Registers

The internal watchdog operates from an independent internal 440kHz ±30kHz clock, and operates after power-up or a reset to check that the 20MHz to 30MHz system clock is operating within reasonable bounds. The serial interfaces remain inoperative until the watchdog test is complete.

There are two fault outputs: wd_clk_fault and sys_clk_fault. A fault means that either the respective clock is stuck, or that the watchdog clock and system clock are not running at the expected relative frequency. The watchdog cannot distinguish which clock (or even both) is at the wrong frequency, just that the relative frequency is outside the bounds set by the window settings.

A wd_clk_fault is a maskable fault, because by itself it does not create any functional issue, but indicates that part of the on-chip diagnostics are not functioning properly.

A sys_clk_fault indicates that there is something wrong with the 20MHz to 30MHz system clock and so is treated as a critical fault. Since this may indicate that the system clock is frozen, preventing the chip from entering a valid state, this fault will hold the chip in reset.

The watchdog configures two up-counters, the 16 bit sys_clk_counter and the 11 bit wd_clk_counter, to check the relative frequency between the watchdog clock and the system clock. Window registers set the acceptable tolerance between the two clocks. Two up/down-counters, sys_clk_counter and wd_clk_counter, count successive tests from the perspective of each clock. The up/down-counters both start at the value 2, and are incremented for each successful test, and decremented for a failure. If either counter reaches 0, the watchdog terminates with a fault. If wd_clk_counter reaches 4, the watchdog exits successfully.

The watchdog state machine operates as follows:

- The good system clock restart counter sys_count and the good system clock restart counter wd_count are set to 0x2
- The two up-counters sys_clk_counter and wd_clk_counter are cleared and start counting from system clock and watchdog clock respectively
- When the sys_clk_counter up-counter reaches the value wd_sample_size (default:10000) set in the WATCHDOG_REG3 register:
  - The value of wd_clk_counter shadowed in the WATCHDOG_REG7 register is checked to be between the lower limit wd_window_lo (default: 50) set in the WATCHDOG_REG2 register and the upper limit wd_window_hi (default:1000) set in the WATCHDOG_REG1 register
    - If shadow wd_clk_counter is within the window, then sys_count is incremented
    - If shadow wd_clk_counter is not within the window, then sys_count is decremented
  - The value of wd_clk_counter itself is also checked to be between wd_window_lo and wd_window_hi
    - If wd_clk_counter is within the window, then wd _count is incremented
    - If wd_clk_counter is not within the window, then wd _count is decremented
- If the sys_count counter has reached 0, this is treated as a watchdog fault, and the watchdog exits with a wd_clk_fault
- If the wd_count counter has reached 0, this is treated as a system clock fault, and the watchdog exits with a sys_clk_fault
- If the wd_count counter has reached 2, the watchdog exits successfully. Otherwise, the two up-counters sys_clk_counter and wd_clk_counter are cleared again and another test performed

There are two other checks that catch unusual fault scenarios:

- When the sys_clk_counter reaches a low count value, wd_ min_clk (default:500) set in the WATCHDOG_REG4 register, the watchdog counter is checked that it is not already past the lower limit wd_window_lo. This detects the case where watchdog clock is stuck and the watchdog counter is frozen in the range between wd_window_lo and wd_window_hi
- If the watchdog counter goes above the upper limit wd_window_hi during the tests, the system clock is either stopped or running very slowly. The watchdog exits with a sys_clk_fault

Address	Name	R/W	Register Contents														
			D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0x201	WATCHDOG_REG1	R/W	-	-	-	-	-	wd_window_hi[10:0]										
0x202	WATCHDOG_REG2	R/W	-	-	-	-	-	wd_window_lo[10:0]										
0x203	WATCHDOG_REG3	R/W	wd_sample_size[15:0]															
0x204	WATCHDOG_REG4	R/W	wd_ min_clk[15:0]															
0x206	WATCHDOG_REG6	R	-	-	-	-	-	wd_clk_counter[10:0]										
0x207	WATCHDOG_REG7	R	sys_clk_counter[15:0]															
0x208	WATCHDOG_REG8	R	-	-	-	-	-	-	-	-	-	-	wd_count[2:0]			sys_count[2:0]		

12.3.1 WATCHDOG_REG1 REGISTER

Bits	Name	Safe Value	Description
10 - 0	wd_window_hi[10:0]	1000	High window for watchdog
11 - 15	-	-	Unimplemented bits

12.3.2 WATCHDOG_REG2 REGISTER

Bits	Name	Safe Value	Description
10 - 0	wd_window_lo[10:0]	50	Low window for watchdog
11 - 15	-	-	Unimplemented bits

12.3.3 WATCHDOG_REG3 REGISTER

The safe value of 10000 counts reduces the 20MHz - 30MHz system clock to 2 - 3kHz, providing a watchdog window check every 333 - 500µs.

Bits	Name	Safe Value	Description
15 - 0	wd_sample_size[15:0]	10000	Number of system clocks before checking watchdog window

12.3.4 WATCHDOG_REG4 REGISTER

Bits	Name	Safe Value	Description
15 - 0	wd_min_clk[15:0]	500	Early sample to make sure watchdog clock is not stuck in the good window range

12.3.5 WATCHDOG_REG6 REGISTER

Bits	Name	Description
10 - 0	wd_clk_counter[10:0]	Shadow of the watchdog clock counter value, synchronized to the system clock
11 - 15	-	Unimplemented bits

12.3.6 WATCHDOG_REG7 REGISTER

Bits	Name	Description
15 - 0	sys_clk_counter[15:0]	Shadow of the system clock counter value, synchronized to the system clock

12.3.7 WATCHDOG_REG8 REGISTER

Bits	Name	Description
0 - 2	sys_count[2:0]	Good system clock restart count
3 - 5	wd_count[2:0]	Good watchdog clock restart count
6 - 15	-	Unimplemented bits

12.4 Clock Generator Registers

The CLKGEN_REG0, CLKGEN_REG2, CLKGEN_REG3 and CLKGEN_REG4 registers are normally configured as part of the post power-up register configuration, before any of the ISENSEx analog inputs are enabled using the CLKGEN_REG1 register. A fault will be issued if one of these 4 registers is modified while any of the ISENSEx analog inputs are enabled, or if the ISENSEx analog inputs have just been disabled but an ongoing ISENSEx acquisition sequence hasn't completed.

Address	Name	R/W	Register Contents															
			D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0x210	CLKGEN_REG0	R/W	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	pll_en
0x211	CLKGEN_REG1	R/W	-	-	-	-	-	-	-	-	lvdt_isens_ena							
0x212	CLKGEN_REG2	R/W	-	-	-	-	-	-	-	-	isense_clk_cfg							
0x213	CLKGEN_REG3	R/W	-	-	lvdt12_clk_cfg													
0x214	CLKGEN_REG4	R/W	-	-	lvdt34_clk_cfg													

12.4.1 CLKGEN_REG0 REGISTER

Bits	Name	Safe Value	Description
0	pll_en	0	When low, uses the frequency set at the OSC1 and OSC2 pins as the system clock When high, uses the internal 4x PLL as the system clock. This is 4x the frequency set at the OSC1 and OSC2 pins when the PLL is in lock
1 - 15	-	-	Unimplemented bits

12.4.2 CLKGEN_REG1 REGISTER

Configure the CLKGEN_REG0, CLKGEN_REG2, CLKGEN_REG3 and CLKGEN_REG4 registers before enabling any of the ISENSEx analog inputs.

Bits	Name	Safe Value	Description
0	isense1_en	0	When high, enables the ISENSE1 analog input at pin 60
1	isense2_en	0	When high, enables the ISENSE2 analog input at pin 61
2	isense3_en	0	When high, enables the ISENSE3 analog input at pin 62
3	isense4_en	0	When high, enables the ISENSE4 analog input at pin 63
4	isense5_en	0	When high, enables the ISENSE5 analog input at pin 64
5	lvdt12_out_en	0	When high, enables the LVDT_x1 and LVDT_x2 inputs at pins 37 to 42
6	lvdt34_out_en	0	When high, enables the LVDT_x3 and LVDT_x4 inputs at pins 43 to 48
7	clk_az_isens_en	0	When high, enables the auto-zero clock for the ISENSEx analog inputs
8 - 15	-	-	Unimplemented bits

12.4.3 CLKGEN_REG2 REGISTER

Ensure that (4 * $2^{isense\_sinc\_div}$) * (8 * isense_de_div) * (sar_pwm_mult + 1) < 2^{14} (16384) otherwise the PWM counters in the SAR ADC will overflow and issue a fault.

Bits	Name	Safe Value	Description
0 - 1	isense_de_div	0	Divides the 20 - 30MHz system clock by 8, 16, 24, or 32 for values 0 to 3
2 - 4	isense_sinc_div	0	Divides the isense_de_div output by 4 * 2^2, 4 * 2^3, 4 * 2^4, 4 * 2^5, 4 * 2^6, or 4 * 2^7 for values 2 to 7
5 - 7	sar_pwm_mult	0	PWM period = ISENSE decimation period * (sar_pwm_mult + 1)
8 - 15	-	-	Unimplemented bits

12.4.4 CLKGEN_REG3 REGISTER

Bits	Name	Safe Value	Description
0 - 4	lvdt12_de_div	0	Divides the 20 - 30MHz system clock by 8 to 32 for values 7 to 31. A fault will be issued when any of the ISENSEx analog inputs are enabled (CLKGEN_REG1) if the value here is in the range 0 to 7 at the time
5 - 12	lvdt12_sinc_div	0	Divides the lvdt12_de_div output by 8 to 256 for values 7 to 255. A fault will be issued when any of the ISENSEx analog inputs are enabled (CLKGEN_REG1) if the value here is in the range 0 to 7 at the time
13	lvdt12_osr_div	0	When low, divides the lvdt12_sinc_div output by 4 When high, divides the lvdt12_sinc_div output by 8
14 - 15	-	-	Unimplemented bits

12.4.5 CLKGEN_REG4 REGISTER

Bits	Name	Safe Value	Description
0 - 4	lvdt34_de_div	0	Divides the 20 - 30MHz system clock by 8 to 32 for values 7 to 31. A fault will be issued when any of the ISENSEx analog inputs are enabled (CLKGEN_REG1) if the value here is in the range 0 to 7 at the time
5 - 12	lvdt34_sinc_div	0	Divides the lvdt34_de_div output by 8 to 256 for values 7 to 255. A fault will be issued when any of the ISENSEx analog inputs are enabled (CLKGEN_REG1) if the value here is in the range 0 to 7 at the time
13	lvdt34_osr_div	0	When low, divides the lvdt34_sinc_div output by 4 When high, divides the lvdt34_sinc_div output by 8
14 - 15	-	-	Unimplemented bits

12.5 Fault Debounce (Glitch) Registers

The glitch registers set up debounce times for fault and status signals to allow transient alerts to be ignored.

Address	Name	R/W	Register Contents															
			D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0x220	GLITCH_REG0	R/W	-	-	-	-	-	-	-	-	fault_io_filter							
0x221	GLITCH_REG1	R	-	-	-	-	-	-	-	fault_io_counter								
0x222	GLITCH_REG2	R	-	-	-	-	-	-	-	fault_b_io_counter								
0x223	GLITCH_REG3	R/W	-	-	-	-	-	reset_filter_size										
0x224	GLITCH_REG4	R	-	-	-	-	reset_filter_counter											
0x225	GLITCH_REG5	R/W	-	-	-	-	-	-	-	-	overcurrent_wait							
0x226	GLITCH_REG6	R	-	-	-	-	-	-	-	drv1_overcurrent_counter								
0x227	GLITCH_REG7	R	-	-	-	-	-	-	-	drv2_overcurrent_counter								
0x228	GLITCH_REG8	R	-	-	-	-	-	-	-	-	-	-	-	hv fault counter				
0x229	GLITCH_REG9	R	-	-	-	-	-	-	-	-	-	-	-	drv1_fault_counter				
0x22A	GLITCH_REGA	R	-	-	-	-	-	-	-	-	-	-	-	drv2_fault_counter				
0x22B	GLITCH_REGB	R	-	-	-	-	-	-	-	-	-	-	-	vcc_uv_counter				
0x22C	GLITCH_REGC	R	-	-	-	-	-	-	-	-	-	-	-	vcc_uv_counter				
0x22D	GLITCH_REGD	R	-	-	-	-	-	-	-	-	-	-	-	vcc_uv_counter				
0x22E	GLITCH_REGE	R	-	-	-	-	-	-	-	-	-	-	-	isens_range_flt				
0x22F	GLITCH_REGF	R	-	-	-	-	-	-	-	-	-	-	-	overtemp				
0x230	GLITCH_REG10	R	-	-	-	-	-	-	-	-	-	-	-	vfb uv/ov counter				

12.5.1 GLITCH_REG0 Register

Bits	Name	Safe Value	Description
0 - 7	fault_io_filter	0x20	controls how big the filter is on fault/fault_b IO faults, units are 1/1024 sys clk each, so 0x20 (32) gives 1-1.5ms
8 - 15		-	Unimplemented bits

12.5.2 GLITCH_REG1 Register

Bits	Name	Description
0 - 8	fault_io_counter	monitor count of cycles (1/1024 sys clk) where fault out != fault receiver
9 - 15	-	Unimplemented bits

12.5.3 GLITCH_REG2 Register

Bits	Name	Description
0 - 8	fault_b_io_counter	monitor count of cycles (1/1024 sys clk) where fault_b out != fault_b receiver
9 - 15	-	Unimplemented bits

12.5.4 GLITCH_REG3 Register

Bits	Name	Safe Value	Description
0 - 10	reset_filter_size	0x20	how many (1/1024 sys clk) cycles does reset need to be high for before the chip reset will occur
11 - 15		-	Unimplemented bits

12.5.5 GLITCH_REG4 REGISTER

Bits	Name	Description
0 - 11	reset_filter_counter	monitor count of cycles (1/1024 sys clk) where reset is high
12 - 15	-	Unimplemented bits

12.5.6 GLITCH_REG5 REGISTER

Bits	Name	Safe Value	Description
0 - 7	overcurrent_wait	0x20	controls count size (1/1024 sys clk), of filter of drv1/2 overcurrent filter
8- 15		-	Unimplemented bits

12.5.7 GLITCH_REG6 REGISTER

Bits	Name	Description
0 - 8	drv1_overcurrent_counter	monitors count (1/1024 sys clk), after enabling of lvdt1 driver. Once it reaches reg5, any overcurrent will cause a fault
9 - 15	-	Unimplemented bits

12.5.8 GLITCH_REG7 REGISTER

Bits	Name	Description
0 - 8	drv2_overcurrent_counter	monitors count (1/1024 sys clk), after enabling of lvdt2 driver. Once it reaches reg5, any overcurrent will cause a fault
9 - 15	-	Unimplemented bits

12.5.9 GLITCH_REG8 REGISTER

Bits	Name	Description
0 - 4	hv fault counter	number of counts where hv1 or hv2 is faulting, when == 31(1/1024 sys clk, ~1.5ms), fault declared
5 - 15	-	Unimplemented bits

12.5.10 GLITCH_REG9 REGISTER

Bits	Name	Description
0 - 4	drv1_fault_counter	number of counts where drv1 is faulting, when == 31(1/1024 sys clk, ~1.5ms), fault declared
5 - 15	-	Unimplemented bits

12.5.11 GLITCH_REGA REGISTER

Bits	Name	Description
0 - 4	drv2_fault_counter	number of counts where drv2 is faulting, when == 31 (1/1024 sys clk, ~1.5ms), fault declared
5 - 15	-	Unimplemented bits

12.5.12 GLITCH_REGB REGISTER

Bits	Name	Description
0 - 4	vcc_uv_counter	number of counts where vcc undervoltage is faulting, when == 31 (1/1024 sys clk, ~1.5ms), fault declared
5 - 15	-	Unimplemented bits

12.5.13 GLITCH_REGC REGISTER

Bits	Name	Description
0 - 4	vcc_uv_counter	number of counts (sys clk, ~1.5us) where psX_ot is faulting, when == 31, fault declared
5 - 15	-	Unimplemented bits

12.5.14 GLITCH_REGD REGISTER

Bits	Name	Description
0 - 4	vcc_uv_counter	number of counts (sys clk, ~1.5us) where tempX is faulting, when == 31, fault declared
5 - 15	-	Unimplemented bits

12.5.15 GLITCH_REGE REGISTER

Bits	Name	Description
0 - 4	isens_range_flt	number of counts (sys clk, ~1.5us) where isens rangeX is faulting, when == 31, fault declared
5 - 15	-	Unimplemented bits

12.5.16 GLITCH_REGF REGISTER

Bits	Name	Description
0 - 4	overtemp	number of counts (sys clk/8, ~8-12us) where XXX_ot are faulting, when == 31, fault declared
5 - 15	-	Unimplemented bits

12.5.17 GLITCH_REG10 REGISTER

Bits	Name	Description
0 - 4	vfb uv/ov counter	number of counts (sys clk/1024, ~1-1.5ms) where vfb_uv/ov are faulting, when == 31, fault declared
5 - 15	-	Unimplemented bits

12.6 Fault Registers

There are 64 fault alert bits accessible in the 4 read-only fault status registers FAULT_REG0 to FAULT_REG3. Any combination of these faults are maskable by the same bit position in the 4 read-write fault mask registers FAULT_REG8 to FAULT_REGB as to whether they cause the LX4580 to initiate Safe Mode if the fault occurs. By default, all faults initiate Safe Mode.

Faults alerted in registers FAULT_REG0 to FAULT_REG3 can be cleared by clearing the same bit position in the write-only fault reset registers FAULT_REG4 to FAULT_REG7, after appropriate action has been taken to remove the issue causing the fault.

Most faults cause the FAULT pin 103 to go high and the $\overline{\text{FAULT}}$ pin 102 to go low to signal the fault. A small number of faults only affect the FAULT and $\overline{\text{FAULT}}$ pins if their fault mask register bits are clear to select Safe Mode on fault.

Address	Name	R/W	Register Contents															
			D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0x100	FAULT_REG0	R	fault_reg0															
0x101	FAULT_REG1	R	fault_reg1															
0x102	FAULT_REG2	R	fault_reg2															
0x103	FAULT_REG3	R	fault_reg3															
0x104	FAULT_REG4	W	fault_clear0															
0x105	FAULT_REG5	W	fault_clear1															
0x106	FAULT_REG6	W	fault_clear2															
0x107	FAULT_REG7	W	fault_clear3															
0x108	FAULT_REG8	R/W	fault_mask0															
0x109	FAULT_REG9	R/W	fault_mask1															
0X10A	FAULT_REGA	R/W	fault_mask2															
0X10B	FAULT_REGB	R/W	fault_mask3															
0x10C	FAULT_REGC	R	fatal_fault_reg0															
0x10D	FAULT_REGD	W	fatal_fault_clear0															
0x10E	FAULT_REGE	R/W									force_safe_override							
0x10F	FAULT_REGF	R																SM

12.6.1 FAULT_REG0 Register

Faults alerted in fault status register FAULT_REG0 can be cleared by clearing the same bit position in fault reset register FAULT_REG4, after the fault has been cleared. Any of these faults are maskable by the same bit position in fault mask FAULT_REG8 as to whether they cause the LX4580 to initiate Safe Mode if the fault occurs.

Any of these faults cause the FAULT pin 103 to go high and the $\overline{\text{FAULT}}$ pin 102 to go low to signal the fault.

Bit	Name	Description
0	gpio_fault	Set by a overloaded output in one or more GPIOs set as an output. The faulty output(s) can be identified by comparing the expected GPIO output logic levels in register GPIO_REG6 with the actual readback logic levels in register GPIO_REG5. The fault condition can be removed by setting overloaded output(s) to input(s) in register GPIO_REG3
1	-	Implemented bit with reserved function
2	clkgen_fault	fault in clockgen block. sources: #1,2 only are checked when isens_en is high (clkgen_reg1, one or more of bits 4-0 high) 1) write to clkgen_reg0/2/3/4 2) isens_sinc_div < 2 (in clkgen_reg2) 3) lvdt12_de_div < 7 or lvdt12_sinc_div < 7 3) lvdt34_de_div < 7 or lvdt34_sinc_div < 7 disable isens (write clkgen_reg1, bits 4-0 = 0). read clkgen_reg2/3/4, identify bad configuration If none are mis-configured, it was a bad write command
3	por_fault	fault in por block. v1v5d (digital supply) has fault in either uv or ov detectors fault is defined as having inconsistent results on 1 of 3 detectors for 255 cycles read uv and ov signals (POR_REG1) may require external analysis to determine whether issue is detector or actual voltage level
4	watchdog_wd_fault	fault in watchdog clock watchdog clock is failing (or frequencies mismatched between watchdog and system clock) Verify watchdog window settings given watchdog clock freqnency and oscillator clock frequency WATCHDOG_REG1, WATCHODG_REG2, WATRCHDOG_REG3, WATCHDOG_REG4 Monitor clk_wd on gpio(5/7). Monitor system clock on gpio 3/8 (only works when unlock IO high) Monitor pwm_sync period to make sure it's correct
5	fault_status_reserve	this is dependent on the use of reserve bits. There's a 16 bit register (STATUS_REG7) that's ANDed with each reserve bit. If any of the ANDs goes high, then this fault fires.
6	otp_correctable_fault	fault reading otp bits in secded mode, was correctable a single bit error was detected and corrected at power-up, means a single bit error in the trim and coms section was detected during the power-up load of otp state after power-up, means that the prior operation had a correctable bit error no action is required (it was corrected), but to understand failure, put otp in raw mode (OTP_REG5) and read out data. Check secded encoding vs data read.
7	otp_fault	a write to a register occurred at an illegal time or an attempt to program an otp bit in a locked sector write was blocked and did not happen what otp commands just occurred? A program command to a locked bit? A write when the otp controller is not in the idle state? A program command when the unlock pin is low? A write to OTP_REG0 (OTP mem address) with bena[0] low or address chosen > 127? A write to OTP_REG6 (shadow reload) that's not 16bit write or not the keyword data? A write to a trim register while shadow load is ongoing?
8	otp_error_fault	bad load of trim bits from otp memory indicates ECC error (>=2 bit) or CRC error or a stuck bit in the TRIM regs. Read trim regs, read otp mem and compare contents. If that looks good, check ECC and CRC encoding (will need to read in "raw" mode to see ECC encoding)
9	trim_fault	write to TRIM_REG0/1/2/3 when unlock_i pin low write was blocked and did not happen
10	status_fault	reserved
11	control_fault	reserved
12	sar_fault	1) fault in pwms (configuration or synchronization), 2) attempt to start new burst before last burst finishes, 3) bad sar cfg, write to SAR_REG0/1/3/6/7/8/9/10-17 when isens_enabled, 4) die temp too high for #3 or config issue in #1, they will fire when isens_en is turned on (CLKGEN_REG1[4:0]). If pwm period is too short for one sar read to finish before next sar burst starts or isens_en is not turned off for an entire burst #2 may occur. To Check #4, check die temp sar target stored values vs SAR_REGB. If none of those, must have been synchronization issue between filters and pwms. Should only be a transient glitch.
13	fault_b IO fault	fault_b IO appears stuck hi/low opposite to driven value check meta_fault_b_i and fault status, out of sync
14	fault IO fault	fault IO appears stuck hi/low opposite to driven value check meta_fault_b_i and fault status, out of sync
15	-	Implemented bit with reserved function

12.6.2 FAULT_REG1 Register

Faults alerted in fault status register FAULT_REG1 can be cleared by clearing the same bit position in fault reset register FAULT_REG5, after the fault has been cleared. Any of these faults are maskable by the same bit position in fault mask FAULT_REG9 as to whether they cause the LX4580 to initiate Safe Mode if the fault occurs.

Most of these faults cause the FAULT pin 103 to go high and the $\overline{\text{FAULT}}$ pin 102 to go low to signal the fault. Some faults only affect the FAULT and $\overline{\text{FAULT}}$ pins if their fault mask register bits in FAULT_REG9 are clear to select Safe Mode on fault. These faults are identified by a Yes in the "FAULT masked?" colum below. For these faults, if the corresponding bit 0 in fault mask FAULT_REG9 is set, then this fault will not cause the FAULT pin to go high and the $\overline{\text{FAULT}}$ pin to go low to signal the fault, as well as not initiate Safe Mode

Bit	Name	Description	FAULT masked?
0	ch2_fault_header	header (pack received out of order). Transaction is invalid. Resend the transaction	-
1	ch1_fault_header	header (pack received out of order). Transaction is invalid. Resend the transaction	-
2	ch2_fault_arbst	arbst (arbiter state register error). Arbiter state is invalid. Resend the transaction	-
3	ch1_fault_arbst	arbst (arbiter state register error). Arbiter state is invalid. Resend the transaction	-
4	ch2_fault_dbe	DED (Double Error Detected). Transaction is invalid. Resend the transaction	-
5	ch1_fault_dbe	DED (Double Error Detected). Transaction is invalid. Resend the transaction	-
6	ch2_fault_sbc	SEC (Single Error Corrected). Transaction with corrected data	-
7	ch1_fault_sbc	SEC (Single Error Corrected). Transaction with corrected data	-
8	fault_vosc	v1v5vosc overvoltage	-
9	fault_vfb	vfb under or overvoltage. Check meta_vfb_uv and meta_vfb_ov	Yes
10	fault_vbk	vbk under or overvoltage. Check meta_vbk_uv and meta_vbk_ov	Yes
11	fault_vcc	vcc overvoltage	-
12	fault_v1v5	v1v5ind under or overvoltage, v1v5ina under/over, or v1v5va under/over. Check meta_v1v5ind_uv/ov, meta_v1v5ina_uv/ov, meta_v1v5va_uv/ov	-
13	fault_v5	vc5_uv/ov, v5vin_uv/ov, v5v_uv/ov, v5ve_uv/ov. Check meta_vc5_uv/ov, meta_v5vin_uv/ov, meta_v5va_uv/ov, meta_v5ve_uv/ov	-
14	uart1_fault_frame	illegal state, or bad parity, or bad stop bit, or double bit error. These faults cause the whole transaction to be invalid. Any of these and the transaction should be abandoned and retried	-
15	uart2_fault_frame	illegal state, or bad parity, or bad stop bit, or double bit error. These faults cause the whole transaction to be invalid. Any of these and the transaction should be abandoned and retried	-

12.6.3 FAULT_REG2 REGISTER

Faults alerted in fault status register FAULT_REG2 can be cleared by clearing the same bit position in fault reset register FAULT_REG6, after the fault has been cleared. Any of these faults are maskable by the same bit position in fault mask FAULT_REGA as to whether they cause the LX4580 to initiate Safe Mode if the fault occurs.

Any of these faults cause the FAULT pin 103 to go high and the $\overline{\text{FAULT}}$ pin 102 to go low to signal the fault.

Bit	Name	Description
0	-	Implemented bit with reserved function
1	-	Implemented bit with reserved function
2	filter _fault0	LVDT ch1 RMS overflow. The MSB of the signal is outside of the range observed. So the signal will likely look like noise.
3	filter_fault1	LVDT ch2 RMS overflow. The MSB of the signal is outside of the range observed. So the signal will likely look like noise.
4	filter_fault2	LVDT ch3 RMS overflow. The MSB of the signal is outside of the range observed. So the signal will likely look like noise.
5	filter_fault3	LVDT ch4 RMS overflow. The MSB of the signal is outside of the range observed. So the signal will likely look like noise.
6	filter_fault4	iSens1 signal range overflow. The MSB of the signal is outside of the range observed. So the signal will likely look like noise.
7	filter_fault5	iSens2 signal range overflow. The MSB of the signal is outside of the range observed. So the signal will likely look like noise.
8	filter_fault6	iSens3 signal range overflow. The MSB of the signal is outside of the range observed. So the signal will likely look like noise.
9	filter_fault7	iSens4 signal range overflow. The MSB of the signal is outside of the range observed. So the signal will likely look like noise.
10	filter_fault8	iSens5 signal range overflow. The MSB of the signal is outside of the range observed. So the signal will likely look like noise.
11	lvdt2_fault	1) bist fault 2) write to LVDT_REB80/81 when isens_enabled 3) frame size or pwm_period illegal values (see reg map for LVDT_REG80/81) 4) lvdt block out of sync with filters
12	lvdt1_fault	1) bist fault 2) write to LVDT_REB80/81 when isens_enabled 3) frame size or pwm_period illegal values (see reg map for LVDT_REG80/81) 4) lvdt block out of sync with filters
13	unlock high	unlock pin is high. Considered unsafe, though you can mask it to allow operation to continue. Not unsafe by itself, but lets a lot of other things happen that are normally blocked
14	uart1_fault_noise	noise on receiver (data recovered). Caused by incosistent bit sample or single bit correction
15	uart2_fault_noise	noise on receiver (data recovered). Caused by incosistent bit sample or single bit correction

12.6.4 FAULT_REG3 Register

Faults alerted in fault status register FAULT_REG3 can be cleared by clearing the same bit position in fault reset register FAULT_REG7, after the fault has been cleared. Any of these faults are maskable by the same bit position in fault mask FAULT_REGB as to whether they cause the LX4580 to initiate Safe Mode if the fault occurs.

Most of these faults cause the FAULT pin 103 to go high and the $\overline{\text{FAULT}}$ pin 102 to go low to signal the fault. Some faults only affect the FAULT and $\overline{\text{FAULT}}$ pins if their fault mask register bits in FAULT_REGB are clear to select Safe Mode on fault. These faults are identified by a Yes in the "FAULT masked?" colum below. For these faults, if the corresponding bit 0 in fault mask FAULT_REGB is set, then this fault will not cause the FAULT pin to go high and the $\overline{\text{FAULT}}$ pin to go low to signal the fault, as well as not initiate Safe Mode

Bit	Name	Description	FAULT masked?
0	fault_isens_range_flt	isens1/2/3/4/5 or return voltage out of range, appears to be floating. Check sar readings	Yes
1	fault_lvdt2_flt	lvdt3/4 p/n appear to be floating. Check sar readings	Yes
2	fault_lvdt1_flt	lvdt1/2 p/n appear to be floating. Check sar readings	Yes
3	fault_drv2_flt	drv2 p/n appear to be floating. Probably fatal	Yes
4	fault_drv1_flt	drv1 p/n appear to be floating. Probably fatal	Yes
5	fault_hv	hv1 or hv2 appear to be floating	Yes
6	fault_pressure	ps1/2/3 overtemp. Check meta_ps1/2/3_src_ot	-
7	fault_temp_float	temp1/2/3/4/5 appear to be floating. Check meta_temp1/2/3/4/5	Yes
8	fault_drv2_ot	drv2 p/n overtemp condition . Check meta_drv2p/n_ot	-
9	fault_drv1_ot	drv1 p/n overtemp condition. Check meta_drv1p/n_ot	-
10	fault_drv2_ovc	drv2 overcurrent condition. Check meta_drv2_ovc	-
11	fault_drv1_ovc	drv1 overcurrent condition. Check meta_drv1_ovc	-
12	pll unlock	pll is not locked. Read pll lock signal in status reg	-
13	fault_vcc_uv	filtered (1ms) response to vcc_uv. Puts the chip in safe mode. Do not mask	-
14	meta_vcc_uv	immediate response to vcc uv. may be masked, in case vcc_uv glitches. vcc is low, can be confirmed with the sar. Read status reg of vcc_uv to confirm uv status	-
15	fault_ot	overtemp on buck, v5v,/v5ve, v1v5va, v1v5vd.. Check meta_v5v_v5ve_ot, meta_v1v5vd_ot, meta_v1v5va_ot, meta_buck_ot. These power supplies automatically cut off if overtemp is detected	-

12.6.5 FAULT_REG4 Register

Faults alerted in fault status register FAULT_REG0 can be cleared by clearing the same bit position in fault reset register FAULT_REG4, after the fault has been cleared. Any of these faults cause the FAULT pin 103 to go high and the $\overline{\text{FAULT}}$ pin 102 to go low to signal the fault.

Bit	Name	Description
0	gpio_fault	Set this bit to clearing the same bit position in FAULT_REG0
1	-	Implemented bit with reserved function
2	clkgen_fault	Set this bit to clearing the same bit position in FAULT_REG0
3	por_fault	Set this bit to clearing the same bit position in FAULT_REG0
4	watchdog_wd_fault	Set this bit to clearing the same bit position in FAULT_REG0
5	fault_status_reserve	Set this bit to clearing the same bit position in FAULT_REG0
6	otp_correctable_fault	Set this bit to clearing the same bit position in FAULT_REG0
7	otp_fault	Set this bit to clearing the same bit position in FAULT_REG0
8	otp_error_fault	Set this bit to clearing the same bit position in FAULT_REG0
9	trim_fault	Set this bit to clearing the same bit position in FAULT_REG0
10	status_fault	reserved
11	control_fault	reserved
12	sar_fault	Set this bit to clearing the same bit position in FAULT_REG0
13	fault_b IO fault	Set this bit to clearing the same bit position in FAULT_REG0
14	fault IO fault	Set this bit to clearing the same bit position in FAULT_REG0
15	-	

12.6.6 FAULT_REG5 Register

Faults alerted in fault status register FAULT_REG1 can be cleared by clearing the same bit position in fault reset register FAULT_REG5, after the fault has been cleared.

Most of these faults cause the FAULT pin 103 to go high and the $\overline{\text{FAULT}}$ pin 102 to go low to signal the fault. Some faults only affect the FAULT and $\overline{\text{FAULT}}$ pins if their fault mask register bits in FAULT_REG9 are clear to select Safe Mode on fault. These faults are identified by a Yes in the "FAULT masked?" colum below. For these faults, if the corresponding bit 0 in fault mask FAULT_REG9 is set, then this fault will not cause the FAULT pin to go high and the $\overline{\text{FAULT}}$ pin to go low to signal the fault, as well as not initiate Safe Mode

Bit	Name	Description	FAULT masked?
0	ch2_fault_header	Set this bit to clearing the same bit position in FAULT_REG1	-
1	ch1_fault_header	Set this bit to clearing the same bit position in FAULT_REG1	-
2	ch2_fault_arbst	Set this bit to clearing the same bit position in FAULT_REG1	-
3	ch1_fault_arbst	Set this bit to clearing the same bit position in FAULT_REG1	-
4	ch2_fault_dbe	Set this bit to clearing the same bit position in FAULT_REG1	-
5	ch1_fault_dbe	Set this bit to clearing the same bit position in FAULT_REG1	-
6	ch2_fault_sbc	Set this bit to clearing the same bit position in FAULT_REG1	-
7	ch1_fault_sbc	Set this bit to clearing the same bit position in FAULT_REG1	-
8	fault_vosc	Set this bit to clearing the same bit position in FAULT_REG1	-
9	fault_vfb	Set this bit to clearing the same bit position in FAULT_REG1	Yes
10	fault_vbk	Set this bit to clearing the same bit position in FAULT_REG1	Yes
11	fault_vcc	Set this bit to clearing the same bit position in FAULT_REG1	-
12	fault_v1v5	Set this bit to clearing the same bit position in FAULT_REG1	-
13	fault_v5	Set this bit to clearing the same bit position in FAULT_REG1	-
14	uart1_fault_frame	Set this bit to clearing the same bit position in FAULT_REG1	-
15	uart2_fault_frame	Set this bit to clearing the same bit position in FAULT_REG1	-

12.6.7 FAULT_REG6 Register

Faults alerted in fault status register FAULT_REG2 can be cleared by clearing the same bit position in fault reset register FAULT_REG6, after the fault has been cleared.

Any of these faults cause the FAULT pin 103 to go high and the $\overline{\text{FAULT}}$ pin 102 to go low to signal the fault.

Bit	Name	Description
0	-	Implemented bit with reserved function
1	-	Implemented bit with reserved function
2	filter _fault0	Set this bit to clearing the same bit position in FAULT_REG2
3	filter_fault1	Set this bit to clearing the same bit position in FAULT_REG2
4	filter_fault2	Set this bit to clearing the same bit position in FAULT_REG2
5	filter_fault3	Set this bit to clearing the same bit position in FAULT_REG2
6	filter_fault4	Set this bit to clearing the same bit position in FAULT_REG2
7	filter_fault5	Set this bit to clearing the same bit position in FAULT_REG2
8	filter_fault6	Set this bit to clearing the same bit position in FAULT_REG2
9	filter_fault7	Set this bit to clearing the same bit position in FAULT_REG2
10	filter_fault8	Set this bit to clearing the same bit position in FAULT_REG2
11	lvdt2_fault	Set this bit to clearing the same bit position in FAULT_REG2
12	lvdt1_fault	Set this bit to clearing the same bit position in FAULT_REG2
13	unlock high	Set this bit to clearing the same bit position in FAULT_REG2
14	uart1_fault_noise	Set this bit to clearing the same bit position in FAULT_REG2
15	uart2_fault_noise	Set this bit to clearing the same bit position in FAULT_REG2

12.6.8 FAULT_REG7 Register

Faults alerted in fault status register FAULT_REG3 can be cleared by clearing the same bit position in fault reset register FAULT_REG7, after the fault has been cleared.

Most of these faults cause the FAULT pin 103 to go high and the $\overline{\text{FAULT}}$ pin 102 to go low to signal the fault. Some faults only affect the FAULT and $\overline{\text{FAULT}}$ pins if their fault mask register bits in FAULT_REGB are clear to select Safe Mode on fault. These faults are identified by a Yes in the "FAULT masked?" colum below. For these faults, if the corresponding bit 0 in fault mask FAULT_REGB is set, then this fault will not cause the FAULT pin to go high and the $\overline{\text{FAULT}}$ pin to go low to signal the fault, as well as not initiate Safe Mode

Bit	Name	Description	FAULT masked?
0	fault_isens_range_flt	Set this bit to clearing the same bit position in FAULT_REG1	Yes
1	fault_lvdt2_flt	Set this bit to clearing the same bit position in FAULT_REG1	Yes
2	fault_lvdt1_flt	Set this bit to clearing the same bit position in FAULT_REG1	Yes
3	fault_drv2_flt	Set this bit to clearing the same bit position in FAULT_REG1	Yes
4	fault_drv1_flt	Set this bit to clearing the same bit position in FAULT_REG1	Yes
5	fault_hv	Set this bit to clearing the same bit position in FAULT_REG1	Yes
6	fault_pressure	Set this bit to clearing the same bit position in FAULT_REG1	-
7	fault_temp_float	Set this bit to clearing the same bit position in FAULT_REG1	Yes
8	fault_drv2_ot	Set this bit to clearing the same bit position in FAULT_REG1	-
9	fault_drv1_ot	Set this bit to clearing the same bit position in FAULT_REG1	-
10	fault_drv2_ovc	Set this bit to clearing the same bit position in FAULT_REG1	-
11	fault_drv1_ovc	Set this bit to clearing the same bit position in FAULT_REG1	-
12	pll unlock	Set this bit to clearing the same bit position in FAULT_REG1	-
13	fault_vcc_uv	Set this bit to clearing the same bit position in FAULT_REG1	-
14	meta_vcc_uv	Set this bit to clearing the same bit position in FAULT_REG1	-
15	fault_ot	Set this bit to clearing the same bit position in FAULT_REG1	-

12.6.9 FAULT_REG8 Register

Faults alerted in fault status register FAULT_REG0 are maskable by the same bit position in fault mask register FAULT_REG8 as to whether they cause the LX4580 to initiate Safe Mode if the fault occurs.

Any of these faults cause the FAULT pin 103 to go high and the $\overline{\text{FAULT}}$ pin 102 to go low to signal the fault.

Bit	Name	Safe Value	Description
0	gpio_fault	0	Set this bit to prevent the LX4580 from entering Safe Mode if the fault occurs
1	-	-	Implemented bit with reserved function
2	clkgen_fault	0	Set this bit to prevent the LX4580 from entering Safe Mode if the fault occurs
3	por_fault	0	Set this bit to prevent the LX4580 from entering Safe Mode if the fault occurs
4	watchdog_wd_fault	0	Set this bit to prevent the LX4580 from entering Safe Mode if the fault occurs
5	fault_status_reserve	0	Set this bit to prevent the LX4580 from entering Safe Mode if the fault occurs
6	otp_correctable_fault	0	Set this bit to prevent the LX4580 from entering Safe Mode if the fault occurs
7	otp_fault	0	Set this bit to prevent the LX4580 from entering Safe Mode if the fault occurs
8	otp_error_fault	0	Set this bit to prevent the LX4580 from entering Safe Mode if the fault occurs
9	trim_fault	0	Set this bit to prevent the LX4580 from entering Safe Mode if the fault occurs
10	status_fault	0	reserved
11	control_fault	0	reserved
12	sar_fault	0	Set this bit to prevent the LX4580 from entering Safe Mode if the fault occurs
13	fault_b IO fault	0	Set this bit to prevent the LX4580 from entering Safe Mode if the fault occurs
14	fault IO fault	0	Set this bit to prevent the LX4580 from entering Safe Mode if the fault occurs
15	-	-	

12.6.10 FAULT_REG9 REGISTER

Faults alerted in fault status register FAULT_REG1 are maskable by the same bit position in fault mask register FAULT_REG9 as to whether they cause the LX4580 to initiate Safe Mode if the fault occurs.

Most of these faults cause the FAULT pin 103 to go high and the $\overline{\text{FAULT}}$ pin 102 to go low to signal the fault. Some faults only affect the FAULT and $\overline{\text{FAULT}}$ pins if their fault mask register bits in FAULT_REG9 are clear to select Safe Mode on fault. These faults are identified by a Yes in the "FAULT masked?" colum below. For these faults, if the corresponding bit 0 in fault mask FAULT_REG9 is set, then this fault will not cause the FAULT pin to go high and the $\overline{\text{FAULT}}$ pin to go low to signal the fault, as well as not initiate Safe Mode

Bit	Name	Safe Value	Description	FAULT masked?
0	ch2_fault_header	0	Set this bit to prevent the LX4580 from entering Safe Mode if the fault occurs	-
1	ch1_fault_header	0	Set this bit to prevent the LX4580 from entering Safe Mode if the fault occurs	-
2	ch2_fault_arbst	0	Set this bit to prevent the LX4580 from entering Safe Mode if the fault occurs	-
3	ch1_fault_arbst	0	Set this bit to prevent the LX4580 from entering Safe Mode if the fault occurs	-
4	ch2_fault_dbe	0	Set this bit to prevent the LX4580 from entering Safe Mode if the fault occurs	-
5	ch1_fault_dbe	0	Set this bit to prevent the LX4580 from entering Safe Mode if the fault occurs	-
6	ch2_fault_sbc	0	Set this bit to prevent the LX4580 from entering Safe Mode if the fault occurs	-
7	ch1_fault_sbc	0	Set this bit to prevent the LX4580 from entering Safe Mode if the fault occurs	-
8	fault_vosc	0	Set this bit to prevent the LX4580 from entering Safe Mode if the fault occurs	-
9	fault_vfb	0	Set this bit to prevent the LX4580 from entering Safe Mode if the fault occurs	Yes
10	fault_vbk	0	Set this bit to prevent the LX4580 from entering Safe Mode if the fault occurs	Yes
11	fault_vcc	0	Set this bit to prevent the LX4580 from entering Safe Mode if the fault occurs	-
12	fault_v1v5	0	Set this bit to prevent the LX4580 from entering Safe Mode if the fault occurs	-
13	fault_v5	0	Set this bit to prevent the LX4580 from entering Safe Mode if the fault occurs	-
14	uart1_fault_frame	0	Set this bit to prevent the LX4580 from entering Safe Mode if the fault occurs	-
15	uart2_fault_frame	0	Set this bit to prevent the LX4580 from entering Safe Mode if the fault occurs	-

12.6.11 FAULT_REGA REGISTER

Faults alerted in fault status register FAULT_REG2 are maskable by the same bit position in fault mask register FAULT_REGA as to whether they cause the LX4580 to initiate Safe Mode if the fault occurs.

Any of these faults cause the FAULT pin 103 to go high and the $\overline{\text{FAULT}}$ pin 102 to go low to signal the fault.

Bit	Name	Safe Value	Description
0	-	-	Implemented bit with reserved function
1	-	-	Implemented bit with reserved function
2	filter _fault0	0	Set this bit to prevent the LX4580 from entering Safe Mode if the fault occurs
3	filter_fault1	0	Set this bit to prevent the LX4580 from entering Safe Mode if the fault occurs
4	filter_fault2	0	Set this bit to prevent the LX4580 from entering Safe Mode if the fault occurs
5	filter_fault3	0	Set this bit to prevent the LX4580 from entering Safe Mode if the fault occurs
6	filter_fault4	0	Set this bit to prevent the LX4580 from entering Safe Mode if the fault occurs
7	filter_fault5	0	Set this bit to prevent the LX4580 from entering Safe Mode if the fault occurs
8	filter_fault6	0	Set this bit to prevent the LX4580 from entering Safe Mode if the fault occurs
9	filter_fault7	0	Set this bit to prevent the LX4580 from entering Safe Mode if the fault occurs
10	filter_fault8	0	Set this bit to prevent the LX4580 from entering Safe Mode if the fault occurs
11	lvdt2_fault	0	Set this bit to prevent the LX4580 from entering Safe Mode if the fault occurs
12	lvdt1_fault	0	Set this bit to prevent the LX4580 from entering Safe Mode if the fault occurs
13	unlock high	0	Set this bit to prevent the LX4580 from entering Safe Mode if the fault occurs
14	uart1_fault_noise	0	Set this bit to prevent the LX4580 from entering Safe Mode if the fault occurs
15	uart2_fault_noise	0	Set this bit to prevent the LX4580 from entering Safe Mode if the fault occurs

12.6.12 FAULT_REGB REGISTER

Faults alerted in fault status register FAULT_REG3 are maskable by the same bit position in fault mask register FAULT_REGB as to whether they cause the LX4580 to initiate Safe Mode if the fault occurs.

Most of these faults cause the FAULT pin 103 to go high and the $\overline{\text{FAULT}}$ pin 102 to go low to signal the fault. Some faults only affect the FAULT and $\overline{\text{FAULT}}$ pins if their fault mask register bits in FAULT_REGB are clear to select Safe Mode on fault. These faults are identified by a Yes in the "FAULT masked?" colum below. For these faults, if the corresponding bit 0 in fault mask FAULT_REGB is set, then this fault will not cause the FAULT pin to go high and the $\overline{\text{FAULT}}$ pin to go low to signal the fault, as well as not initiate Safe Mode

Bit	Name	Safe Value	Description	FAULT masked?
0	fault_isens_range_flt	0	Set this bit to prevent the LX4580 from entering Safe Mode if the fault occurs	Yes
1	fault_lvdt2_flt	0	Set this bit to prevent the LX4580 from entering Safe Mode if the fault occurs	Yes
2	fault_lvdt1_flt	0	Set this bit to prevent the LX4580 from entering Safe Mode if the fault occurs	Yes
3	fault_drv2_flt	0	Set this bit to prevent the LX4580 from entering Safe Mode if the fault occurs	Yes
4	fault_drv1_flt	0	Set this bit to prevent the LX4580 from entering Safe Mode if the fault occurs	Yes
5	fault_hv	0	Set this bit to prevent the LX4580 from entering Safe Mode if the fault occurs	Yes
6	fault_pressure	0	Set this bit to prevent the LX4580 from entering Safe Mode if the fault occurs	-
7	fault_temp_float	0	Set this bit to prevent the LX4580 from entering Safe Mode if the fault occurs	Yes
8	fault_drv2_ot	0	Set this bit to prevent the LX4580 from entering Safe Mode if the fault occurs	-
9	fault_drv1_ot	0	Set this bit to prevent the LX4580 from entering Safe Mode if the fault occurs	-
10	fault_drv2_ovc	0	Set this bit to prevent the LX4580 from entering Safe Mode if the fault occurs	-
11	fault_drv1_ovc	0	Set this bit to prevent the LX4580 from entering Safe Mode if the fault occurs	-
12	pll unlock	0	Set this bit to prevent the LX4580 from entering Safe Mode if the fault occurs	-
13	fault_vcc_uv	0	Set this bit to prevent the LX4580 from entering Safe Mode if the fault occurs	-
14	meta_vcc_uv	0	Set this bit to prevent the LX4580 from entering Safe Mode if the fault occurs	-
15	fault_ot	0	Set this bit to prevent the LX4580 from entering Safe Mode if the fault occurs	-

12.6.13 FAULT_REGC AND FAULT_REGD REGISTERS

Faults alerted in fault status register FAULT_REGC are deemed to be critical, and cause the LX4580 to enter severe safe mode. All registers except FAULT_REGC lose their data, and both the FAULT pin 103 and the $\overline{\text{FAULT}}$ pin 102 go low to signal a critical fault.

The serial busses are also disabled during critical fault, and the external system must determine and correct the fault(s) before the LX4580 can be accessed. The LX4580 will indicate recovery by taking the FAULT pin high. The fault status register FAULT_REGC can then be read to check which critical faults were latched.

Faults alerted in register FAULT_REGC can be cleared by clearing the same bit position in the write-only fault reset register FAULT_REGD.

Bit	Name	Description
0	vdd_ov	VDD I/O supply voltage is high
1	vdd_uv	VDD I/O supply voltage is too low
2	-	
3	sys_clk_fault	Watchdog has detected that the 20MHz to 30MHz system clock is slow or stuck
4	v1v5d_ov_fault	1.5V digital core supply voltage is too high
5	v1v4d_uv_fault	1.5V digital core supply voltage is too low
6 - 15	-	

12.6.14 FAULT_REGE REGISTER

Writing 0xC3 to FAULT_REGE forces the LX4580 into safe mode, tri-stating all outputs except the serial and JTAG interfaces. Write another value to FAULT_REGE or take the RESET pin high which clears the register to exit forced safe mode.

Address	Action	R/W	Register Contents															
			D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0x10E	Force safe mode	R/W	-	-	-	-	-	-	-	-	1	1	0	0	0	0	1	1
	Normal operation		-	-	-	-	-	-	-	-	Any value but 0xC3							

12.6.15 FAULT_REGF REGISTER

The read-only FAULT_REGE register provides safe mode status.

Bit	Name	Description
0	safe_mode	High indicates that the LX4580 is in safe mode
1 - 15	-	

12.7 Filter Registers

Address	Name	R/W	Register Contents															
			D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0X300	FILTER_CH12_CFG1	R/W																
0X301	FILTER_CH12_CFG2	R/W																
0X302	FILTER_CH12_COR	R/W																
0X308	FILTER_CH34_CFG1	R																
0X309	FILTER_CH34_CFG2	R																
0X30A	FILTER_CH34_COR	R																
0X310	FILTER_CH1_SINC	R																
0X311	FILTER_CH2_SINC	R																
0X312	FILTER_CH3_SINC	R																
0X313	FILTER_CH4_SINC	R																
0X314	FILTER_CH1_IIR	R																
0X315	FILTER_CH2_IIR	R/W																
0X316	FILTER_CH3_IIR	R/W																
0X317	FILTER_CH4_IIR	R/W																
0X318	FILTER_CH1_SQAVRT	R																
0X319	FILTER_CH2_SQAVRT	R																
0X31A	FILTER_CH3_SQAVRT	R																
0X31B	FILTER_CH4_SQAVRT	R																
0X31C	FILTER_CH1_OUT	R																
0X31D	FILTER_CH2_OUT	R																
0X31E	FILTER_CH3_OUT	R																
0X31F	FILTER_CH4_OUT	R																
0X321	FILTER_IS1_CFG	R/W																
0X322	FILTER_IS2_CFG	R																
0X323	FILTER_IS3_CFG	R																
0X324	FILTER_IS4_CFG	R/W																
0X325	FILTER_IS5_CFG	R																
0X331	FILTER_IS1_SINC	R																
0X332	FILTER_IS2_SINC	R/W																
0X333	FILTER_IS3_SINC	R																
0X334	FILTER_IS4_SINC	R																
0X335	FILTER_IS5_SINC	R/W																
0X336	FILTER_IS1_IIR	R																
0X337	FILTER_IS2_IIR	R																
0X338	FILTER_IS3_IIR	R/W																
0X339	FILTER_IS4_IIR	R																
0X33A	FILTER_IS5_IIR	R																

12.7.1 FILTER_CH12_CFG1 Register

Bits	Name	Safe Value	Description
0 - 3	decay12	10	iir decay factor (for removing DC offset)
4 - 7	sinc12_gain	4	gain of the sinc filter
8 - 9	avg12_gain	2	for high frequency signals this gain can give more definition
10	avg12_abs	0	use absolute value instead of RMS for averager
11	iir12_en	1	enable the iir filter
12	pwm12_en	0	input to ch1 and ch2 filters are feedback from pwm1 and pwm2 instead of the SigmaDelta channels
13 - 15	-	-	Unimplemented bits

12.7.2 FILTER_CH12_CFG2 REGISTER

Bits	Name	Safe Value	Description
0 - 2	n312_gain	0	gain of the n3sinc filter
3	sqavrt12_bypass	0	use the rectified only signal as input to last sinc filter
4	avg12_16	1	0: average last 8 samples; 1 : averages last 16 samples
10 - 15	-	-	Unimplemented bits

12.7.3 FILTER_CH12_COR REGISTER

Bits	Name	Safe Value	Description
0 - 15	correction12	0	dc offset correction factor

12.7.4 FILTER_CH1_SINC REGISTER

Bit	Name	Description
0 - 15	ch1_sinc	output from sinc_n8 stage

12.7.5 FILTER_CH1_IIR REGISTER

Bit	Name	Description
0 - 15	ch1_iir	output from iir stage

12.7.6 FILTER_CH1_SQAVRT REGISTER

Bit	Name	Description
0 - 15	ch1_sqavrt	output from RMS stage

12.7.7 FILTER_CH1_OUT REGISTER

Bit	Name	Description
0 - 15	ch1_out	output from sinc_n3 stage

12.7.8 FILTER_CH2_SINC REGISTER

Bit	Name	Description
0 - 15	ch2_sinc	output from sinc_n8 stage

12.7.9 FILTER_CH2_IIR REGISTER

Bit	Name	Description
0 - 15	ch2_iir	output from iir stage

12.7.10 FILTER_CH2_SQAVRT REGISTER

Bit	Name	Description
0 - 15	ch2_sqavrt	output from RMS stage

12.7.11 FILTER_CH2_OUT REGISTER

Bit	Name	Description
0 - 15	ch2_out	output from sinc_n3 stage

12.7.12 FILTER_CH34_CFG1 REGISTER

Bits	Name	Safe Value	Description
0 - 3	decay34	10	iir decay factor (for removing DC offset)
4 - 7	sinc34_gain	4	gain of the sinc filter
8 - 9	avg34_gain	2	for high frequency signals this gain can give more definition
10	avg34_abs	0	use absolute value instead of RMS for averager
11	iir34_en	1	enable the iir filter
12	pwm34_en	0	input to ch3 and ch4 filters are feedback from pwm3 and pwm4 instead of the SigmaDelta channels
13 - 15	-	-	Unimplemented bits

12.7.13 FILTER_CH34_CFG2 REGISTER

Bits	Name	Safe Value	Description
0 - 2	n334_gain	0	gain of the n3sinc filter
3	sqavrt34_bypass	0	use the rectified only signal as input to last sinc filter
4	avg34_16	1	0: average last 8 samples; 1 : averages last 16 samples
10 - 15	-	-	Unimplemented bits

12.7.14 FILTER_CH34_COR REGISTER

Bits	Name	Safe Value	Description
0 - 15	correction34	0	dc offset correction factor

12.7.15 FILTER_CH3_SINC REGISTER

Bit	Name	Description
0 - 15	ch3_sinc	output from sinc_n8 stage

12.7.16 FILTER_CH3_IIR REGISTER

Bit	Name	Description
0 - 15	ch3_iir	output from iir stage

12.7.17 FILTER_CH3_SQAVRT REGISTER

Bit	Name	Description
0 - 15	ch3_sqavrt	output from RMS stage

12.7.18 FILTER_CH3_OUT REGISTER

Bit	Name	Description
0 - 15	ch3_out	output from sinc_n3 stage

12.7.19 FILTER_CH4_SINC REGISTER

Bit	Name	Description
0 - 15	ch4_sinc	output from sinc_n8 stage

12.7.20 FILTER_CH4_IIR REGISTER

Bit	Name	Description
0 - 15	ch4_iir	output from iir stage

12.7.21 FILTER_CH4_SQAVRT REGISTER

Bit	Name	Description
0 - 15	ch4_sqavrt	output from RMS stage

12.7.22 FILTER_CH4_OUT REGISTER

Bit	Name	Description
0 - 15	ch4_out	output from sinc_n3 stage

12.7.23 FILTER_IS1_CFG REGISTER

Bits	Name	Safe Value	Description
0 - 3	isens1_decay	0xA	iir decay factor (for removing DC offset)
4 - 7	isens1_sinc_gain	7	gain of the sinc n11 filter
8	isens1_pwm_en	0	input to isens is feedback from pwm5 instead of the ΣΔ channel
9 - 15	-	-	Unimplemented bits

12.7.24 FILTER_IS1_SINC REGISTER

Bit	Name	Description
0 - 15	isens1_sinc_out	output from sinc_n11 stage

12.7.25 FILTER_IS1_IIR REGISTER

Bit	Name	Description
0 - 15	isens1_iir_out	output from iir stage

12.7.26 FILTER_IS2_CFG REGISTER

Bits	Name	Safe Value	Description
0 - 3	isens2_decay	0xA	iir decay factor (for removing DC offset)
4 - 7	isens2_sinc_gain	7	gain of the sinc n11 filter
8	isens2_pwm_en	0	input to isens is feedback from pwm6 instead of the ΣΔ channel
9 - 15	-	-	Unimplemented bits

12.7.27 FILTER_IS2_SINC REGISTER

Bit	Name	Description
0 - 15	isens2_sinc_out	output from sinc_n11 stage

12.7.28 FILTER_IS2_IIR REGISTER

Bit	Name	Description
0 - 15	isens2_iir_out	output from iir stage

12.7.29 FILTER_IS3_CFG REGISTER

Bits	Name	Safe Value	Description
0 - 3	isens3_decay	0xA	iir decay factor (for removing DC offset)
4 - 7	isens3_sinc_gain	7	gain of the sinc n11 filter
8	isens3_pwm_en	0	input to isens is feedback from pwm7 instead of the ΣΔ channel
9 - 15	-	-	Unimplemented bits

12.7.30 FILTER_IS3_SINC REGISTER

Bit	Name	Description
0 - 15	isens3_sinc_out	output from sinc_n11 stage

12.7.31 FILTER_IS3_IIR REGISTER

Bit	Name	Description
0 - 15	isens3_iir_out	output from iir stage

12.7.32 FILTER_IS4_CFG REGISTER

Bits	Name	Safe Value	Description
0 - 3	isens4_decay	0xA	iir decay factor (for removing DC offset)
4 - 7	isens4_sinc_gain	7	gain of the sinc n11 filter
8	isens4_pwm_en	0	input to isens is feedback from pwm8 (same option as isens5) instead of the ΣΔ channel
9 - 15	-	-	Unimplemented bits

12.7.33 FILTER_IS4_SINC REGISTER

Bit	Name	Description
0 - 15	isens4_sinc_out	output from sinc_n11 stage

12.7.34 FILTER_IS4_IIR REGISTER

Bit	Name	Description
0 - 15	isens4_iir_out	output from iir stage

12.7.35 FILTER_IS5_CFG REGISTER

Bits	Name	Safe Value	Description
0 - 3	isens5_decay	0xA	iir decay factor (for removing DC offset)
4 - 7	isens5_sinc_gain	7	gain of the sinc n11 filter
8	isens5_pwm_en	0	input to isens is feedback from pwm8 (same option as isens4) instead of the ΣΔ channel
9 - 15	-	-	Unimplemented bits

12.7.36 FILTER_IS5_SINC REGISTER

Bit	Name	Description
0 - 15	isens5_sinc_out	output from sinc_n11 stage

12.7.37 FILTER_IS5_IIR REGISTER

Bit	Name	Description
0 - 15	isens5_iir_out	output from iir stage

12.8 Control Registers

Address	Name	R/W	Register Contents															
			D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0x400	CONTROL_REG0	R/W	-	-	-	-	-	-	temp[4:0]_pt_sel					isens[4:0]_in_puen				
0x401	CONTROL_REG1	R/W	-	-	-	LVDT control												
0x402	CONTROL_REG2	R/W	reserved_control															
0x403	CONTROL_REG3	R/W	test2_tstadr[4:0]					test1_tstadr[4:0]					test2			test1		
0x404	CONTROL_REG4	R/W	-	-	-	-	-	-	Test controls									

12.8.1 CONTROL_REG0 REGISTER

Bits	Name	Safe Value	Description
0 - 4	isens[4:0]_in_puen	0	
5 - 9	temp[4:0]_pt_sel	0	
10 - 15	-	-	Unimplemented bits

12.8.2 CONTROL_REG1 REGISTER

Bits	Name	Safe Value	Description
0	lvdt12_in_float_sense_en	0	
1	lvdt34_in_float_sense_en	0	
2	drvsns1_float_det_en	0	
3	drvsns2_float_det_en	0	
4	drvsns1_shortgnd_det_en	0	
5	drvsns2_shortgnd_det_en	0	
6	hvp_float_det_en	0	
7	hvp_shortgnd_det_en	0	
8	drvsns1_shortv1v5va_det_en	0	
9	drvsns2_shortv1v5va_det_en	0	
10	hvp_shortv1v5va_det_en	0	
11	lvdt_mods_bisten	0	
12	isense_mods_bisten	0	
13 - 15	-	-	Unimplemented bits

12.8.3 CONTROL_REG2 REGISTER

Bits	Name	Safe Value	Description
0		0	double bridges current threshold limit when enabled
1		0	override bridges input whit GPI9 when enabled if unlock is high
2		0	when default state 0 clkout pin is enabled, when high clkout pin is disabled
3		0	VBG override with REF_IN
4 - 8	-	-	Unimplemented bits
9		0	enables optional ss_n high mode on spi ports
10 - 13	-	-	Unimplemented bits
14		0	V1R2a
15		0	V1R2b

12.8.4 CONTROL_REG3 REGISTER

Bits	Name	Safe Value	Description
0	test1_dig_o	-	
1	test1_dig_oe	0	
2	test1_ana_ioe	0	
3	test2_dig_o	-	
4	test2_dig_oe	0	
5	test2_ana_ioe	0	
6 - 10	test1_tstadr	0x00	
11 - 15	test21_tstadr	0x00	

12.8.5 CONTROL_REG4 REGISTER

Bits	Name	Safe Value	Description
0	ts_cells_tsten	0	
1	clk_az_tstbus_disable_en	0	
2	bridges_icl_disable	0	
7 - 3	isens[5:1]_mod_tsten	0x00	
9 - 8	sar_test	0x0	
10 - 15	-	-	Unimplemented bits

12.9 Status Registers

Address	Name	R/W	Register Contents															
			D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0x500	STATUS_REG0	R	FAULT outputs, UNLOCK input, UART_EN input, PLL lock, supply over/under-voltage statuses															
0x501	STATUS_REG1	R	-	-	-	RESET input, supply over/under-voltage statuses												
0x502	STATUS_REG2	R	-	-	Hall inputs, 4-20mA and LVDT over-temperature, LVDT over-current													
0x503	STATUS_REG3	R	-	-	LVDT and current sense input faults													
0x504	STATUS_REG4	R	-	LVDT voltage sense input, HV, temperature inputs, and regulator over-temperature faults														
0x505	STATUS_REG5	R	Reserve status bits															
0x506	STATUS_REG6	R/W	Enable/disable for reserve status bits															

12.9.1 STATUS_REG0 REGISTER

Bits	Name	Description
0	fault_in	
1	fault_b_in	
2	unlock_i	
3	uart_en	
4	pll_lock	
5	vcc_uv	
6	vcc_ov	
7	vc5_uv	
8	vc5_ov	
9	vdd_uv	
10	vdd_ov	
11	v1v5ind_uv	
12	v1v5ind_ov	
13	v1v5ina_uv	
14	v1v5ina_ov	
15	v1v5va_uv	

12.9.2 STATUS_REG1 REGISTER

Bits	Name	Description
0	v1v5va_ov	
1	v5vin_uv	
2	v5vin_ov	
3	v5v_uv	
4	v5v_ov	
5	v5ve_uv	
6	v5ve_ov	
7	vbk_uv	
8	vbk_ov	
9	vfb_uv	
10	vfb_ov	
11	v1v5vosc_ov	
12	reset_i	
13 - 15	-	Unimplemented bits

12.9.3 STATUS_REG2 REGISTER

Bits	Name	Description
0	hep1	
1	hep2	
2	hep3	
3	ps1_src_ot	
4	ps2_src_ot	
5	ps3_src_ot	
6	drv1p_ot	
7	drv1n_ot	
8	drv2p_ot	
9	9drv2n_ot	
10	drv1p_ovc	
11	drv1n_ovc	
12	drv2p_ovc	
13	drv2n_ovc	
14 - 15	-	Unimplemented bits

12.9.4 STATUS_REG3 REGISTER

Bits	Name	Description
0	lvdt1_p_flt	
1	lvdt1_n_flt	
2	lvdt2_p_flt	
3	lvdt2_n_flt	
4	lvdt3_p_flt	
5	lvdt3_n_flt	
6	lvdt4_p_flt	
7	lvdt4_n_flt	
8	isens1_range_flt	
9	isens2_range_flt	
10	isens3_range_flt	
11	isens4_range_flt	
12	isens5_range_flt	
13	isens_rtn_range_flt	
14 - 15	-	Unimplemented bits

12.9.5 STATUS_REG4 REGISTER

Bits	Name	Description
0	drvsns1p_flt	
1	drvsns1n_flt	
2	drvsns2p_flt	
3	drvsns2n_flt	
4	hv1_flt	
5	hv2_flt	
6	temp1_flt	
7	temp2_flt	
8	temp3_flt	
9	temp4_flt	
10	temp5_flt	
11	v5v_v5ve_ot	
12	v1v5vd_ot	
13	v1v5va_ot	
14	buck_ot	
15	-	Unimplemented bit

12.9.6 STATUS _REG5 REGISTER

Bits	Name	Description
0	v5ve_open	
1 - 7	b'000 0000'	
8	v1v5va_i_ov	
9	v1v5va_i_uv	
10	v5v_i_ov	
11	v5v_i_uv	
12 - 15	b'0000'	

12.10 Trim Registers

Address	Name	R/W	Register Contents															
			D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0x600	TRIM_REG0	R/W	-	-	-	trim_v1v5vd			trim_v1v5va					trim_v5v				
0x601	TRIM_REG1	R/W	-	trim_vref						trim_vref_tc				trim_vbg_red				
0x602	TRIM_REG2	R/W	-	-	-	trim_vrefh				trim_vrefhl					trim_vtoi			
0x603	TRIM_REG3	R/W	-	-	trim_refpn_lvdt34					trim_refpn_lvdt12					trim_wd			
0x604	TRIM_REG4	R/W	trim_reserve															
0x605	TRIM_REG5	R/W	-	trim_temp3_src					trim_temp2_src					trim_temp1_src				
0x606	TRIM_REG6	R/W	-	trim_refpn_isens12					trim_temp5_src					trim_temp4_src				
0x607	TRIM_REG7	R/W	-	trim_v5ve					trim_refpn_isens5					trim_refpn_isens34				
0x608	TRIM_REG8	R/W	com_cfg0 (uart baud rate tuning)							com_cfg0 (spi/uart timeout)								

Note 1: Registers TRIM_REG0 to TRIM_REG3 can only be written when the UNLOCK input is high

12.11 OTP Registers

Address	Name	R/W	Register Contents															
			D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0x600	OTP_REG0	R/W	-	-	-	-	-	-	-	-	otp_addr							
0x601	OTP_REG1	R/W	-	-	-	-	-	-	-	-	-	-	-	-	-	otp_program		
0x602	OTP_REG2	R/W	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
0x603	OTP_REG3	R	-	-	-	-	-	-	-	otp_read_data								
0x604	OTP_REG4	R	-	-	-	otp_state												
0x605	OTP_REG5	R/W	-	-	-	-	-	-	-	-	-	-	-	-	-	-	otp_config	
0x606	OTP_REG6	W	otp_shadow_load															
0x607	OTP_REG7	R/W	-	-	-	-	-	-	-	otp_write_duration								

12.11.1 OTP_REG0 Register

Bits	Name	Safe Value	Description
0 - 6	otp_addr[6:0]	0x00	target address for otp read and write. These are bits 9:3 of the otp. In secded mode (below), lsb is a don't care
7 - 15	-	-	Unimplemented bits

12.11.2 OTP_REG1 Register

Bits	Name	Safe Value	Description
0 - 2	otp_program[2:0]	0x0	target bit for otp program. Write to this address after choosing the address in OTP_REG0. A write to this location will initiite a programming event if unlock is high
3 - 15	-	-	Unimplemented bits

12.11.3 OTP_REG3 Register

Bits	Name	Description
0 - 8	otp_read_data[8:0]	8 lsb are the 8 bit read, msb is a valid bit. Only valid when read completes (~6 cycles after write to OTP_REG0). Invalidated once another otp command occurs (read/program/shadow_load)
9 - 15	-	Unimplemented bits

12.11.4 OTP_REG4 REGISTER

Bits	Name	Description
0 - 2	otp_state[2:0]	otp state
3 - 7	otp_state[7:3]	command processor state
8 - 11	otp_state[11:8]	secded state
12	otp_state[12]	unlock bit
13 - 15	-	Unimplemented bits

12.11.5 OTP_REG5 REGISTER

Bits	Name	Safe Value	Description
0	otp_config[0]	0	bit 0 controls "raw (uncorrected)" or secded read access. When 0 (or in shadow load mode), lsb of otp addr is ignored and two bytes are read. The two bytes go into a 16-bit secded decoder and the 8 lsb of the secded output are read into reg 3. If a fault occurs, if correctable, otp_correctable_fault fires. If uncorrectable, otp_uncorrectable_fault fires. secded read: read OTP ADDR bbbbbb1 and bbbbbb0, where bbbbbbX is written into OTP_REG0, treat the 16 bits as input to secded decoder, returns 11 bits, use 8 lsbs, drop 3 msbs When 1, then lsb of address is used, 8 bits from that otp location are transferred to reg 3. raw read: read OTP ADDR bbbbbbb where bbbbbbb is written into OTP_REG0, the 8 bits from that otp location go into OTP_REG3
1	otp_config[1]	0	Disables power to the otp memory. In that scenario, no reads or writes will occur. Any operation to the otp with this bit low is a fault
2 - 15	-	-	Unimplemented bits

12.11.6 OTP_REG6 REGISTER

Bits	Name	Safe Value	Description
0 - 15	otp_shadow_load	-	A write to this location of 0x524C will initiate a full refresh of all shadowed registers with the otp values (see otp_mem_map)

12.11.7 OTP_REG7 REGISTER

Bits	Name	Safe Value	Description
0 - 8	otp_write_duration[8:0]	0xC0	Number of system clocks for write pulse (set to ~8us/clock period). Default meets the 6us to 10us spec limit for 20-30Mhz system clock, but you can tune this for better margin to spec
9 - 15	-	-	Unimplemented bits

12.12 SAR Registers

Address	Name	R/W	Register Contents															
			D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0x801	SAR_REG1	R/W			sar_config													
0x802	SAR_REG2	R/W									pwm_oe							
0x803	SAR_REG3	R/W														clkdiv		
0x804	SAR_REG4	R/W	sns1															
0x805	SAR_REG5	R/W	sns2															
0x806	SAR_REG6	R/W									pwm_centered							
0x807	SAR_REG7	R/W									pwm_hi							
0x808	SAR_REG8	R					status1											
0x809	SAR_REG9	R							status2									
0x80A	SAR_REGA	R/W																
0x80B	SAR_REGB	R/W																
0x810	SAR_REG10	R/W	pwmX delay															
...	to																	
0x817	SAR_REG17	R/W																
0x818	SAR_REG18	R/W	pwmX duty															
...	to																	
0x81F	SAR_REG1F	R/W																
0x820	SAR_REG20	R/W	sar1_targets															
...	to																	
0x837	SAR_REG37	R/W																
0x840	SAR_REG40	R/W	sar2_targets															
...	to																	
0x857	SAR_REG57	R/W																
0x860	SAR_REG60	R	sar1_results alternating with sar2_results															
...	to																	
0x89F	SAR_REG89F	R																

12.13 GPIO Registers

The 9 GPIOs on pins 93 to 101 may be used as logic inputs, static logic outputs, or as logic outputs for various internal signals. To use a GPIO as a logic input, clear the appropriate bit in GPIO_REG3 and optionally enable the internal pulldown resistor by clearing the appropriate bit in GPIO_REG4. GPIO inputs are read from GPIO_REG5.

To use a GPIO as a logic output, first select the desired output signal from the table in section 0 on page 52, which provides a 5 bit selection number from 0 to 31. Update the 5 bits in the appropriate one of GPIO_REG0 to GPIO_REG2 to make the selection for that GPIO. Then set the appropriate bit in GPIO_REG4 to enable the GPIO as an output.

Address	Name	R/W	Register Contents															
			D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0xA00	GPIO_REG0	R/W	-	gpio_mux_ctrl123														
0xA01	GPIO_REG1	R/W	-	gpio_mux_ctrl456														
0xA02	GPIO_REG2	R/W	-	gpio_mux_ctrl789														
0xA03	GPIO_REG3	R/W	-	-	-	-	-	-	-	gpio_oe								
0xA04	GPIO_REG4	R/W	-	-	-	-	-	-	-	gpio_pulldown								
0xA05	GPIO_REG5	R/W	-	-	-	-	-	-	-	gpio_i								
0xA06	GPIO_REG6	R/W	-	-	-	-	-	-	-	gpio_o								

12.13.1 GPIO_REG0 REGISTER

Bits	Name	Safe Value	Description
0 - 4	gpio_mux_ctrl1	0x00	Selects one of 32 possible outputs on GPIO1 when output is enabled
5 - 9	gpio_mux_ctrl2	0x00	Selects one of 32 possible outputs on GPIO2 when output is enabled
10 - 14	gpio_mux_ctrl3	0x00	Selects one of 32 possible outputs on GPIO3 when output is enabled
15	-	-	Unimplemented bits

12.13.2 GPIO_REG1 REGISTER

Bits	Name	Safe Value	Description
0 - 4	gpio_mux_ctrl4	0x00	Selects one of 32 possible outputs on GPIO4 when output is enabled
5 - 9	gpio_mux_ctrl5	0x00	Selects one of 32 possible outputs on GPIO5 when output is enabled
10 - 14	gpio_mux_ctrl6	0x00	Selects one of 32 possible outputs on GPIO6 when output is enabled
15	-	-	Unimplemented bits

12.13.3 GPIO_REG2 REGISTER

Bits	Name	Safe Value	Description
0 - 4	gpio_mux_ctrl7	0x00	Selects one of 32 possible outputs on GPIO7 when output is enabled
5 - 9	gpio_mux_ctrl8	0x00	Selects one of 32 possible outputs on GPIO8 when output is enabled
10 - 14	gpio_mux_ctrl9	0x00	Selects one of 32 possible outputs on GPIO9 when output is enabled
15	-	-	Unimplemented bits

12.13.4 GPIO_REG3 REGISTER

All output enables are disabled in safe mode, making all GPIO ports inputs, but GPIO_REG3 values are not changed.

Bits	Name	Safe Value	Description
0	gpio_oe1	0	Set to 1 to enable GPIO1 output enable (GPIO1 is output port)
1	gpio_oe2	0	Set to 1 to enable GPIO2 output enable (GPIO2 is output port)
2	gpio_oe3	0	Set to 1 to enable GPIO3 output enable (GPIO3 is output port)
3	gpio_oe4	0	Set to 1 to enable GPIO4 output enable (GPIO4 is output port)
4	gpio_oe5	0	Set to 1 to enable GPIO5 output enable (GPIO5 is output port)
5	gpio_oe6	0	Set to 1 to enable GPIO6 output enable (GPIO6 is output port)
6	gpio_oe7	0	Set to 1 to enable GPIO7 output enable (GPIO7 is output port)
7	gpio_oe8	0	Set to 1 to enable GPIO8 output enable (GPIO8 is output port)
8	gpio_oe9	0	Set to 1 to enable GPIO9 output enable (GPIO9 is output port)
9 - 15	-	-	Unimplemented bits

12.13.5 GPIO_REG4 REGISTER

All pulldown resistors are enabled in safe mode, but GPIO_REG4 values are not changed.

Bits	Name	Safe Value	Description
0	gpio_pulldown1	0	Clear to 0 to enable GPIO1 pulldown resistor
1	gpio_pulldown2	0	Clear to 0 to enable GPIO2 pulldown resistor
2	gpio_pulldown3	0	Clear to 0 to enable GPIO3 pulldown resistor
3	gpio_pulldown4	0	Clear to 0 to enable GPIO4 pulldown resistor
4	gpio_pulldown5	0	Clear to 0 to enable GPIO5 pulldown resistor
5	gpio_pulldown6	0	Clear to 0 to enable GPIO6 pulldown resistor
6	gpio_pulldown7	0	Clear to 0 to enable GPIO7 pulldown resistor
7	gpio_pulldown8	0	Clear to 0 to enable GPIO8 pulldown resistor
8	gpio_pulldown9	0	Clear to 0 to enable GPIO9 pulldown resistor
9 - 15	-	-	Unimplemented bits

12.13.6 GPIO_REG5 REGISTER

Bits	Name	Description
0	gpio_i1	Read logic input level at GPIO1 pin
1	gpio_i2	Read logic input level at GPIO2 pin
2	gpio_i3	Read logic input level at GPIO3 pin
3	gpio_i4	Read logic input level at GPIO4 pin
4	gpio_i5	Read logic input level at GPIO5 pin
5	gpio_i6	Read logic input level at GPIO6 pin
6	gpio_i7	Read logic input level at GPIO7 pin
7	gpio_i8	Read logic input level at GPIO8 pin
8	gpio_i9	Read logic input level at GPIO9 pin
9 - 15	-	Unimplemented bits

12.13.7 GPIO_REG6 REGISTER

Bits	Name	Description
0	gpio_o1	Read programmed output logic level at GPIO1 pin
1	gpio_o2	Read programmed output logic level at GPIO2 pin
2	gpio_o3	Read programmed output logic level at GPIO3 pin
3	gpio_o4	Read programmed output logic level at GPIO4 pin
4	gpio_o5	Read programmed output logic level at GPIO5 pin
5	gpio_o6	Read programmed output logic level at GPIO6 pin
6	gpio_o7	Read programmed output logic level at GPIO7 pin
7	gpio_o8	Read programmed output logic level at GPIO8 pin
8	gpio_o9	Read programmed output logic level at GPIO9 pin
9 - 15	-	Unimplemented bits

12.13.8 GPIO PORT AND TEST PINS FUNCTION SELECTION

Sel	GPIO1	GPIO2	GPIO3	GPIO4	GPIO5	GPIO6
0	v1v5vd_uv1	v1v5vd_uv2	v1v5vd_uv3	!force_safe	clk_wd	rst
1	(clk20 && unlock_i)	(clk80 && unlock_i)	(clk_pll & unlock_i)	(|jtag_modes)	adc_isens1	adc_isens2
2	adc_lvdt1	adc_lvdt2	adc_lvdt3	adc_lvdt4	bridges_icl_disable	buck_ot
3	ch1_fault_dbe	ch1_fault_header	ch1_fault_sbc	ch1_reinit_dv	ch2_di_qual	ch2_dovalid
4	ch2_fault_sbc	ch2_rd_defer	ch2_reinit_dv	ch2_wr_defer	clk_isenses_adc	clk_lvdt12_adc
5	clk_sar	clk_sspi1	clk_sspi2	die_temp_sns_en	drv1_sense_en	drv1n_ot
6	drv2_sense_en	drv2n_ot	drv2n_ovc	drv2p_ot	drv2p_ovc	drvsns1n_flt
7	fsource_en	hep1	hep2	hep3	hv1_flt	hv2_flt
8	isens1_mod_tsten	isens1_range_flt	isens2_en	isens2_in_puen	isens2_mod_tsten	isens2_range_flt
9	isens3_range_flt	isens4_en	isens4_in_puen	isens4_mod_tsten	isens4_range_flt	isens5_en
10	isens_de	isens_rtn_range_flt	isens_sinc_de	isense_mods_bisten	lvdt12_de	lvdt12_en
11	lvdt1_cm_sense_en	lvdt1_n_flt	lvdt1_p_flt	lvdt1_toggle	lvdt2_cm_sense_en	lvdt2_n_flt
12	lvdt34_en	lvdt34_latency_warn	lvdt34_osr_de	lvdt34_sinc_de	lvdt3_cm_sense_en	lvdt3_n_flt
13	lvdt4_p_flt	0	otp_5v_en	0	0	otp_addr[2]
14	otp_dout[1]	otp_dout[2]	otp_dout[3]	otp_dout[4]	otp_dout[5]	otp_dout[6]
15	0	pll_lock	0	ps1_afe_en	ps1_src_en	ps1_src_ot
16	ps2_src_ot	ps2_src_sns_en	ps3_afe_en	ps3_src_en	ps3_src_ot	ps3_src_sns_en
17	reset_i	sar1_en	sar1_eoc	sar1_inmux[0]	sar1_inmux[1]	sar1_inmux[2]
18	sar2_eoc	sar2_inmux[0]	sar2_inmux[1]	sar2_inmux[2]	sar2_inmux[3]	sar2_vrefl_sel
19	spi1_miso_o	spi1_mosi_i	spi1_ss_n_i	spi2_miso_o	spi2_mosi_i	spi2_ss_n_i
20	temp1_pt_sel	temp1_pt_sns_en	temp1_ref_sns_en	temp1_src_en	temp2_afe_en	temp2_flt
21	temp2_ref_sns_en	temp2_src_en	temp3_afe_en	temp3_flt	temp3_infloat_det_en	temp3_pt_sel
22	temp4_afe_en	temp4_flt	temp4_infloat_det_en	temp4_pt_sel	temp4_pt_sns_en	temp4_ref_sns_en
23	temp5_infloat_det_en	temp5_pt_sel	temp5_pt_sns_en	temp5_ref_sns_en	temp5_src_en	u1_fault_dbe
24	u1_fault_sbc	u1_fault_st	u1_sample_de	u1_warn_baud	u2_fault_dbe	u2_fault_parity
25	u2_fault_st	u2_rd_defer	u2_sample_de	u2_warn_baud	u2_wr_defer	uart_en
26	v1v5ina_uv	v1v5ind_ov	v1v5ind_uv	v1v5va_ot	v1v5va_ov	v1v5va_uv
27	v5v_uv	v5v_v5ve_ot	v5ve_ov	v5ve_uv	v5vin_ov	v5vin_uv
28	vc5_ov	vc5_uv	vcc_ov	vcc_sense_en	vcc_uv	vdd_ov
29	wd_counter[0]	wd_counter[1]	wd_restart	xbar_read	xbar_write	0
30	lvdt1_toggle	lvdt2_toggle	pwm_sync	sar1_eoc	sar_start	clk_wd
31	1	1	1	1	1	1

Sel	GPIO7	GPIO8	GPIO9	TEST1	TEST2
0	fatal_fault	por_n	!bist_done	v1v5va_uv	(unlock_i & clk_pll)
1	adc_isens3	adc_isens4	adc_isens5	isens1_mod_tsten	wd_counter[2]
2	ch1_di_qual	ch1_dovalid	ch1_fault_arbst	isens2_mod_tsten	wd_counter[3]
3	ch2_fault_arbst	ch2_fault_dbe	ch2_fault_header	isens3_mod_tsten	wd_counter[4]
4	clk_lvdt34_adc	clk_osc	clk_pll	isens4_mod_tsten	wd_counter[5]
5	drv1n_ovc	drv1p_ot	drv1p_ovc	isens5_mod_tsten	wd_counter[6]
6	drvsns1p_flt	drvsns2n_flt	drvsns2p_flt	clk_az_tstbus_disable_en	wd_counter[7]
7	hv_sense_en	isens1_en	isens1_in_puen	clk_az_tstbus_disable_en	wd_counter[8]
8	isens3_en	isens3_in_puen	isens3_mod_tsten	clk_az_isenses	wd_counter[9]
9	isens5_in_puen	isens5_mod_tsten	isens5_range_flt	clk_sar	wd_counter[10]
10	lvdt12_latency_warn	lvdt12_osr_de	lvdt12_sinc_de	clk_wd	v1v5vd_ov1
11	lvdt2_p_flt	lvdt2_toggle	lvdt34_de	clk_pll	v1v5vd_ov2
12	lvdt3_p_flt	lvdt4_cm_sense_en	lvdt4_n_flt	!force_safe	v1v5vd_ov3
13	otp_addr[3]	otp_cs	otp_dout[0]	lvdt34_osr_de	clk_az_sars
14	otp_dout[7]	otp_prchg	otp_progen	sar2_eoc	clk_az
15	ps1_src_sns_en	ps2_afe_en	ps2_src_en	clk_isenses_adc	clk_sar
16	pwm_sync	reserve_status[0]	reserve_status[1]	reserve_status[8]	clk_wd
17	sar1_inmux[3]	sar1_vrefl_sel	sar2_en	reserve_status[9]	clk_osc
18	sar_start	scan_enable	scan_mode	reserve_status[10]	lvdt34_sinc_de
19	temp1_afe_en	temp1_flt	temp1_infloat_det_en	reserve_status[11]	reserve_status[2]
20	temp2_infloat_det_en	temp2_pt_sel	temp2_pt_sns_en	control_3[0]	control_3[3]
21	temp3_pt_sns_en	temp3_ref_sns_en	temp3_src_en	sar1_data[0]	sar2_data[0]
22	temp4_src_en	temp5_afe_en	temp5_flt	sar1_data[1]	sar2_data[1]
23	u1_fault_parity	u1_fault_rx	u1_fault_rxd	sar1_data[2]	sar2_data[2]
24	u2_fault_rx	u2_fault_rxd	u2_fault_sbc	sar1_data[3]	sar2_data[3]
25	uart_mode	unlock_i	v1v5ina_ov	sar1_data[4]	sar2_data[4]
26	v1v5vd_ot	v1v5vosc_ov	v5v_ov	sar1_data[5]	sar2_data[5]
27	vbg_sense_en	vbk_ov	vbk_uv	sar1_data[6]	sar2_data[6]
28	vdd_uv	vfb_ov	vfb_uv	sar1_data[7]	sar2_data[7]
29	0	0	0	sar1_data[8]	sar2_data[8]
30	hep1	hep2	hep3	sar1_data[9]	sar2_data[9]
31	1	1	1	reserved	reserved

12.14 LVDT Registers

The 0xBxx registers manage LVDT1, and the 0xCxx registers manage LVDT2.
The offset register provides the number of clocks that the DRV_P and DRV_N outputs are both low for commutation.
The frame counter register identifies which frame is currently being used for duty.
The duty ramp rate register sets rate at which the duty limit rises or falls after lvdt_oe changes (rate = $2 * 2^{\text{Duty ramp rate}}$).
The duty limit register reads 0 when lvdt_en=0, increments every frame by $2^{\text{Duty ramp rate}}$ when lvdt_oe is high, and decrements every frame by $2^{\text{Duty ramp rate}}$ when lvdt_oe is low.

Address	Name	R/W	Register Contents															
			D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0xB00	LVDT_REG0	R/W	-	-	-	-	-	-	Duty cycle (number of system clocks that sets the duty for one frame)									
to		R/W	-	-	-	-	-	-										
0xB7F	LVDT_REG7F	R/W	-	-	-	-	-	-										
0xB80	LVDT_REG80	R/W	-	-	-	-	-	-	-	PWM period (32 to 256 system clocks)								
0xB81	LVDT_REG81	R/W	-	-	-	-	-	-	-		Frame size (8 to 128 duty clock counts)							
0xB82	LVDT_REG82	R/W	-	-	-	-	-	-	-						Offset			
0xB83	LVDT_REG83	R	-	-	-	-	-	-	-			Frame counter						
0xB84	LVDT_REG84	R/W	-	-	-	-	-	-	-						Duty ramp rate			
0xB85	LVDT_REG85	R	-	-	-	-	-	Duty limit (0 to {PWM period} x 4)										

Address	Name	R/W	Register Contents															
			D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0xC00	LVDT_REG0	R/W	-	-	-	-	-	-	Duty cycle (number of system clocks that sets the duty for one frame)									
to		R/W	-	-	-	-	-	-										
0xC7F	LVDT_REG7F	R/W	-	-	-	-	-	-										
0xC80	LVDT_REG80	R/W	-	-	-	-	-	-	-	PWM period (32 to 256 system clocks)								
0xC81	LVDT_REG81	R/W	-	-	-	-	-	-	-		Frame size (8 to 128 duty clock counts)							
0xC82	LVDT_REG82	R/W	-	-	-	-	-	-	-						Offset			
0xC83	LVDT_REG83	R	-	-	-	-	-	-	-			Frame counter						
0xC84	LVDT_REG84	R/W	-	-	-	-	-	-	-						Duty ramp rate			
0xC85	LVDT_REG85	R	-	-	-	-	-	Duty limit (0 to {PWM period} x 4)										

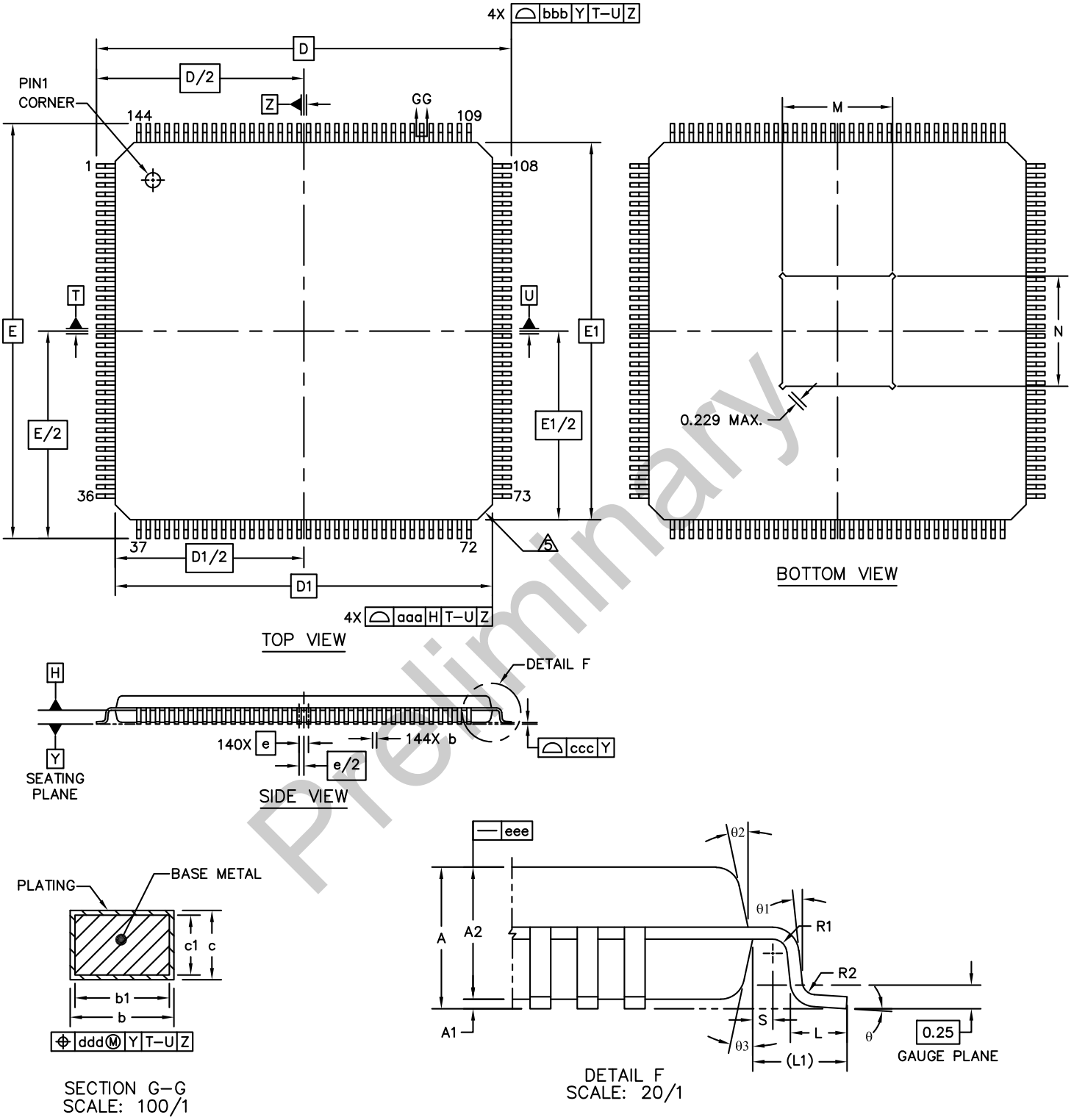
12.15 UART Registers

The 0xD00 and 0xD01 registers manage UART channel 1, and the 0xD02 and 0xD03 registers manage UART channel 2.

The two counters u1_warn_baud_cntr and u2_warn_baud_cntr log up to 255 events of the respective UART bit sampling timing being out of spec, allowing timing shifts in the serial interafce to be monitored.

Address	Name	R/W	Register Contents															
			D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0xD00	UART_U1_WARN	R	-	-	-	-	-	-			u1_warn_baud_cntr							
0xD01	UART_U1_WARN_RST	W	Writing any value to this register resets the u1_warn_baud_cntr counter															
0xD02	UART_U2_WARN	R	-	-	-	-	-	-	-		u2_warn_baud_cntr							
0xD03	UART_U2_WARN_RST	W	Writing any value to this register resets the u2_warn_baud_cntr counter															

13 LQFP-144 Dimensions



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.17	0.22	0.27
LEAD WIDTH		b1	0.17	0.2	0.23
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
	X	D	22 BSC		
	Y	E	22 BSC		
BODY SIZE	X	D1	20 BSC		
	Y	E1	20 BSC		
LEAD PITCH		e	0.5 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
EP SIZE	X	M	5.742	5.842	5.942
	Y	N	5.742	5.842	5.942
PACKAGE EDGE TOLERANCE		aaa	0.1		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.08		
MOLD FLATNESS		eee	0.05		

Figure 3. 144-Lead LQFP Package Dimensions

Note:
1. Controlling dimensions are in mm. Imperial (inch) equivalents are shown for general information
2. Datum T, U, and Z to be determined at datum plane H.
3. Dimensions D and E to be determined at seating plane datum Y.
4. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 per side. Dimensions D1 and E1 do include mold mismatch and are determined at datum plane datum H.
5. Dimension b does not include dam bar protrusion. Allowable dam bar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08 mm. Dam bar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm.

14 Revision History

14.1 Revision 0.2 - June 2021

Pre-release. Changes not logged.

14.2 Revision 1 - xxx 2021

First release.

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