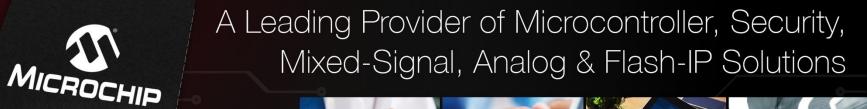


THINNING



Getting Started with the RISC-V Based PolarFire® SoC FPGA Webinar Series Session 11: Handling Binaries Hugh Breslin, Design Engineer

Hugh Breslin, Design Engineer Thursday Mar. 12, 2020



Second Thursdays

- Mar. 12 Webinar 11: Handling Binaries
- April 9 Webinar 12: Two Bare-Metal Applications on PolarFire[®] SoC
- May 14 Webinar 13: Linux[®] on Renode
- June 11 Webinar 14: Building Applications for Linux on PolarFire SoC
- July 9 Webinar 15: Real-Time (AMP Mode) on PolarFire SoC



Supporting Content

www.microsemi.com/Mi-V "Renode Webinar Series"

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Learn how to get started with the PolarFire SoC FPGA, the world's first RISC-V based SoC FPGA, to create fully deterministic, real-time systems alongside the Linux® operating system. We are holding a series of webinars to introduce you to the free Renode™ development platform from Mi-V partner Antmicro that is available with our SoftConsole v6.0 software development environment. You will see demo applications, learn how to create projects, and find out how to set up and configure your own systems targeting the new SoC FPGA architecture.

Click here to register



Webinar 1 (May 2): Discover Renode for PolarFire[™] SoC Design and Debug

In this introductory session, we will provide you with an overview of SoftConsole 6.0 with RenodeTM integration. We will introduce you to the Renode development framework and provide an overview of the platform and its features. You will also learn about the PolarFire™ SoC architecture and how to use Renode to develop your application.

Webinar 1: Discover Renode for PolarFire[®] SoC Design and Debug Webinar 2: How to Get Started with Renode for PolarFire SoC Webinar 3: Learn to Debug a Bare-Metal PolarFire SoC Application with Renode Webinar 4: Tips and Tricks for Even Easier PolarFire SoC Debug with Renode Webinar 5: Add and Debug PolarFire SoC Models with Renode Webinar 6: Add and Debug Pre-Existing Model in PolarFire SoC Webinar 7: How to Write Custom Models Webinar 8: What's New in SoftConsole v6.2

Webinar 9: Getting Started with PolarFire SoC

Webinar 10: Introduction to the PolarFire SoC Bare-Metal Library





- The PolarFire[®] SoC Start Up Sequence
- Setting Breakpoints on Specific Harts
- Demo PolarFire [®] SoC Start Up Sequence
- MPFS_HAL_FIRST_HART
- MPFS_HAL_LAST_HART



The PolarFire[®] SoC Start Up Sequence

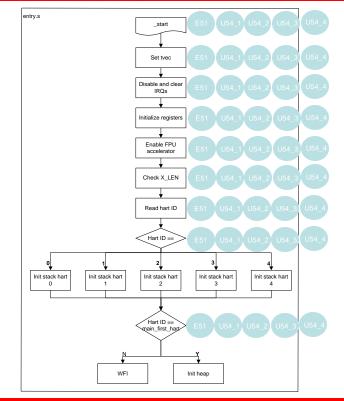


The PolarFire[®] SoC Start Up Sequence

- 1. Harts start from the same "_start" function
- 2. They diverge after initializing their stacks
 - By default the U54 harts go to WFI
 - E51 initializes the heap and wakes up harts in use
- 3. Harts jump to dedicated main functions

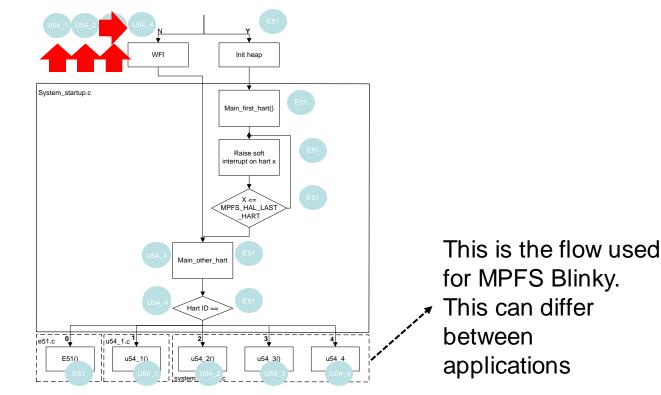


The PolarFire[®] SoC Start Up Sequence





The PolarFire[®] SoC Start Up Sequence





Setting Breakpoints on Specific Harts



Setting Breakpoints on Specific Harts

 Breakpoints can be set for all threads by double clicking on the line the breakpoint is needed

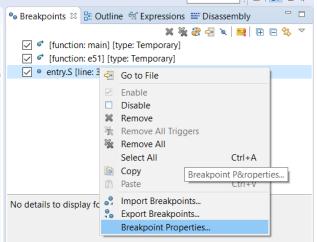
s entry.	s 🛛			🍨 Breakpoints 🛱 📴 Outline 🏘 Expressions 📟 Disassembly 👘 🗖
32 33 34 5 36 37	csrw mtvec, a4 /* Make sure that mtv 1: csrr a5, mtvec bne a4, a5, 1b	<pre># initalise machine trap vector address ec is updated */</pre>	^	 X X 200 -

• They can also be filtered so that only specific harts halt at the breakpoint



- <u>While</u> debugging right click on the breakpoint
- Select "Breakpoint Properties..."

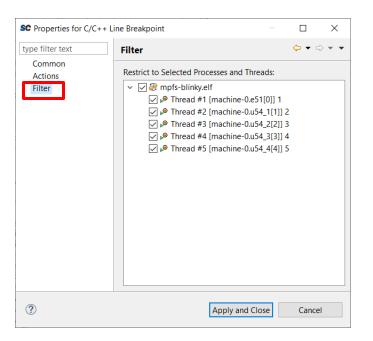
 Note: breakpoint properties will reset between debug sessions



Setting Breakpoints on Specific Harts

• Open the "Filter" heading

 All threads are selected by default, deselect the threads (harts) you don't want to halt on the breakpoint





Demo PolarFire[®] SoC Start Up Sequence

File Edit Source Refactor Navigate Search Project Git Run Window Help

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S /mpfs-blinky/src/platform/mpfs_hal/entry.S

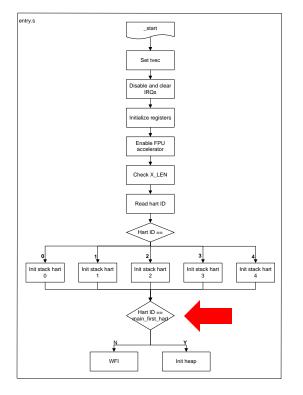




MPFS_HAL_FIRST_HART



MPFS_HAL_FIRST_HART



Here the harts will diverge and the main hart of the system will wake harts in use from WFI, the "MPFS_HAL_FIRST_HART" value can be changed to determine which hart is the main hart.



MPFS_HAL_FIRST_HART

🖻 🔄 🗠 🗖 b mss sw config.h ⊠ Project Explorer 🕴 fpga-cortex-m1-blinky 26 @section m1fpga-cortex-m1-blinky 27 miv-rv32im-interrupt-blinky 28 *//*==== 29 miv-rv32im-systick-blinky miv-rv32imaf-mandelbrot-uart miv-rv32imaf-ravtracer-uart-cpp 32 ✓ ≌ mpfs-blinky 339/* > 🖑 Binaries 34 Includes 36 🗸 🐸 src 37 > > application 38 > > pmodules 39 ✓ ▷ platform 🗸 🗁 config bardware 42 */ > 🗁 linker ✓ ⇒ software 45 #endif Arivers 46 mpfs hal > h mss_sw_config.h > readme.txt 49 #endif > > > drivers 50 > 🗁 hal 51⊖/* 52 > >> profs hal 53 */ > > Debug mpfs-blinky hw-emulation all-harts Debug.launch

30 #ifndef USER CONFIG MSS USER CONFIG H 31 #define USER CONFIG MSS USER CONFIG H MPFS HAL FIRST HART and MPFS HAL LAST HART defines used to specify whi 35 * harts to actually start. * Set MPFS HAL FIRST HART to a value other than 0 if you do not want you * to start and execute code on the E51 hart. * Set MPFS HAL LAST HART to a value smaller than 4 if you do not wish to * all U54 harts. * Harts that are not started will remain in an infinite WFI loop unless through some other method 43 #ifndef MPFS HAL FIRST HART 44 #define MPFS HAL FIRST HART 0 47 #ifndef MPFS HAL LAST HART 48 #define MPFS HAL LAST HART 4 * Markers used to indicate startup status of hart 54 #define HLS DATA IN WFI 0x12345678U

The "MPFS_HAL_FIRST_HART" value is set to 0 by default to select the E51 as the main hart, this value can be changed to use a U54 hart as the main hart. File Edit Source Refactor Navigate Search Project Git Run Window Help

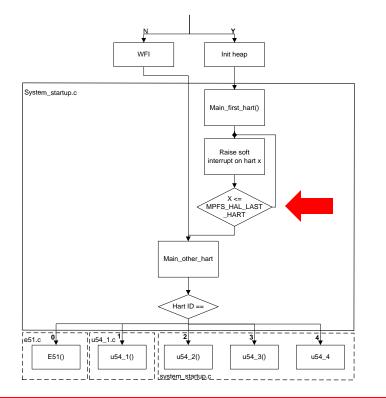
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MPFS_HAL_LAST_HART



MPFS_HAL_LAST_HART



The main hart will loop here turning on the harts being used in the system.

If harts aren't being used, the "MPFS_HAL_LAST_HART" value can be changed to leave unused harts in "wfi" mode.



MPFS HAL LAST HART

Project Explorer 🖾	⊑ 🔩 ▽ 🗆 🗆	ⓑ mss_sw_config.h ⊠	
 fpga-cortex-m1-blinky m1fpga-cortex-m1-blinky miv-rv32im-interrupt-blinky miv-rv32imaf-raytracer-uart-cpp miv-rv32imaf-raytracer-uart-cpp miv-rv32imaf-raytracer-uart-cpp mit-rv32imaf-raytracer-uart-cpp mit-rv32i		<pre>26 @section 27 28 *//*==================================</pre>	FIG_H_ HAL_LAST_HART defines used to specify whi value other than 0 if you do not want you
> 🗁 hal		51 [®] /*	
> 🗁 mpfs_hal		52 * Markers used to indicate start 53 */	lup status of nart
> 🖻 Debug		54 #define HLS DATA IN WFI	0x12345678U
📄 mpfs-blinky hw-emulation all-harts De	bug.launch		0/120-00/00

The "MPFS_HAL_LAST_HART" value is set to 4 by default as harts without a defined function will be put into WFI mode from the weakly linked function.

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- MPFS_HAL_LAST_HART



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Thank You Any Questions?