Total Ionizing Dose Test Report

No. 20T-RTAX4000D-CQ352-DG8GT1

April 2020

March 27, 2020

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I. Summary Table

The TID tolerance for each tested parameter is summarized below in Table 1. The overall tolerance is limited by the standby power-supply current (ICC). The room temperature annealing allowed by 1019.8 to anneal down ICC is performed for approximately 7 days. Every DUT passes the major specifications listed in the table for 300 krad (SiO2) of irradiation.

Table 1 Tolerances for Each Tested Parameter

Parameter	Tolerance
1. Gross Functionality	Passed 300 krad (SiO_2)
2. Power Supply Current (ICCA/ICCI)	Passed 300 krad (SiO_2)
3. Input Threshold (VIL/VIH)	Passed 300 krad (SiO_2)
4. Output Drive (VOL/VOH)	Passed 300 krad (SiO_2)
5. Propagation Delay	Passed 300 krad (SiO_2) for 10% degradation criterion
6. Transition Time	Passed 300 krad (SiO_2)

II. Total Ionizing Dose (TID) Testing

This testing is designed on the basis of an extensive database (see, for example, TID data of antifuse-based FPGAs at http://www.klabs.org and http://www.microsemi.com/soc) accumulated from the TID testing of many generations of antifuse-based FPGAs.

A. Device-Under-Test (DUT) and Irradiation Parameters

Table 2 lists the DUT and irradiation parameters. During irradiation all inputs are grounded except for the inputs Burnin, oe_EAQ, enable_HSB and the utilized clocks (Rclock1-3 and Hclock1-4). The inputs Burnin, oe_EAQ and enable_HSB are set high to 3.3 V and a 1 KHz clock is provided to all clocks in order for the design to remain stable during irradiation. During anneal each input and output is tied to ground or VCCI through a 4.7 kΩ resistor. Appendix A contains the schematics of irradiation-bias circuits.

Table 2 DUT and Irradiation Parameters

Part Number	**RTAX4000D**
Package	CQFP352
Foundry	United Microelectronics Corp.
Technology	0.15 µm CMOS
DUT Design	MASTER_RTAX4000S_DESIGN_80_SP1
Die Lot Number	DG8GT1
Quantity Tested	5
Serial Number	300 krad: 11754, 11755 200 krad: 11745 100 krad: 11728. 11736
Radiation Facility	Defense Microelectronics Activity
Radiation Source	Co-60
Dose Rate (±5%)	10 krad (SiO_2)/min
Irradiation Temperature	Room
Irradiation and Measurement Bias (VCCI/VCCA)	Static at 3.3 V / 1.5 V
I/O Configuration	Single ended: LVTTL Differential pair: LVPECL

B. Test Method

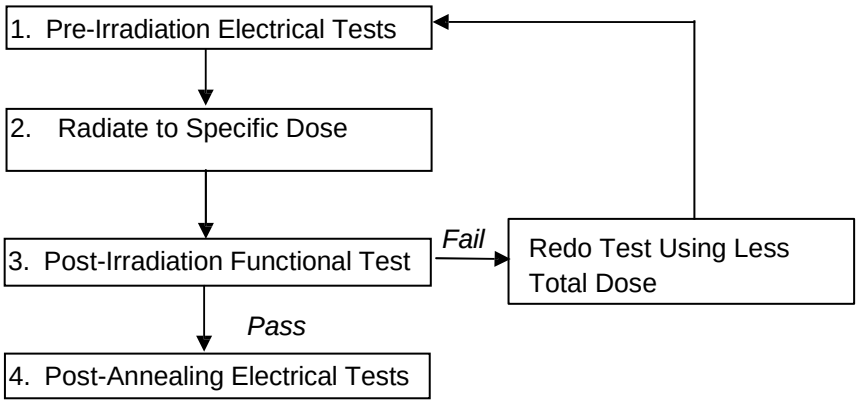

Figure 1 Parametric Test Flow Chart

The test method generally follows the guidelines in the military standard TM1019.8. Figure 1 is the flow chart showing the steps for parametric tests, irradiation, and post-irradiation annealing.

The accelerated aging, or rebound test mentioned in TM1019.8, is unnecessary because there is no adverse time-dependent effect (TDE) in Microsemi SoC Products Group products manufactured by sub-micron CMOS technology. Elevated temperature annealing actually reduces the effects originated from radiation-induced leakages. As indicated by testing data in the following sections, the predominant radiation effects in RTAX4000S are due to radiation-induced leakages.

Room temperature annealing is performed in this test; the duration is approximately 7 days.

C. Design and Parametric Measurements

The DUT uses a high utilization generic design (RTAX4000S_CQ352_MASTER) to evaluate total dose effects for typical space applications. The schematics of this design are documented in Appendix B.

The functionality is measured at 1 MHz and 50 MHz using the minimum and maximum power specifications shown in Table 3.

Table 3 Minimum and Maximum Power Specifications for RTAX-D Devices

Supply Voltage	Minimum	Recommended	Maximum
1.5 V Core	1.4 V	1.5 V	1.6 V
3.3 V I/O	3.0 V	3.3 V	3.6 V
3.3 V VCCDA I/O	3.0 V	3.3 V	3.6 V

The functionality test design is subdivided into two blocks, the EAQ (Enhanced Antifuse Qualification) and the QBI (Qualification Burn-In). The EAQ block includes three 1458-bit shift registers and tests the I/Os (1560 I/O registers and 520 I/Os) and RAM (1x16384 RAM). The QBI block tests all offered macros and I/O standards. The results from the functional tests are obtained from the following outputs: IO_Monitor_EAQ, RAM_Monitor_EAQ, Array_Monitor_EAQ, Global_Monitor_EAQ, C_test_mon_QBI, ALU_test_mon_QBI, Global_mon_QBI_TP, and Global_mon_QBI_BI. Details on the Functionality Test are shown in Appendix B.

ICC is measured on the power supply of the logic-array (ICCA) and I/O (ICCI) respectively. The input logic threshold (VIL/VIH) is tested on single-ended inputs Shiftin1, Shiftin2, Shiftin3, Shiftin4, Shiftin5, Shiftin7, Shiftin8, zoom_sel_n_1, zoom_sel_n_0, zoom, TOG_n, SEU_sel, Set_n, Resetn, oe_EAQ, enable_HSB, test_done_sel_2, IO_Pattern_Length_2, IO_Pattern_Length_1, IO_Pattern_Length_0, IO_Johnson, A_Johnson, A_Pattern_Length_1, and A_Pattern_Length_0. The output-drive voltage (VOL/VOH) is measured on single-ended outputs Array_out_EAQ_0, Array_out_EAQ_1, Array_out_EAQ_2, Global_Monitor_EAQ, Shiftout3, Shiftout7, Shiftout8, RAM_Monitor_EAQ, RAM_out_EAQ_0, RAM_out_EAQ_4, RAM_out_EAQ_8.

The propagation delays are measured on the outputs of five delay strings; each one comprises of 1,170 NAND4-inverters. There are 6 delay measurements: one measurement for each delay string and a total delay measurement obtained from cascading all the delay strings. The propagation delay is defined as the time delay from the triggering edge at the HClock1 input to the switching edge at the output. The delay measurements are taken for both rising and falling edges, the average reading of the two measurements is reported. The transition characteristics, measured on the output delay_out_SEU4, are shown as oscilloscope captures.

Table 4 lists measured electrical parameters and the corresponding logic design.

Table 4 Logic Design for Parametric Measurements

Parameters	Logic Design
1. Functionality	IO_Monitor_EAQ, RAM_Monitor_EAQ, Array_Monitor_EAQ, Global_Monitor_EAQ, C_test_mon_QBI, ALU_test_mon_QBI, Global_mon_QBI_TP, and Global_mon_QBI_BI
2. ICC (ICCA/ICCI)	DUT power supply
3. Input Threshold (VIL/VIH)	Single ended inputs (Shiftin1, Shiftin2, Shiftin3, Shiftin4, Shiftin5, Shiftin7, Shiftin8, zoom_sel_n_1, zoom_sel_n_0, zoom, TOG_n, SEU_sel, Set_n, Resetn, oe_EAQ, enable_HSB, test_done_sel_2, IO_Pattern_Length_2, IO_Pattern_Length_1, IO_Pattern_Length_0, IO_Johnson, A_Johnson, A_Pattern_Length_1, A_Pattern_Length_0)
4. Output Drive (VOL/VOH)	Single-ended outputs (Array_out_EAQ_0, Array_out_EAQ_1, Array_out_EAQ_2, Global_Monitor_EAQ, Shiftout3, Shiftout7, Shiftout8, RAM_Monitor_EAQ, RAM_out_EAQ_0, RAM_out_EAQ_4, RAM_out_EAQ_8)
5. Propagation Delay	String of NAND4-inverters. Measured from output delay_out_SEU4
6. Transition Characteristic	NAND4-inverter output (delay_out_SEU4)

III. Test Results

The test results mainly compare the electrical parameter measured pre-irradiation with the same parameter measured post-irradiation-and-annealing, or post-annealing.

A. Functionality

Every DUT passed the pre-irradiation and post-annealing functional tests.

B. Power Supply Current (ICCA and ICCI)

The logic-array power supply (VCCA) is 1.5 V, and the IO power supply (VCCI) is 3.3 V. Their standby currents, ICCA and ICCI, are monitored influx. Figure 2-6 show the influx ICCA and ICCI versus total dose for the DUTs.

Referring to TM1019.8 subsection 3.11.2.c, the post-irradiation-parametric limit (PIPL) for the post-annealing ICC, should be defined as the addition of highest ICCI, ICCDA, and ICCDIFFA values in Table 2-4 of the *RTAX-S/SL and RTAX-DSP Radiation-Tolerant FPGAs datasheet* posted on the Microsemi SoC Products Group website:

http://www.microsemi.com/soc/documents/RTAXS_DS.pdf

Therefore, the PIPL for ICCA is 600 mA, and the PIPL for ICCI is 60 mA.

Table 5 summarizes the pre-irradiation, post-irradiation right after irradiation and before anneal, and post-annealing ICCA and ICCI data.

Table 5 Pre-irradiation, Post Irradiation and Post-Annealing ICC

DUT	Total Dose	ICCA (mA)			ICCI (mA)		
		Pre-Irrad.	Post-Irrad.	Post-Ann.	Pre-Irrad.	Post-Irrad.	Post-Ann.
11728	100 krad	2.3	2.7	2.4	13.9	15	2.4
11736	100 krad	2.3	2.7	2.4	13.5	14.8	2.4
11745	200 krad	3.0	5.1	3.2	13.8	130	3.2
11754	300 krad	2.1	65	7.7	13.7	175	7.7
11755	300 krad	2.5	61.2	8.1	13.7	131	8.1

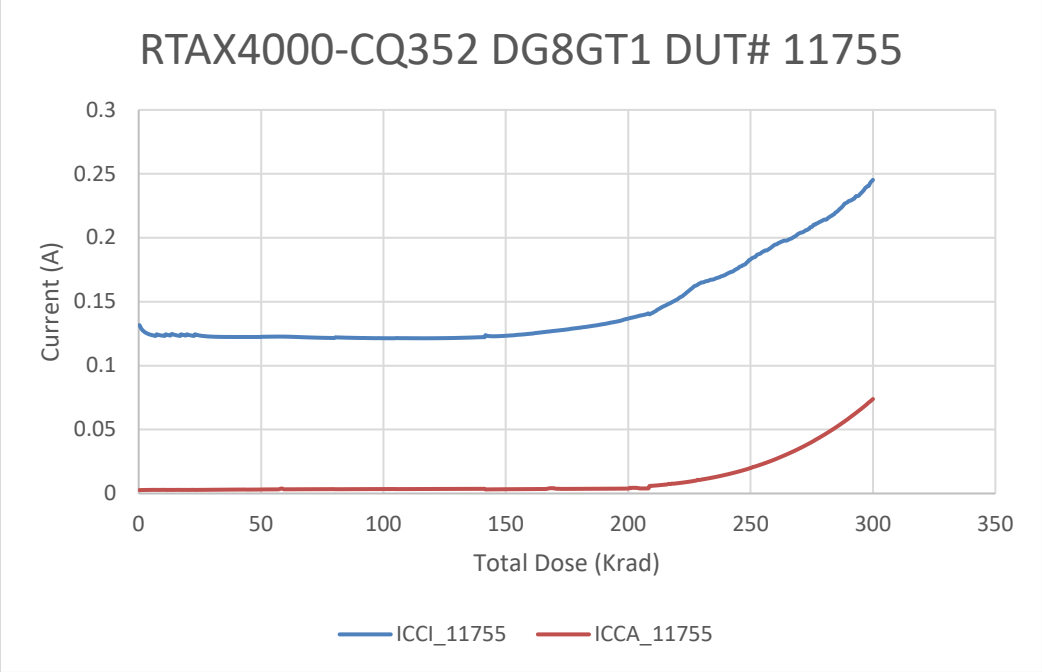

Figure 2 DUT 11754 Influx ICCI and ICCA

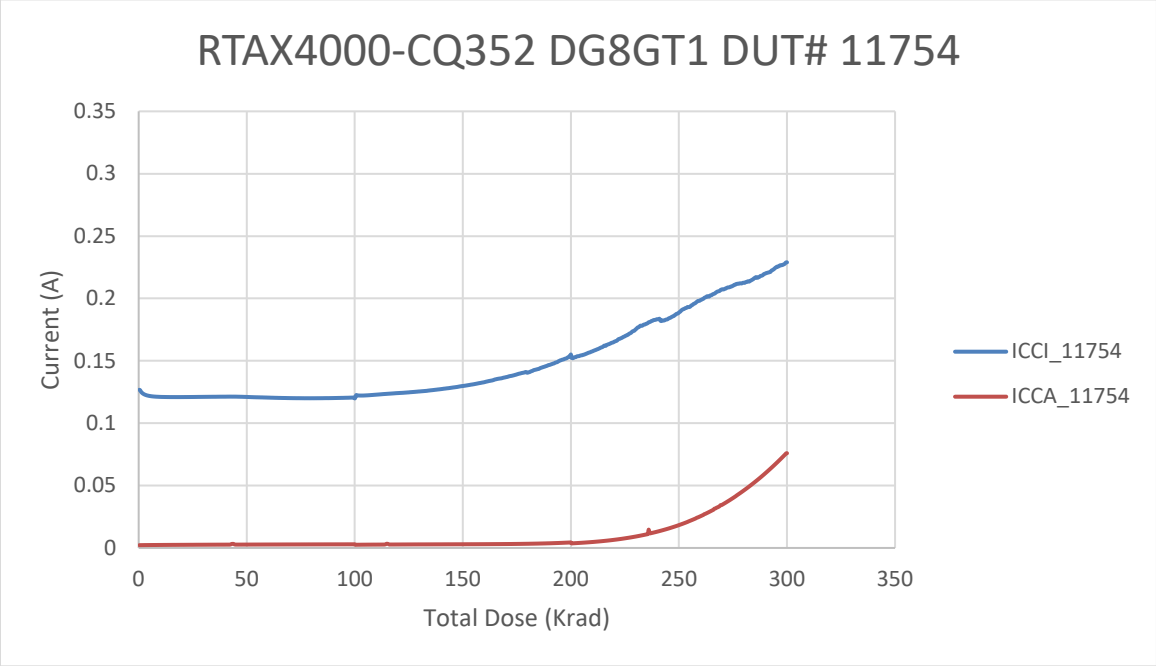

Figure 3 DUT 11755 Influx ICCI and ICCA

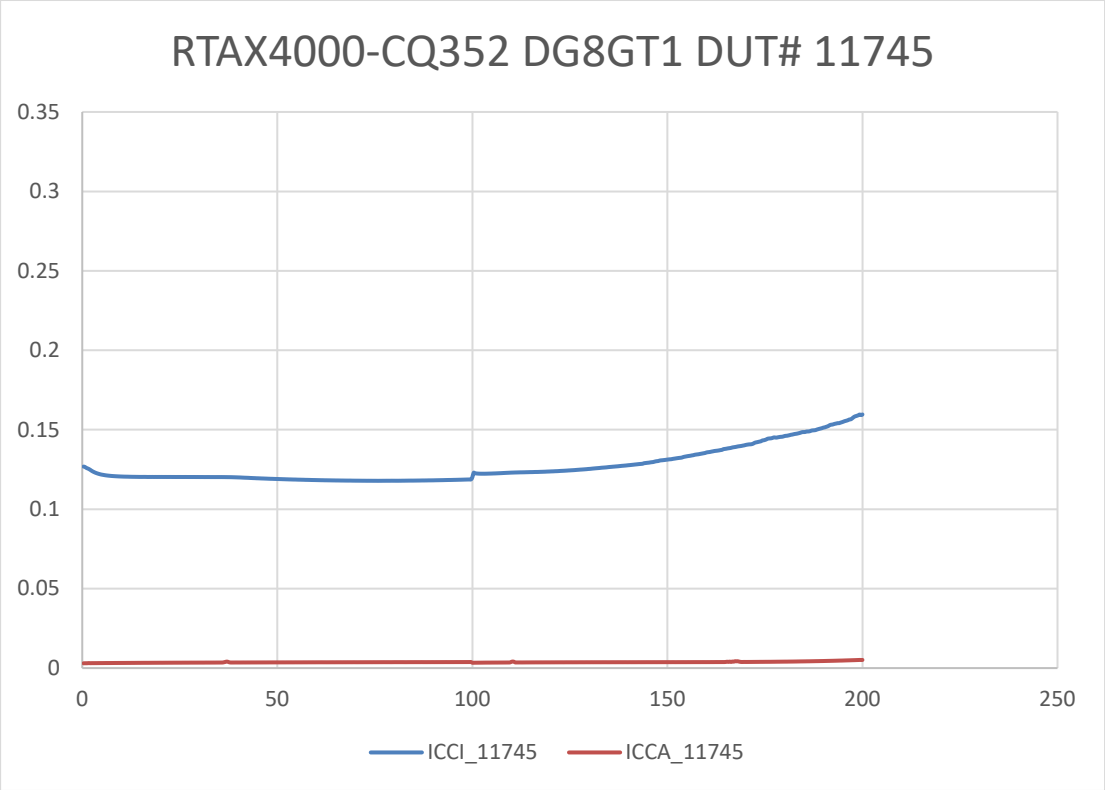

Figure 4 DUT 11745 Influx ICCI and ICCA

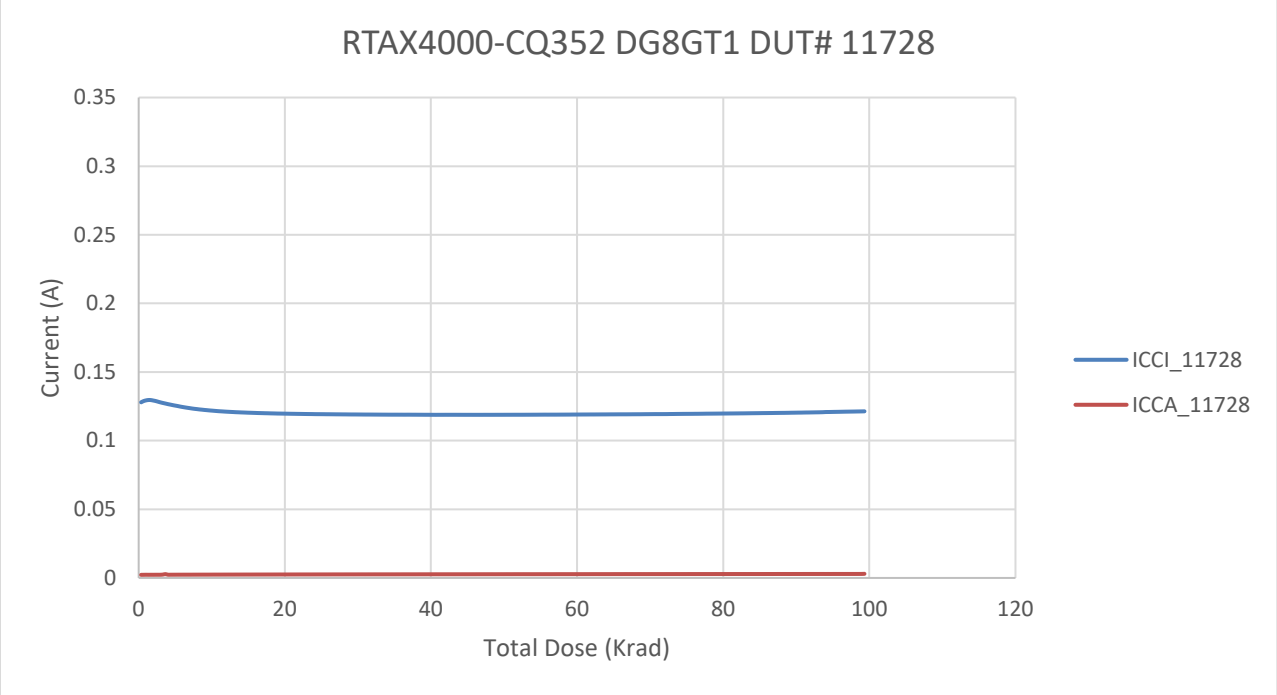

Figure 5 DUT 11728 Influx ICCI and ICCA

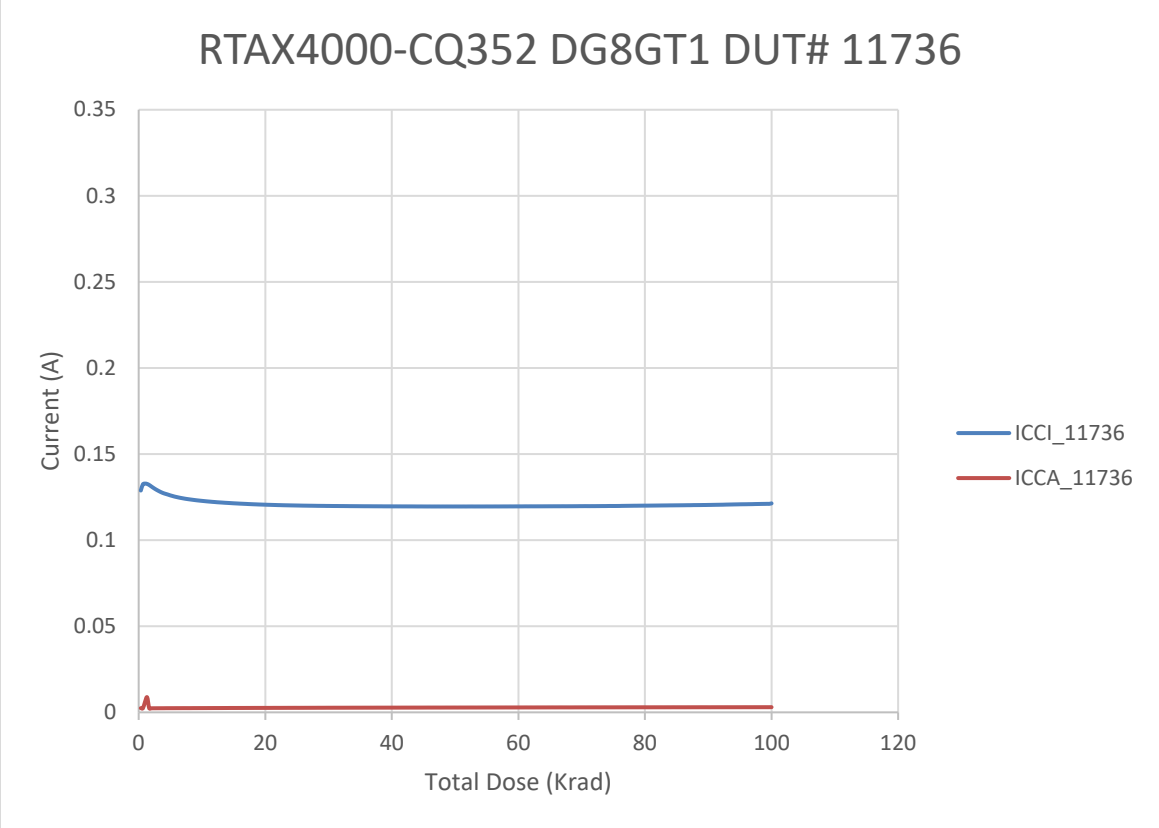

Figure 6 DUT 11736 Influx ICCI and ICCA

C. Single-Ended 3.3 V LVTTL Input Logic Threshold (VIL/VIH)

The input switching threshold, or trip point, is defined as the applied input voltage at which the output of the design, often just input and output buffers, starts to switch: VIH is the input trip point when the input is going high to low; VIL is the input trip point when the input is going low to high. They are listed in Tables 6 and 7. The difference between the pre-irradiation and post-annealing data is usually negligibly small.

Table 6 Pre-Irradiation and Post-Annealing Input Thresholds (VIL)

Pin \ DUT(Dose)	11754 (300 krad)		11755 (300 krad)		11745 (200 krad)		11728 (100 krad)		11736 (100 krad)	
	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an
SEU_sel	1.345	1.325	1.34	1.32	1.345	1.33	1.345	1.34	1.34	1.33
zoom_sel_n_0	1.345	1.33	1.345	1.33	1.35	1.34	1.35	1.345	1.345	1.34
zoom_sel_n_1	1.345	1.325	1.345	1.325	1.345	1.33	1.35	1.34	1.34	1.335
zoom	1.34	1.325	1.34	1.325	1.345	1.33	1.345	1.335	1.335	1.33
TOG_n	1.355	1.35	1.355	1.355	1.365	1.36	1.35	1.35	1.355	1.35
Set_n	1.34	1.33	1.345	1.33	1.345	1.335	1.345	1.335	1.345	1.34
Resetn	1.35	1.345	1.35	1.345	1.355	1.35	1.355	1.35	1.345	1.345
oe_EAQ	1.36	1.35	1.355	1.35	1.365	1.355	1.36	1.355	1.355	1.35
enable_HSB	1.345	1.34	1.35	1.345	1.35	1.345	1.345	1.345	1.345	1.345
IO_Pattern_Length_1	1.35	1.345	1.355	1.35	1.355	1.35	1.355	1.355	1.35	1.35
IO_Pattern_Length_2	1.355	1.345	1.355	1.345	1.355	1.35	1.355	1.35	1.355	1.35

Table 7 Pre-Irradiation and Post-Annealing Input Thresholds (VIH)

Pin \ DUT(Dose)	11754 (300 krad)		11755 (300 krad)		11745 (200 krad)		11728 (100 krad)		11736 (100 krad)	
	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an
SEU_sel	1.625	1.6	1.625	1.6	1.63	1.61	1.63	1.62	1.625	1.61
zoom_sel_n_0	1.62	1.595	1.62	1.595	1.625	1.605	1.625	1.61	1.62	1.605
zoom_sel_n_1	1.63	1.605	1.63	1.605	1.63	1.61	1.635	1.62	1.625	1.615
zoom	1.625	1.605	1.625	1.6	1.63	1.61	1.63	1.62	1.62	1.61
TOG_n	1.64	1.635	1.645	1.635	1.65	1.64	1.635	1.63	1.64	1.635
Set_n	1.625	1.61	1.63	1.615	1.63	1.615	1.625	1.62	1.63	1.62
Resetn	1.625	1.62	1.625	1.615	1.63	1.62	1.63	1.625	1.62	1.615
oe_EAQ	1.63	1.62	1.63	1.62	1.635	1.625	1.63	1.625	1.63	1.62
enable_HSB	1.63	1.62	1.635	1.625	1.635	1.63	1.63	1.625	1.635	1.625
IO_Pattern_Length_1	1.635	1.625	1.64	1.63	1.64	1.63	1.645	1.635	1.64	1.635
IO_Pattern_Length_2	1.625	1.61	1.63	1.615	1.63	1.62	1.635	1.62	1.625	1.62

D. Output-Drive Voltage (VOL/VOH)

The pre-irradiation and post-annealing VOL/VOH are listed in Tables 6 and 7. The post-annealing data are within the specification limits; in each case, the radiation-induced degradation is within 10%.

Table 6 Pre-Irradiation and Post-Annealing VOL (mV)

Pin \ DUT(Dose)	11754 (300 krad)		11755 (300 krad)		11745 (200 krad)		11728 (100 krad)		11736 (100 krad)	
	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an
Array_out_EAQ_0	168.3	161.1	171	164.4	169.4	166.9	170.6	169.5	171.9	166.2
Array_out_EAQ_1	138.5	132.9	140.5	134.3	140.6	137.8	140.1	138	144.1	136.9
Array_out_EAQ_2	183.1	176.6	186.3	178.8	184.9	194.7	185.5	192.4	188.3	190.6
Global_Monitor_EAQ	140	133.5	143.1	136.4	142.6	140.7	142.2	139.8	143.7	137.9
Shiftout3	141.7	135.5	144.7	139	142.4	141.8	144.2	141.6	146.2	138.1
Shiftout7	146.1	139.4	147	140.3	148.6	143.8	146.5	144.6	149.1	144.6
Shiftout8	194.1	177.8	185.5	177.5	188	176.1	184.6	178.4	187.2	183.1
RAM_Monitor_EAQ	15.6	16.3	18.2	16.9	17	16.5	16.2	17.4	17.9	17
RAM_out_EAQ_0	17.8	17.3	18	17.1	18.2	17.5	18.3	17.6	19.8	17.5
RAM_out_EAQ_4	14.4	16.8	17.1	16.7	16.9	16.8	16.9	16.8	17.3	15.8
RAM_out_EAQ_8	16.9	17.2	17.5	17.1	18	16.9	18.1	17	17.4	17

Table 7 Pre-Irradiation and Post-Annealing VOH (V)

Pin \ DUT(Dose)	11754 (300 krad)		11755 (300 krad)		11745 (200 krad)		11728 (100 krad)		11736 (100 krad)	
	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an
Array_out_EAQ_0	2.737	2.736	2.734	2.732	2.737	2.734	2.735	2.733	2.732	2.736
Array_out_EAQ_1	2.776	2.773	2.774	2.77	2.774	2.77	2.774	2.772	2.769	2.772
Array_out_EAQ_2	2.72	2.719	2.72	2.718	2.718	2.708	2.717	2.709	2.716	2.707
Global_Monitor_EAQ	2.767	2.763	2.764	2.759	2.765	2.761	2.764	2.762	2.763	2.762
Shiftout3	2.769	2.769	2.767	2.766	2.768	2.768	2.766	2.767	2.764	2.767
Shiftout7	2.758	2.755	2.756	2.753	2.756	2.753	2.756	2.755	2.753	2.753
Shiftout8	2.722	2.722	2.723	2.723	2.724	2.725	2.723	2.726	2.718	2.725
RAM_Monitor_EAQ	2.957	2.955	2.957	2.955	2.958	2.956	2.957	2.957	2.956	2.957
RAM_out_EAQ_0	2.956	2.956	2.956	2.954	2.956	2.955	2.956	2.956	2.956	2.956
RAM_out_EAQ_4	2.957	2.958	2.957	2.956	2.958	2.957	2.958	2.957	2.957	2.958

E. Propagation Delay

Table 8 lists the pre-irradiation and post-annealing propagation delays. The results show small radiation effects; in any case, the percentage change is well below 10%.

Table 8 Radiation-Induced Propagation Delay Degradations

Delay (µs)							
	DUT	**Total Dose**	**Pre-rad**	**100 krad**	**200 krad**	**300 krad**	**Post-ann**
	11728	100 krad	8.15	8.13	-	-	8.1
	11736	100 krad	8.21	8.2	-	-	8.16
	11745	200 krad	8.22	8.21	8.29	-	8.13
	11754	300 krad	8.14	8.13	8.15	8.45	8.06
	11755	300 krad	8	8	8.08	8.26	7.93
Radiation Δ (%)							
	DUT	**Total Dose**	**Pre-rad**	**100 krad**	**200 krad**	**300 krad**	**Post-ann**
	11728	100 krad	-	-0.25%	-	-	-0.61%
	11736	100 krad	-	-0.12%	-	-	-0.61%
	11745	200 krad	-	-0.12%	0.79%	-	-1.16%
	11754	300 krad	-	-0.06%	0.18%	3.87%	-0.92%
	11755	300 krad	-	0.06%	1.00%	3.31%	-0.88%

F. Transition Time

Figure 8a to Figure 19b show the pre-irradiation and post-annealing transition edges. In each case, the radiation-induced transition-time degradation is not observable.

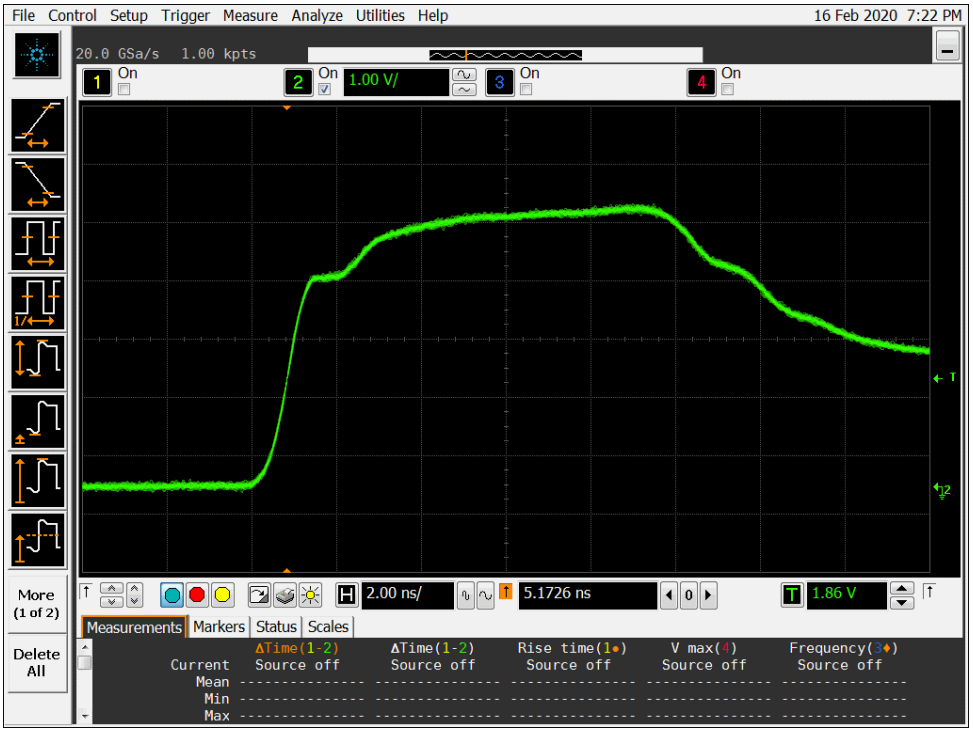

Figure 8a DUT 11754 Pre-Irradiation Rising Edge.

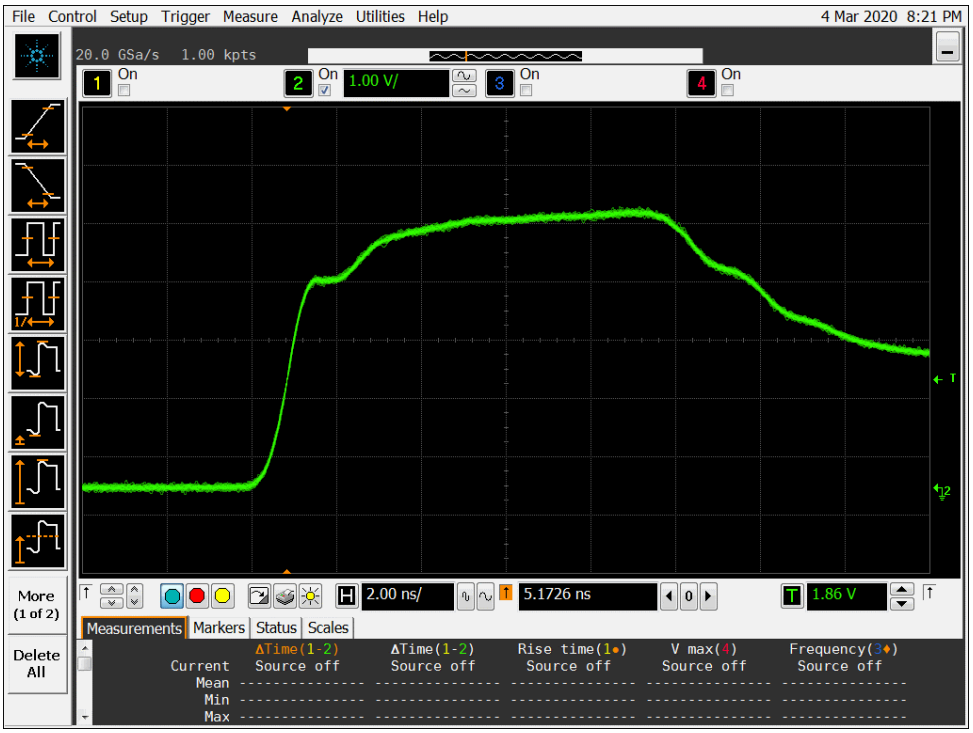

Figure 8b DUT 11754 Post-Annealing Rising Edge.

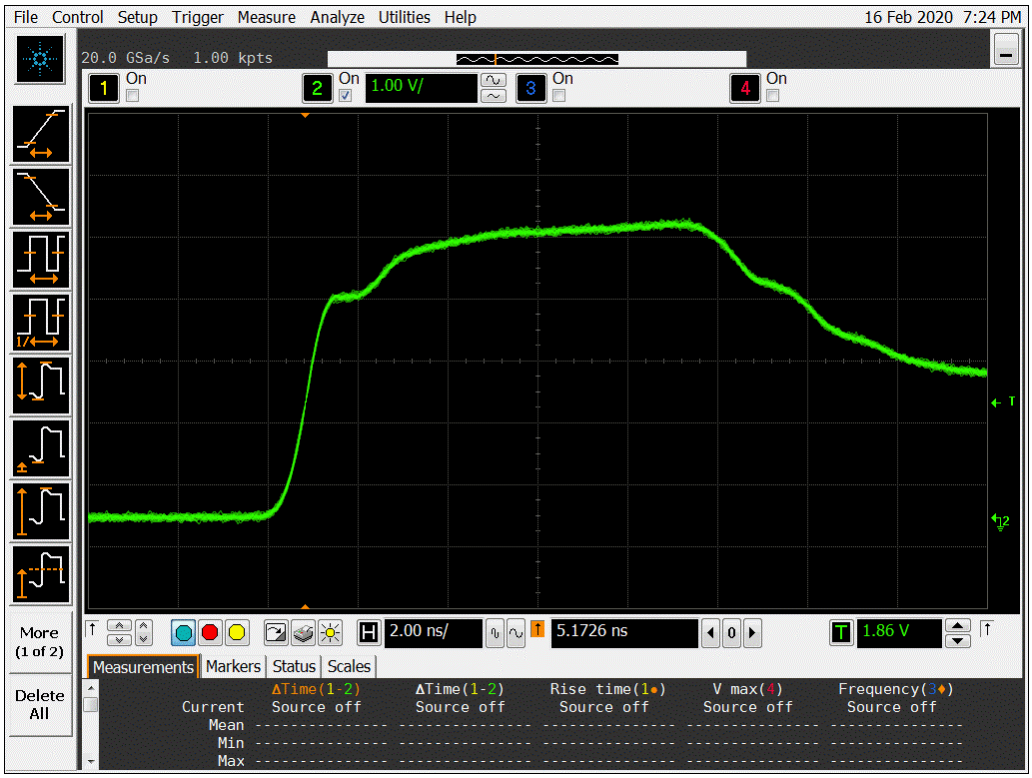

Figure 9a DUT 11755 Pre-irradiation Rising Edge.

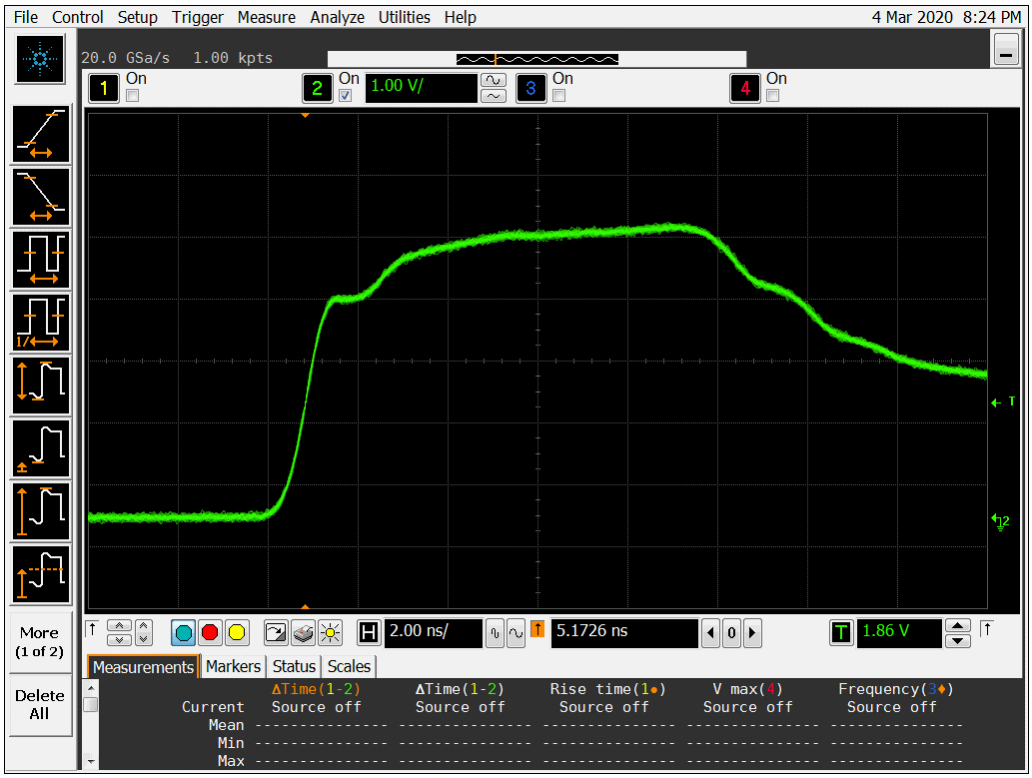

Figure 9b DUT 11755 Post-Annealing Rising Edge.

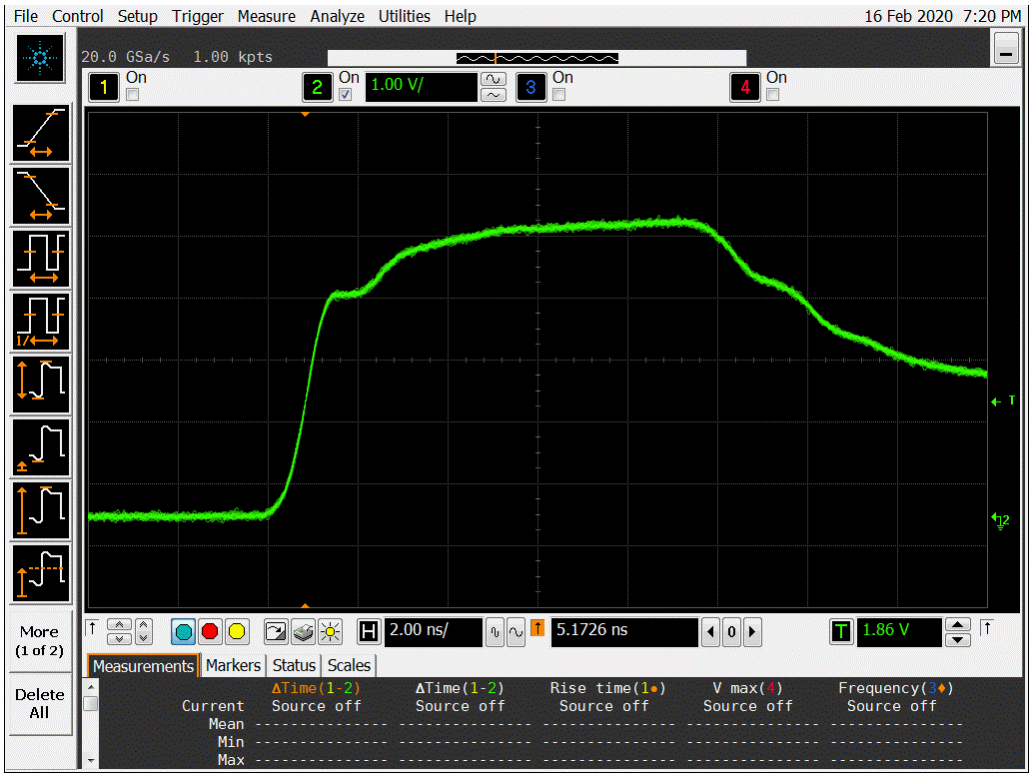

Figure 11a DUT 11745 Pre-Irradiation Rising Edge.

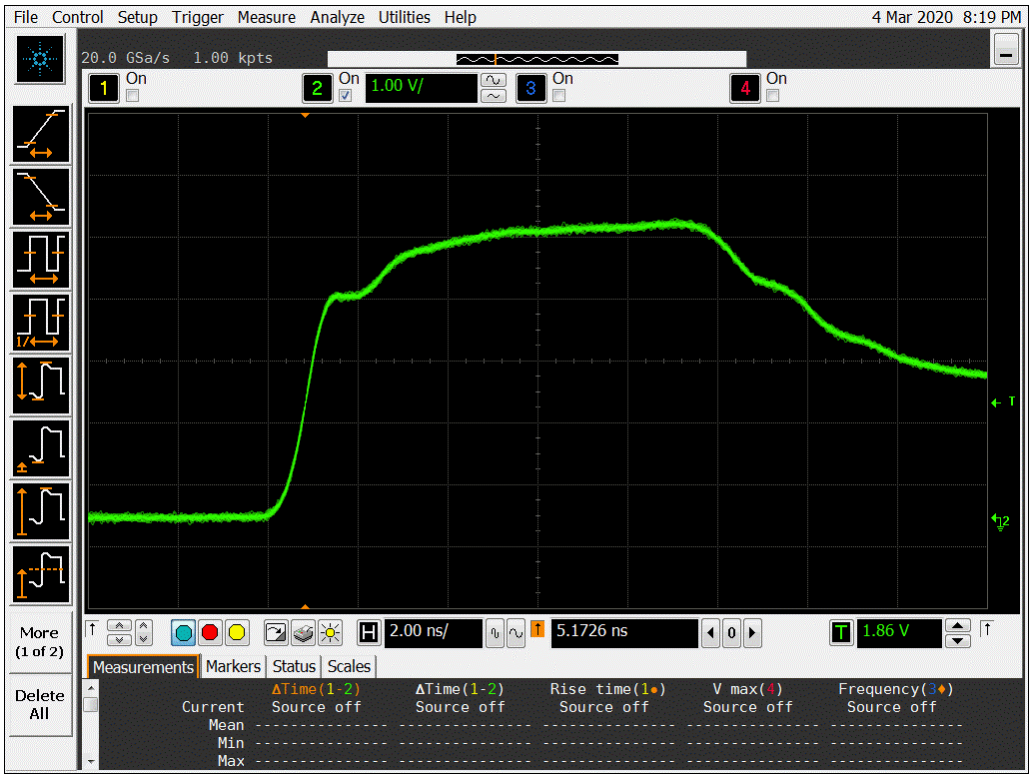

Figure 11b DUT 11745 Post-Annealing Rising Edge.

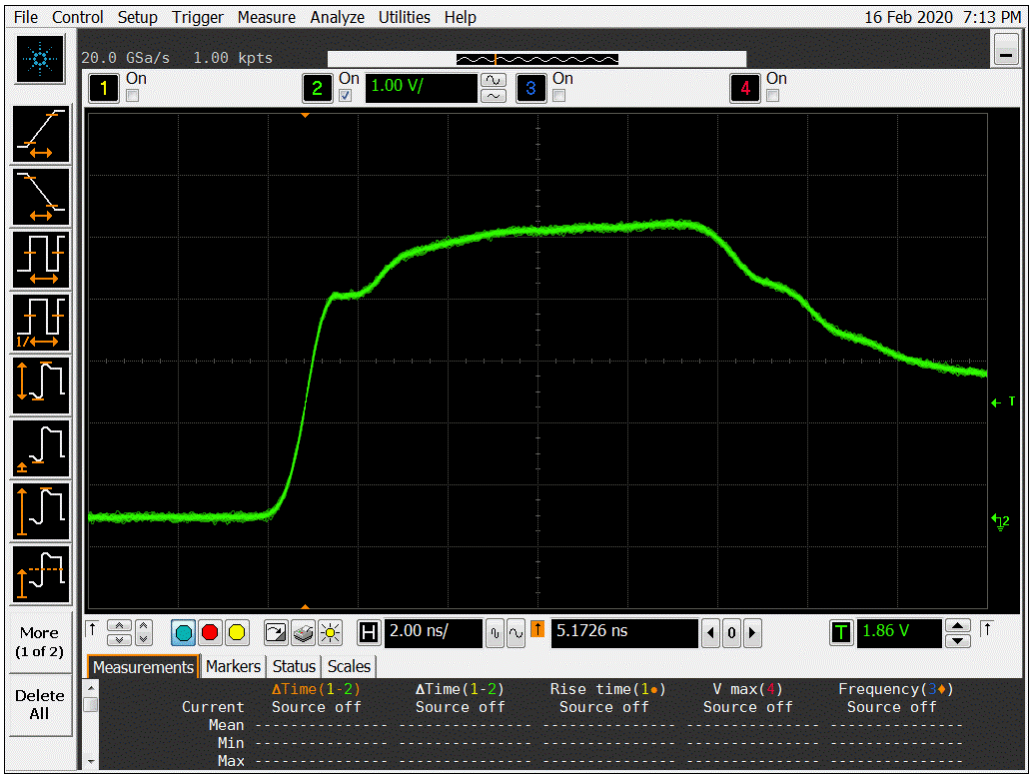

Figure 12a DUT 11728 Pre-Irradiation Rising Edge.

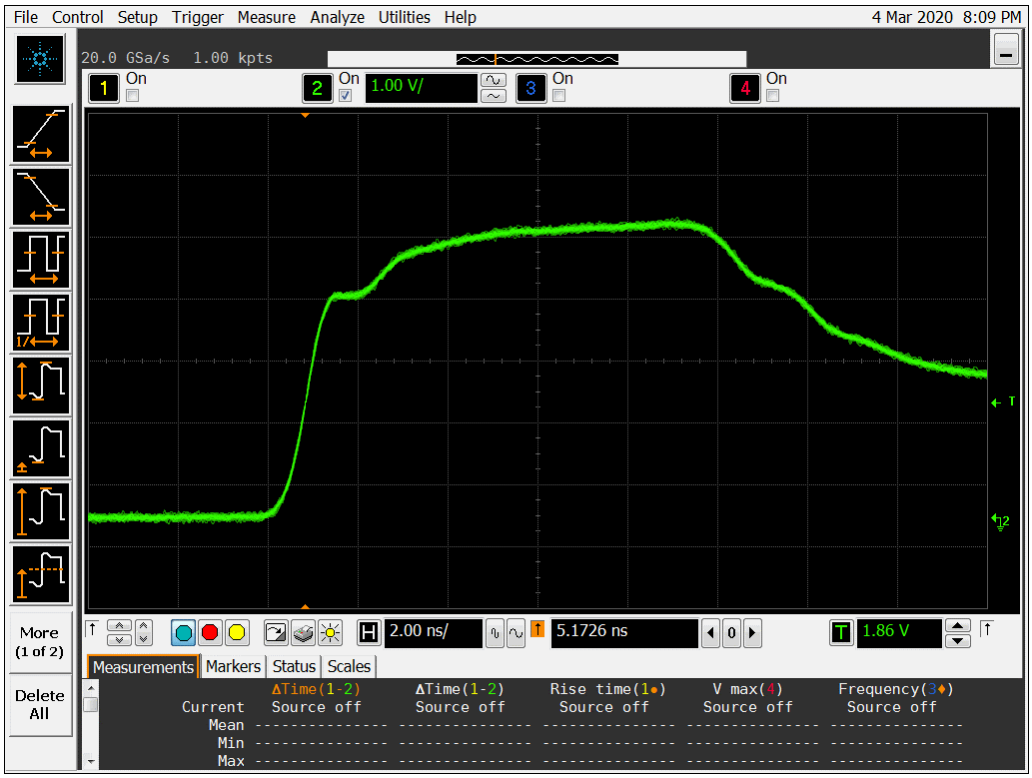

Figure 12b DUT 11728 Post-Annealing Rising Edge.

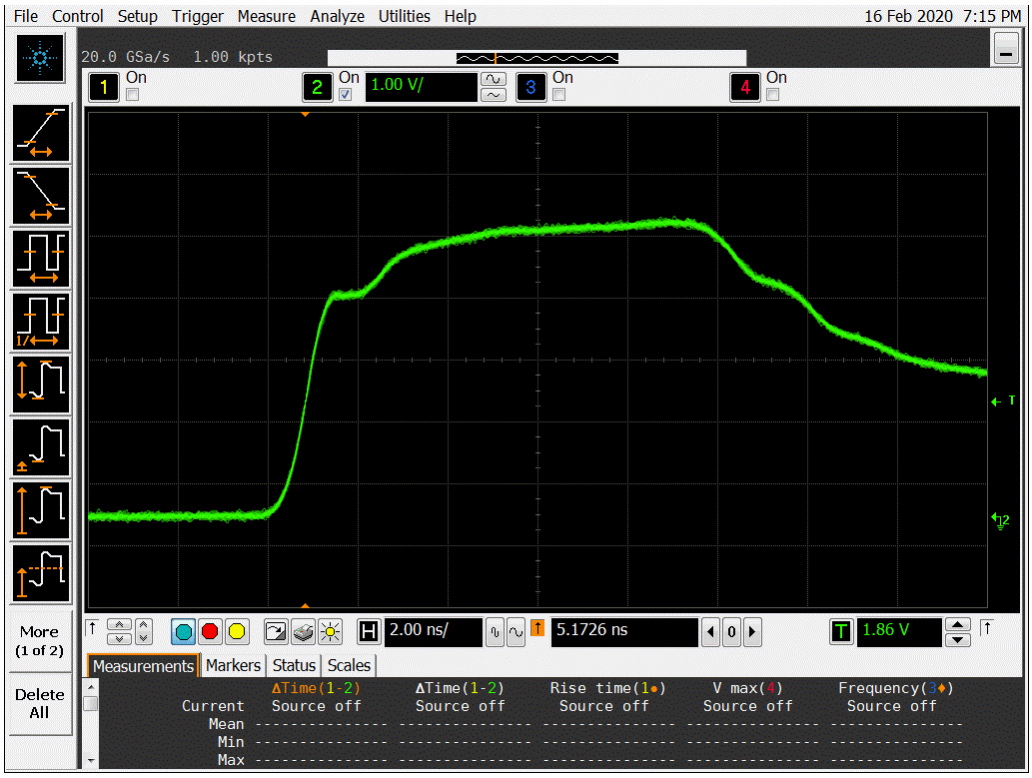

Figure 13a DUT 11736 Pre-Irradiation Rising Edge.

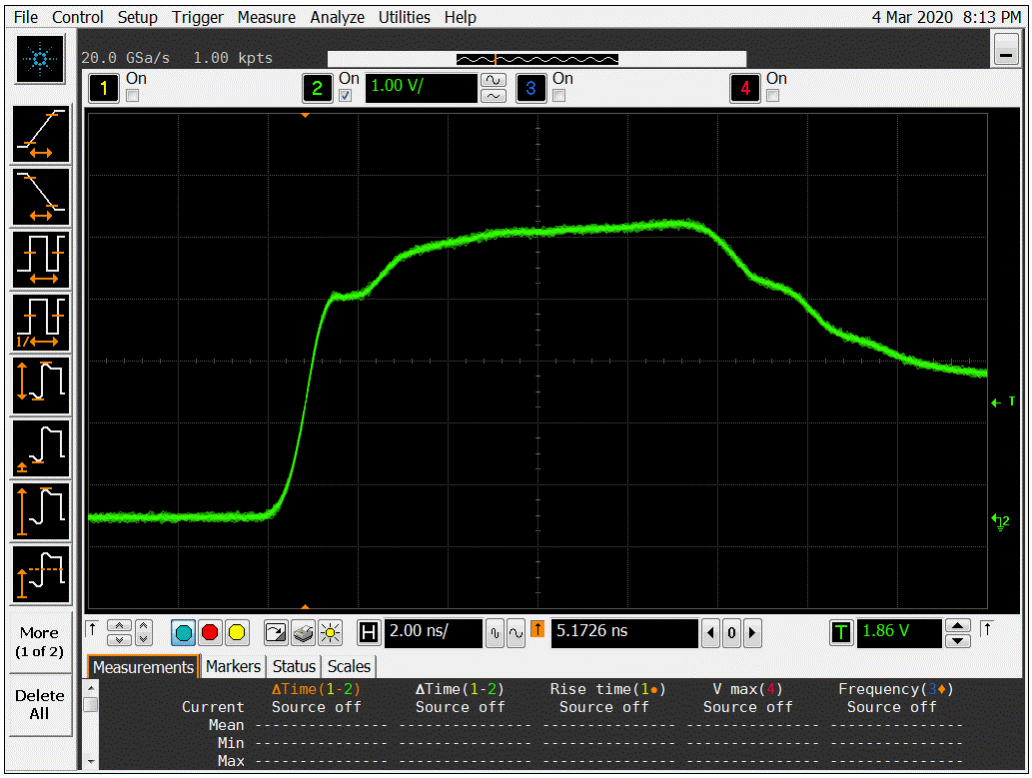

Figure 13b DUT 11736 Post-Annealing Rising Edge.

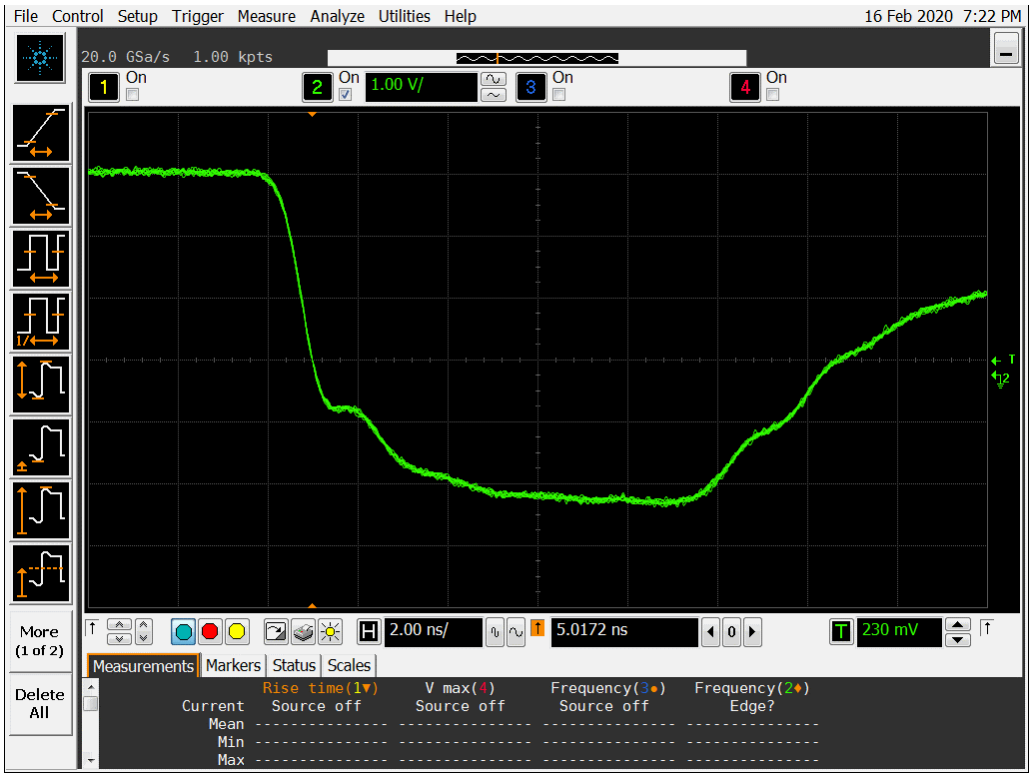

Figure 14a DUT 11754 Pre-Irradiation Falling Edge.

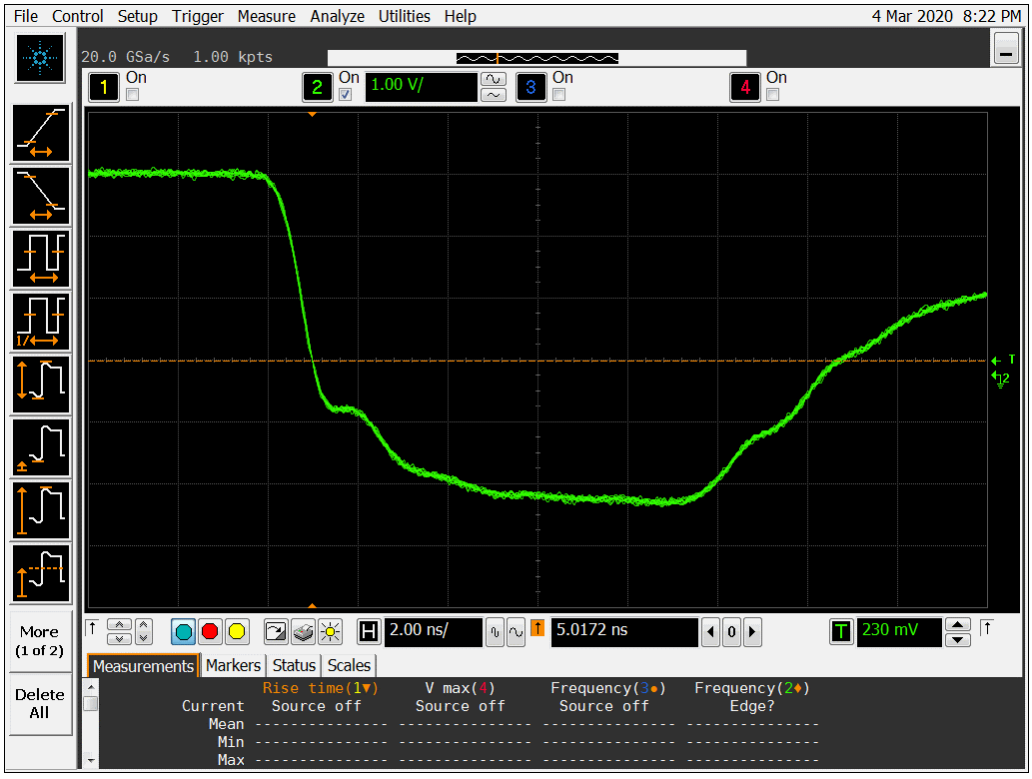

Figure 14b DUT 11754 Post-Annealing Falling Edge.

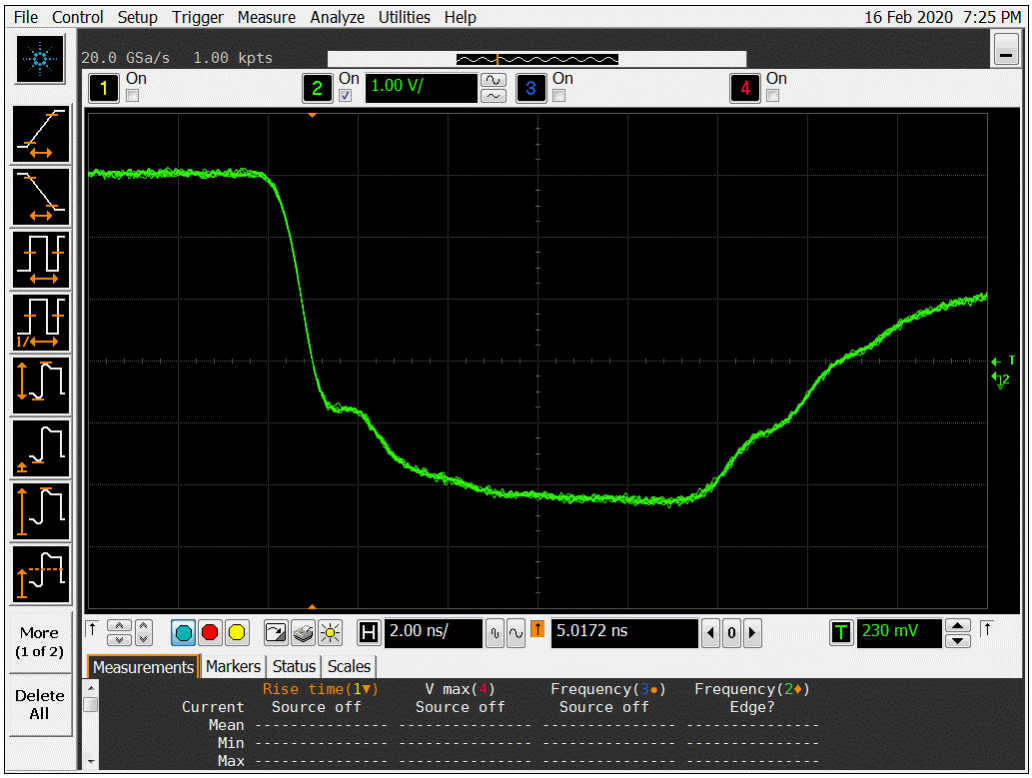

Figure 15a DUT 11755 Pre-Irradiation Falling Edge.

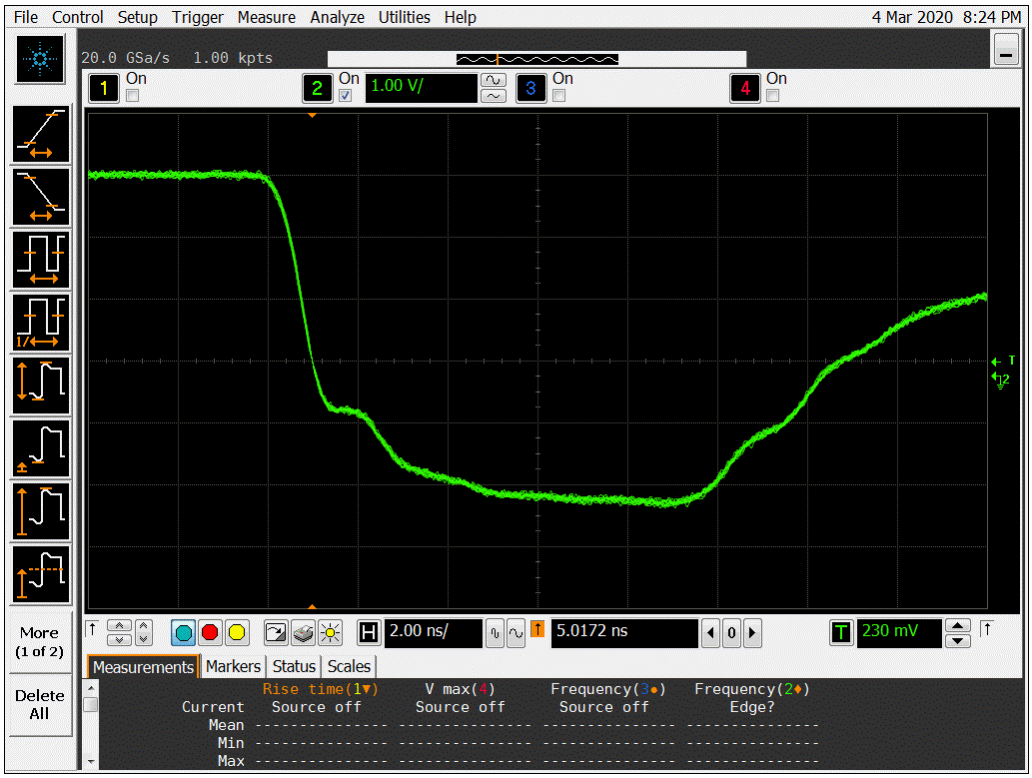

Figure 15b DUT 11755 Post-Annealing Falling Edge.

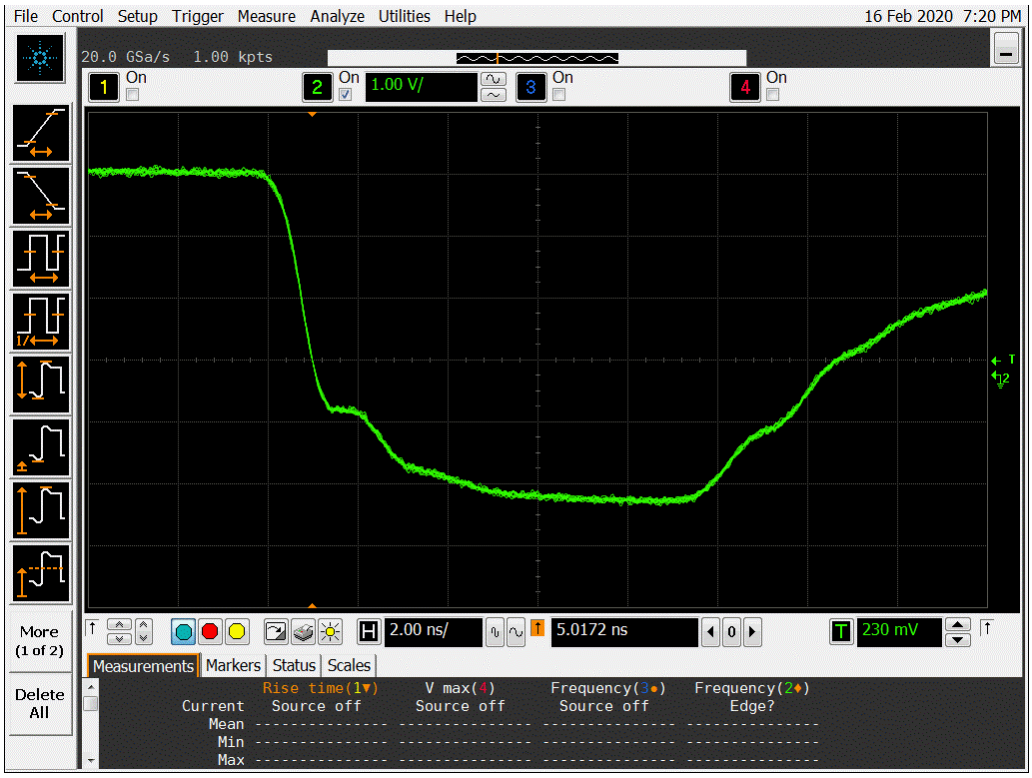

Figure 17a DUT 11745 Pre-Irradiation Falling Edge.

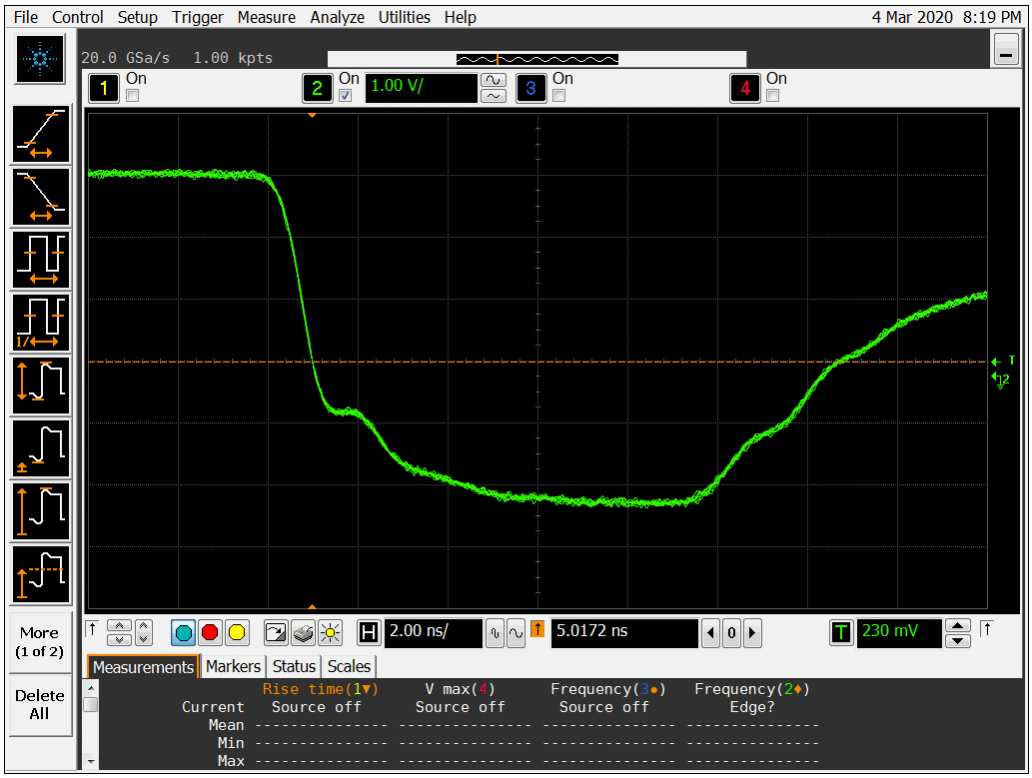

Figure 17b DUT 11745 Post-Annealing Falling Edge.

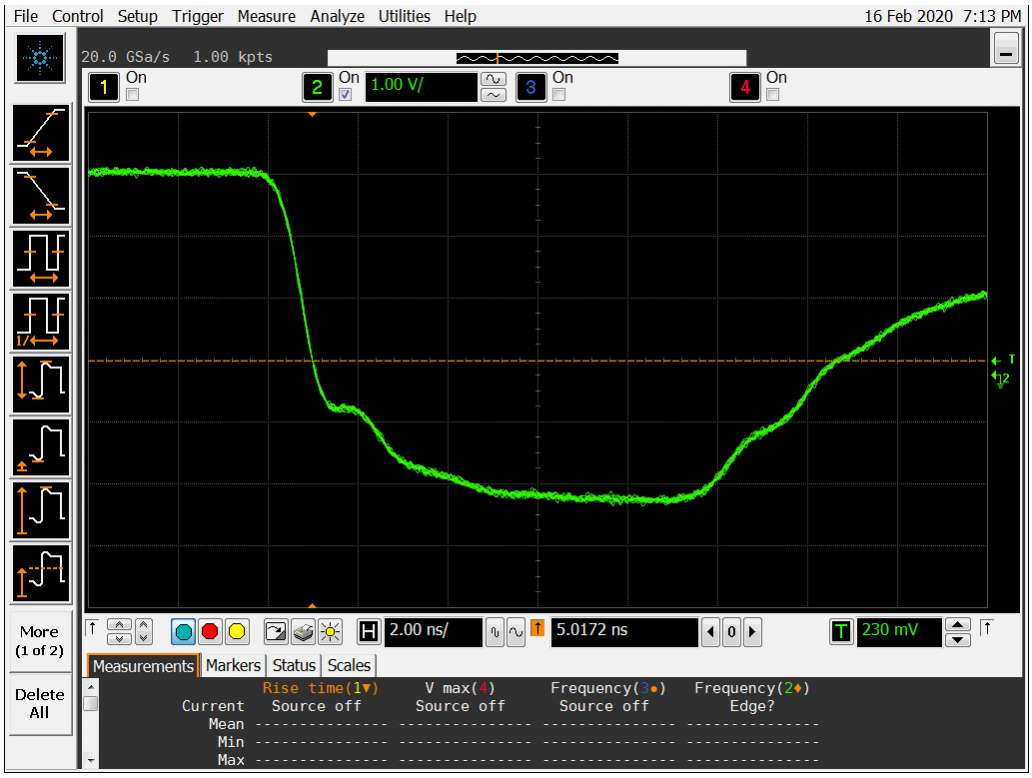

Figure 18a DUT 11728 Pre-Irradiation Falling Edge.

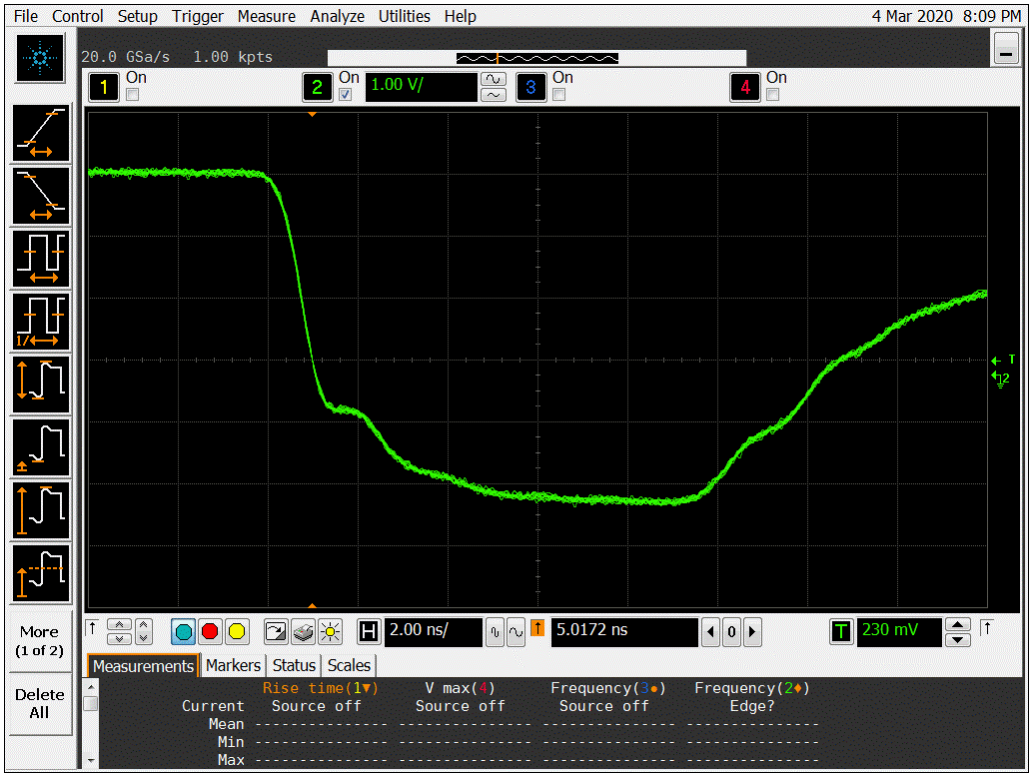

Figure 18b DUT 11728 Post-Annealing Falling Edge.

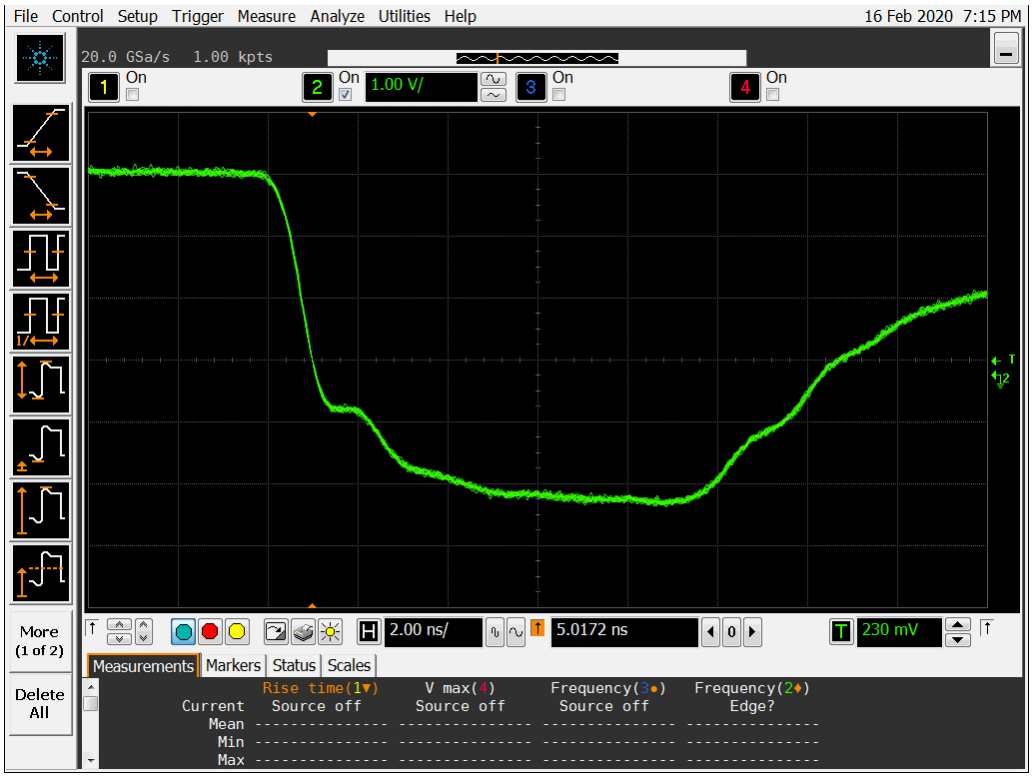

Figure 19a DUT 11736 Pre-Irradiation Falling Edge.

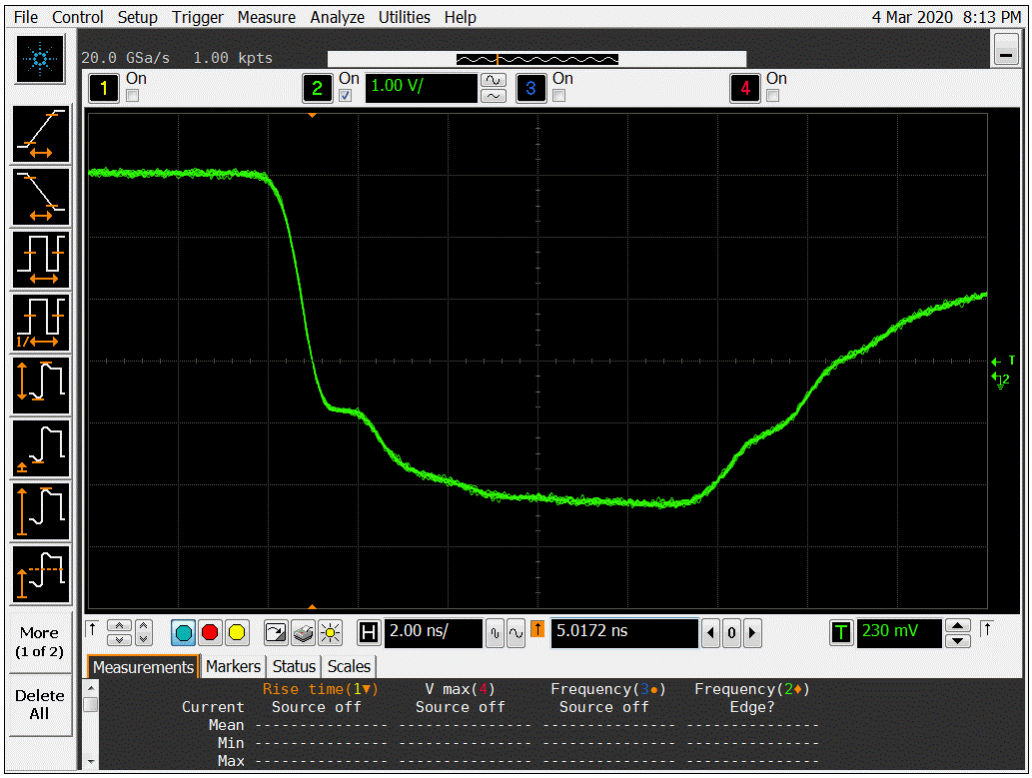

Figure 19b DUT 11736 Post-Annealing Falling Edge.

Appendix A: DUT Bias Diagram

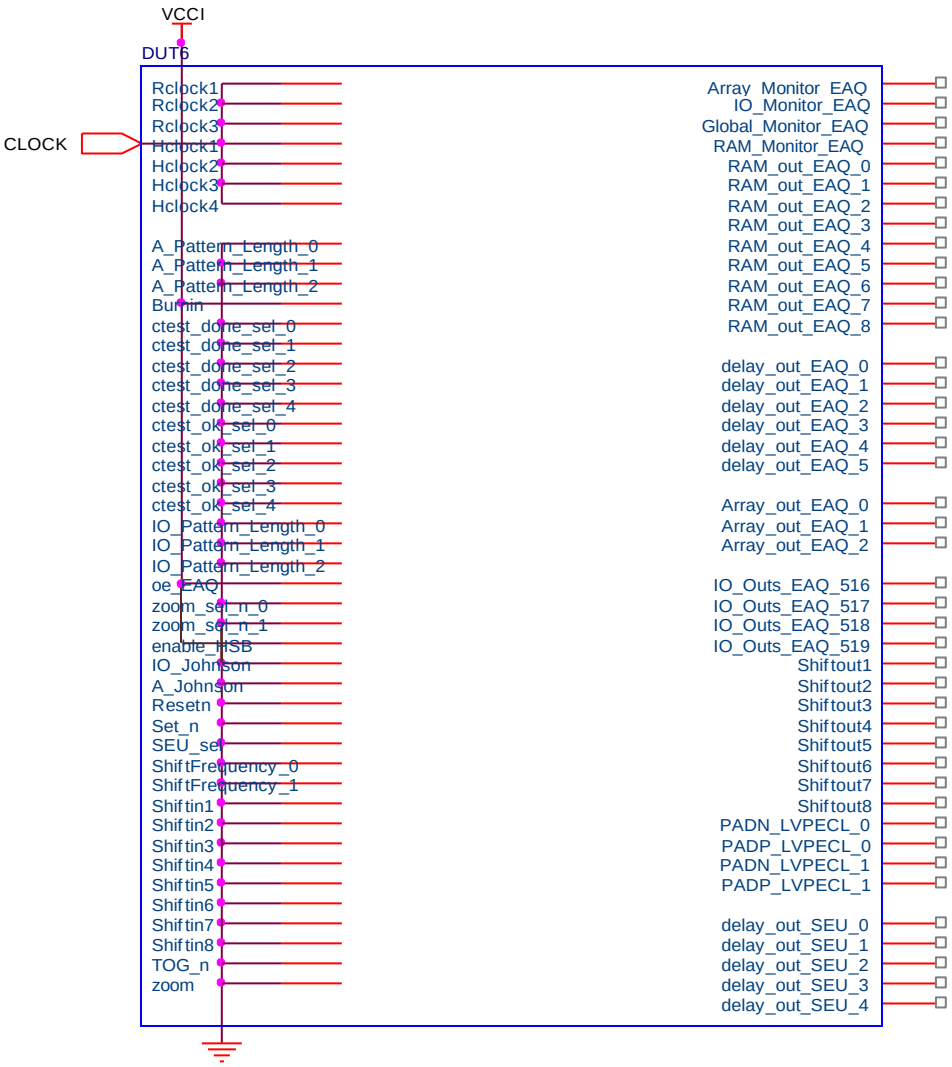

Figure A1 I/O Bias During Irradiation

VCCI_3.3

DUT1D

B11		AB10	
	VCCI1	VCCI	VCCR U
B14	VCCI1	8	VCCR VCCR VCCR VCCR VCCR VCCR VCCR VCCR VCCR VCCR
B17	VCCI1	VCCI	VCCR VCCR VCCR VCCR VCCR VCCR VPP1 VPP10 VPP11
B5	VCCI1	8	VPP12 VPP13 VPP14 VPP15 VPP16 VPP17 VPP18 VPP19 VPP2
B8	VCCI1	VCCI	VPP20 VPP21 VPP22 VPP23 VPP24 VPP25 VPP26 VPP27 VPP28
F11	VCCI1	8	VPP29 VPP3 VPP30 VPP4 VPP5 VPP6 VPP7 VPP8 VPP9 VSV
F14	VCCI1		VSV VSV VSV VSV VSV VSV VSV
F17	VCCI1		
F8	VCCI1		
K11	VCCI1		
K14	VCCI1		
K17	VCCI1		
N15	VCCI1		VCC VCC VCC VCC VCC VCC VCC VCC VCC VCC VCC VCC VCC
N17	VCCI1		VCC VCC VCC VCC VCC VCC VCC VCC VCC VCC VCC VCC VCC
B20	VCCI1		VCC VCC VCC VCC VCC VCC VCC VCC VCC VCC VCC VCC VCC
B23	VCCI2		VCC VCC VCC VCC VCC VCC VCC VCC VCC VCC VCC VCC VCC
B26	VCCI2		VCC VCC VCC VCC VCC VCC
B29	VCCI2		
B32	VCCI2		
F20	VCCI2		
F23	VCCI2		
F26	VCCI2		
F29	VCCI2		
K20	VCCI2		
K23	VCCI2		
K26	VCCI2		
N20	VCCI2		
N22	VCCI2		
E35	VCCI2		
H31	VCCI3		
H35	VCCI3		
K27	VCCI3		
L31	VCCI3		
L35	VCCI3		
P27	VCCI3		
P31	VCCI3		
P35	VCCI3		
R24	VCCI3		
U24	VCCI3		
U27	VCCI3		
U31	VCCI3		
U35	VCCI3		
AB24	VCCI3		
AC27	VCCI4		
AC31	VCCI4		
AC35	VCCI4		
AF31	VCCI4		
AF35	VCCI4		
AG27	VCCI4		
AJ31	VCCI4		
AJ35	VCCI4		
AM35	VCCI4		
Y24	VCCI4		
Y27	VCCI4		
Y31	VCCI4		
Y35	VCCI4		
AD20	VCCI4		
AD22	VCCI5		
AG20	VCCI5		
AG23	VCCI5		
AG26	VCCI5		
AL20	VCCI5		
AL23	VCCI5		
AL26	VCCI5		
AL29	VCCI5		
AR20	VCCI5		
AR23	VCCI5		
AR26	VCCI5		
AR29	VCCI5		
AR32	VCCI5		
AD15	VCCI5		
AD17	VCCI6		
AG11	VCCI6		
AG14	VCCI6		
AG17	VCCI6		
AL11	VCCI6		
AL14	VCCI6		
AL17	VCCI6		
AL8	VCCI6		
AR11	VCCI6		
AR14	VCCI6		
AR17	VCCI6		
AR5	VCCI6		
AR8	VCCI6		
AB13	VCCI6		
AC10	VCCI7		
AC2	VCCI7		
AC6	VCCI7		
AF2	VCCI7		
AF6	VCCI7		
AG10	VCCI7		
AJ2	VCCI7		
AJ6	VCCI7		
AM2	VCCI7		
Y10	VCCI7		
Y13	VCCI7		
Y2	VCCI7		
Y6	VCCI7		
E2	VCCI7		
H2	VCCI8		
H6	VCCI8		
K10	VCCI8		
L2 L6	VCCI8		
P10	VCCI8		
P2	VCCI8		
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R13	VCCI8		
U10	VCCI8		
U13	VCCI8		
U2	VCCI8		

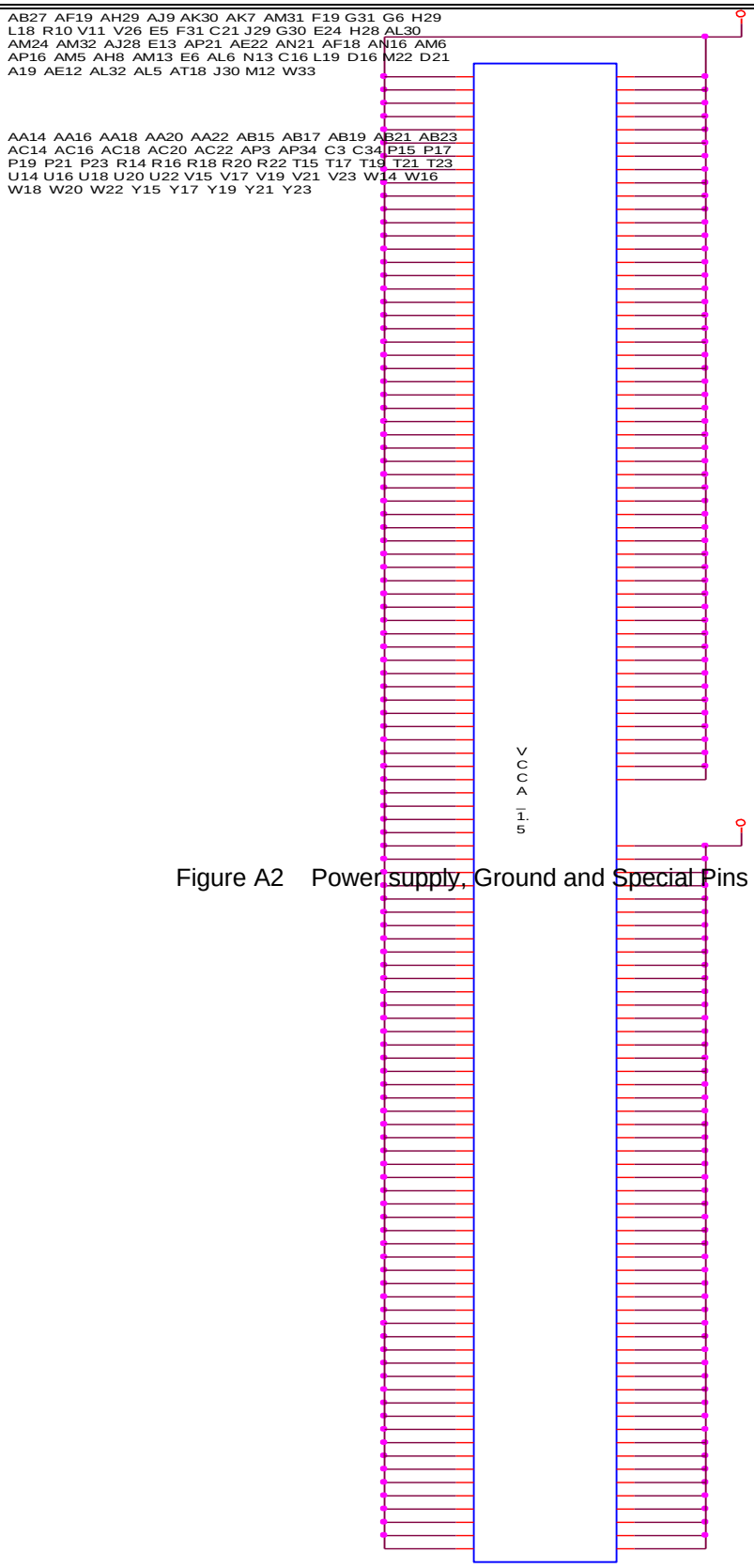

Figure A2 Power supply, Ground and Special Pins Bias During Irradiation

Appendix B: Functionality Tests

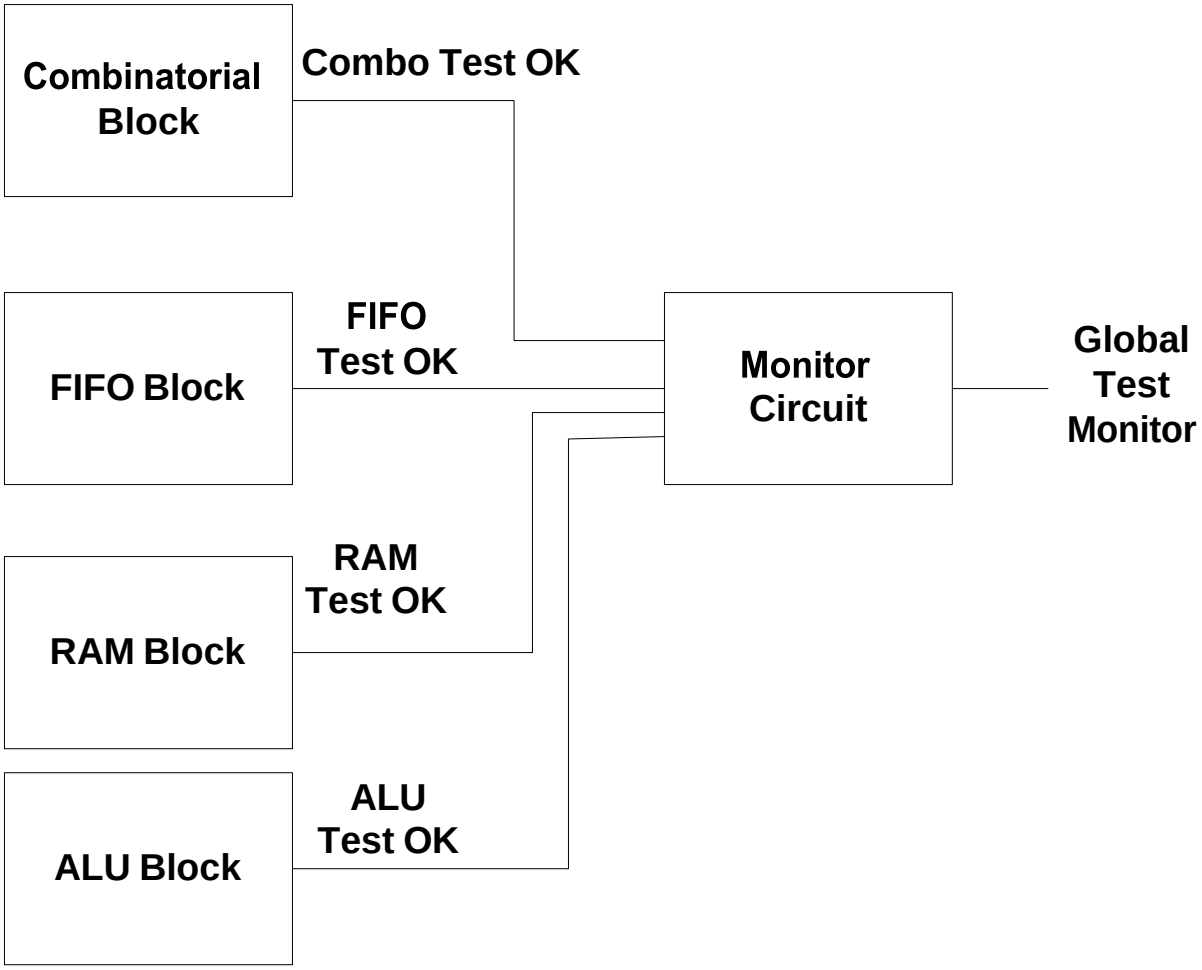

Figure B1 QBI Block – Top-Level Design

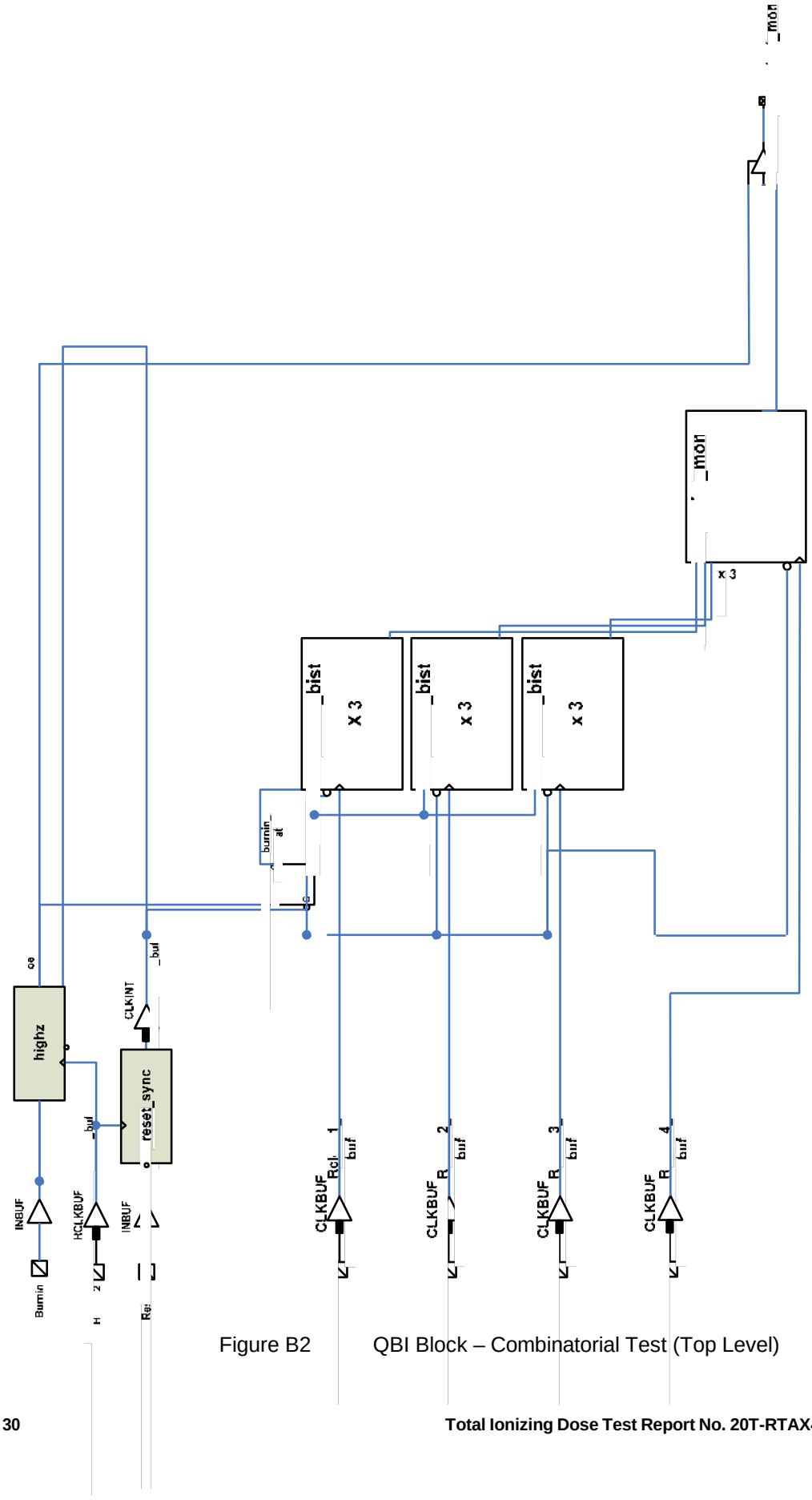

Figure B2 QBI Block – Combinatorial Test (Top Level)

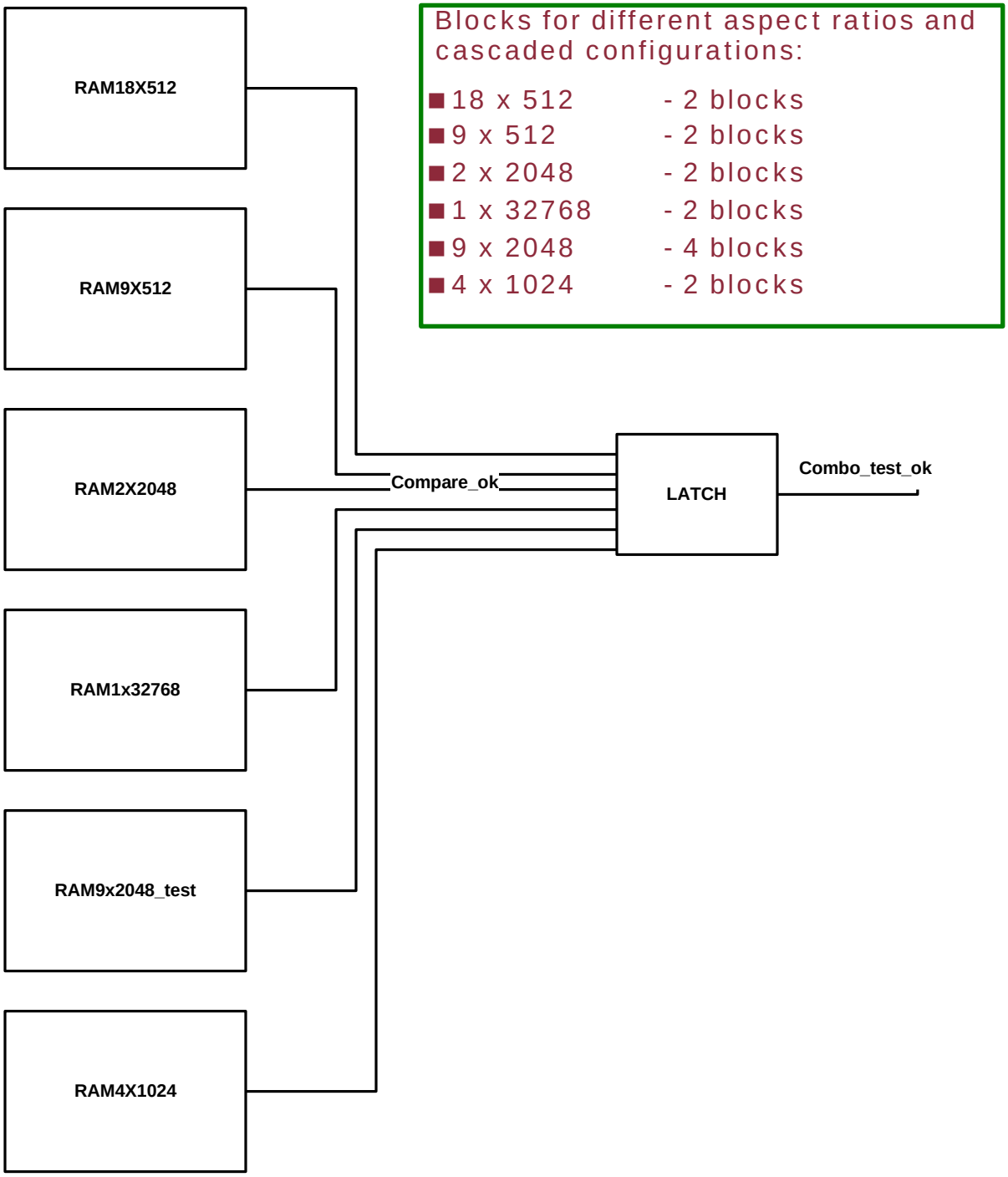

Figure B3 QBI Block – RAM Test (Top Level)

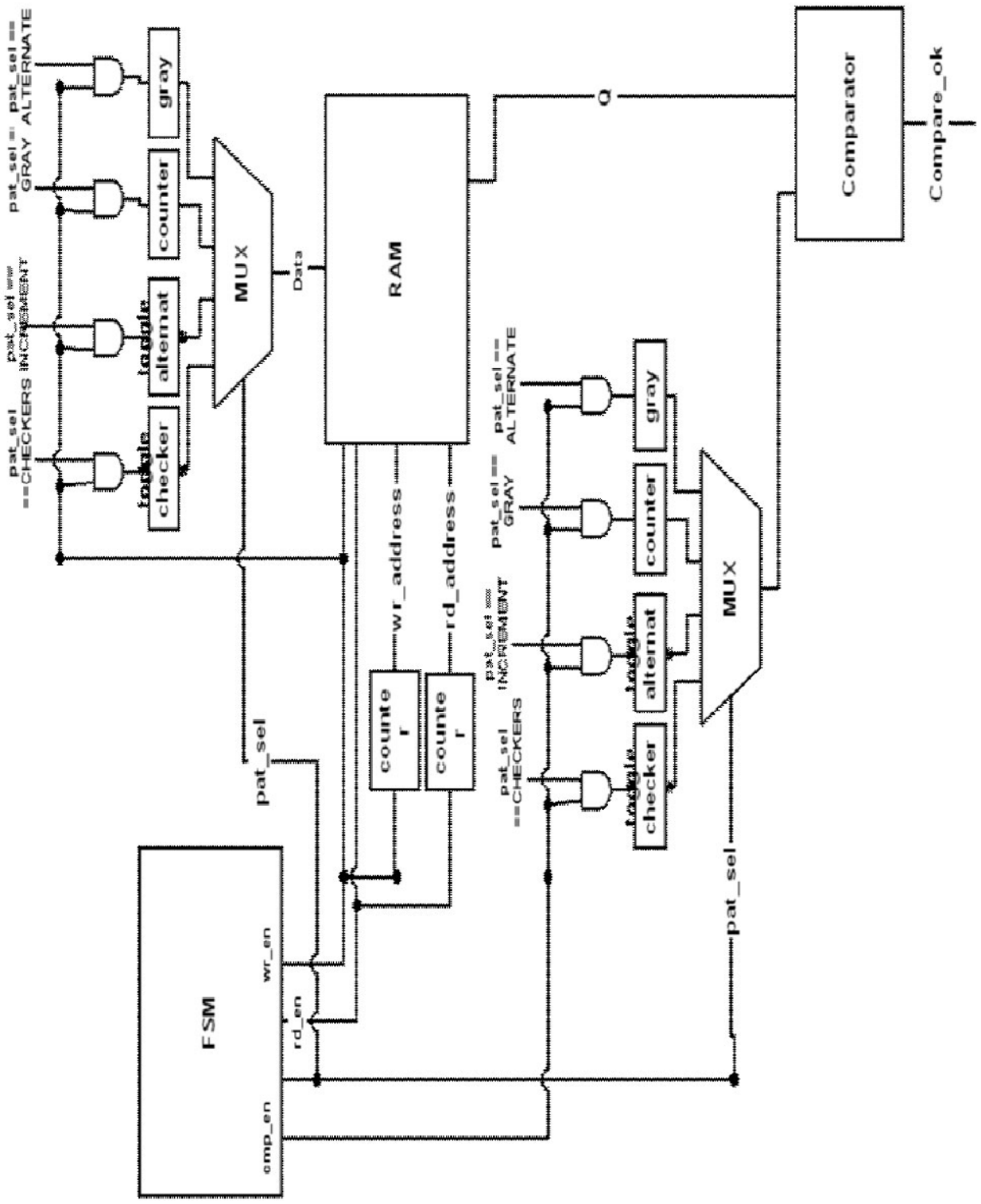

Figure B4 QBI Block – RAM Block

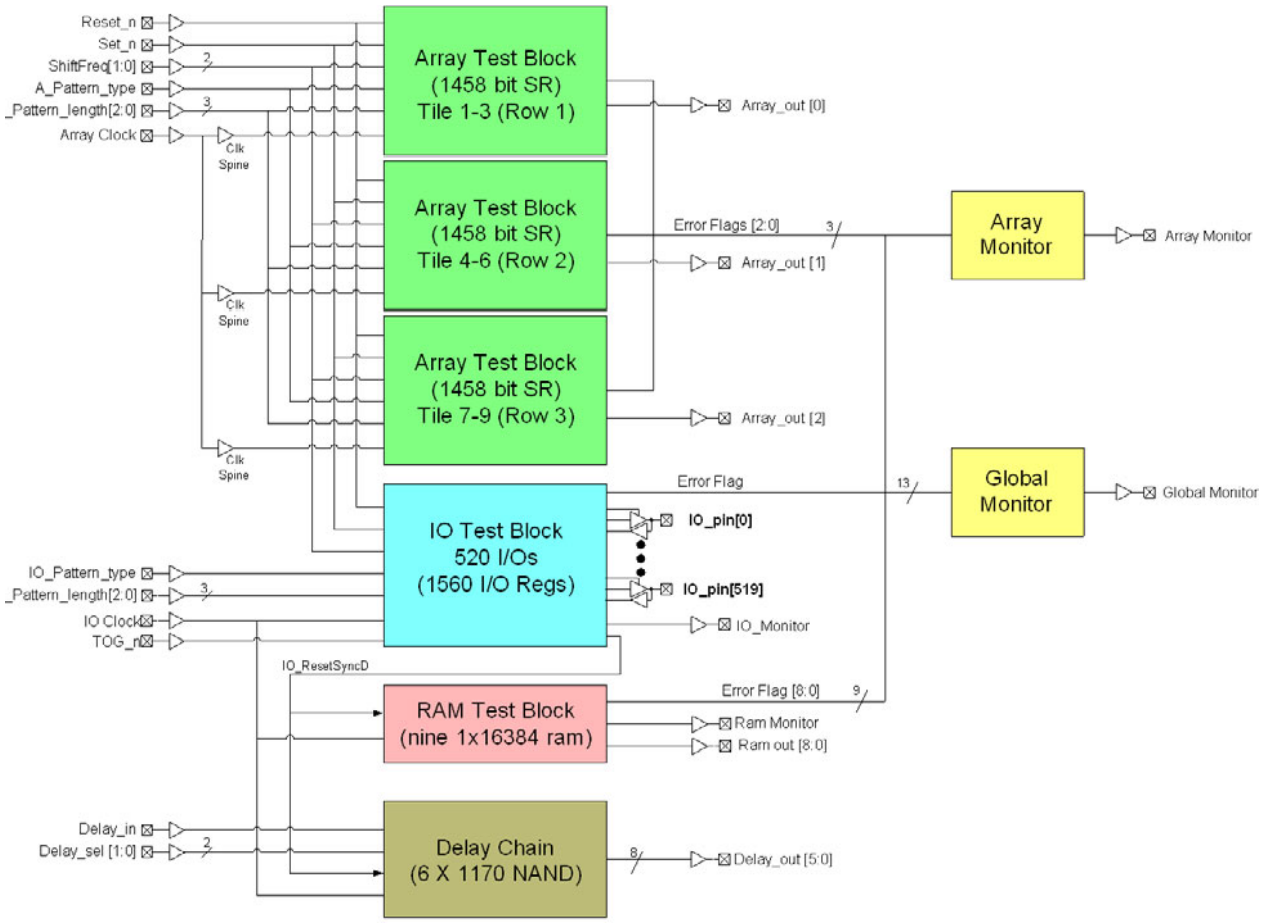

Figure B5 EAQ Block – Top Level

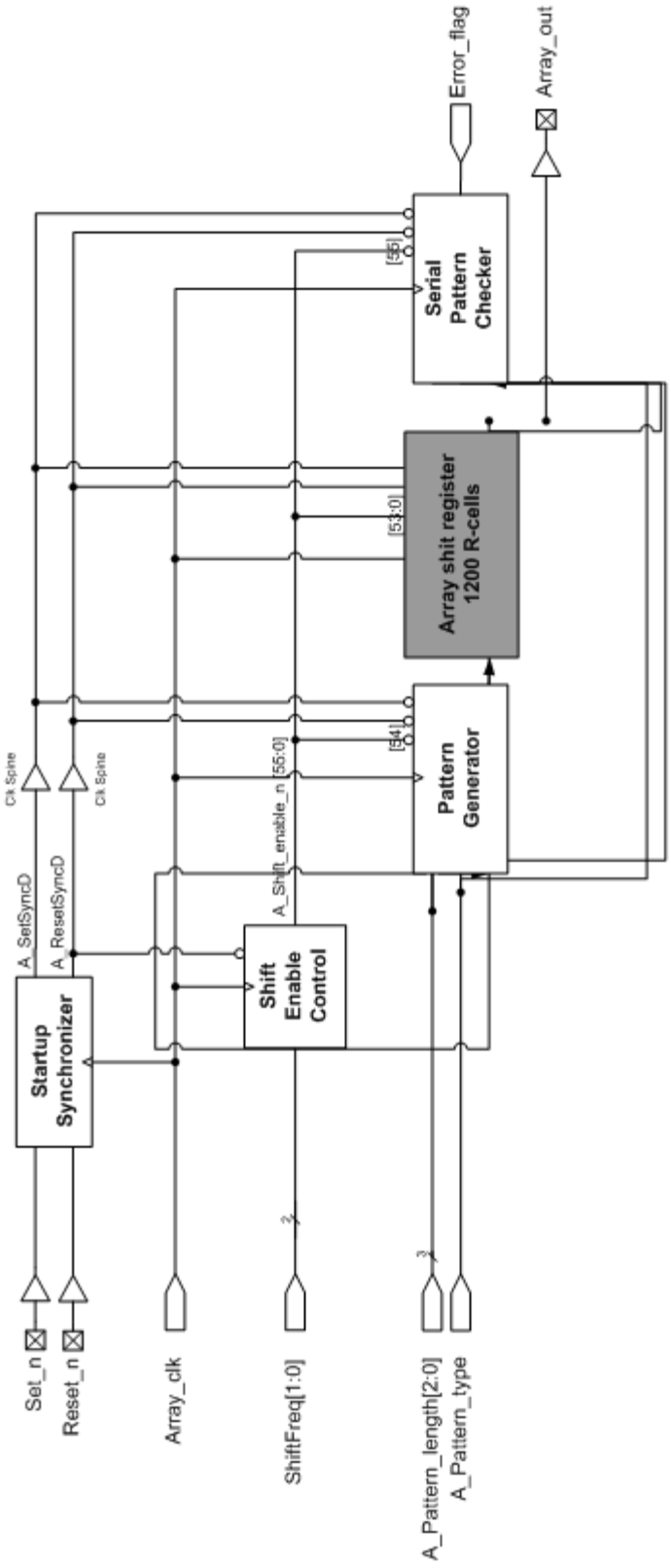

Figure B6 EAQ Block – Array Test (Shift Register)

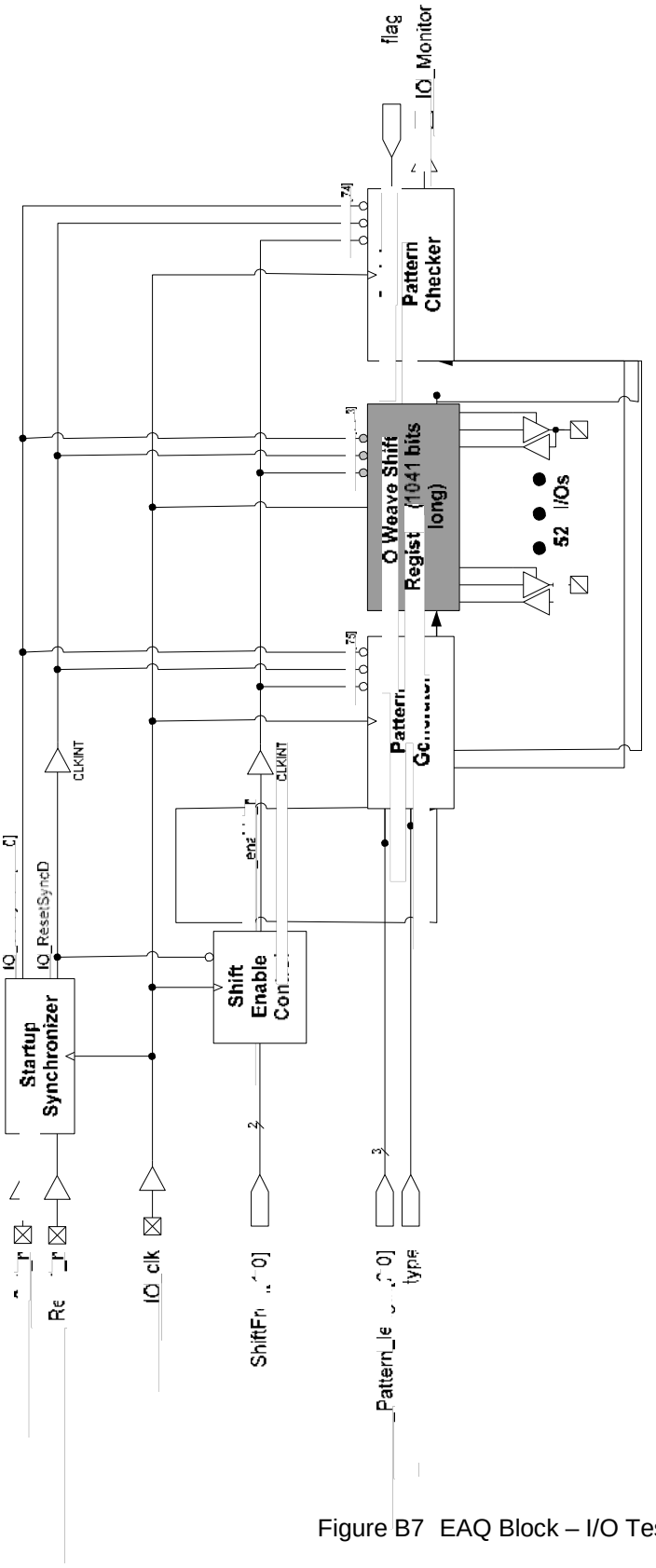

Figure B7 EAQ Block – I/O Test (Top Level)

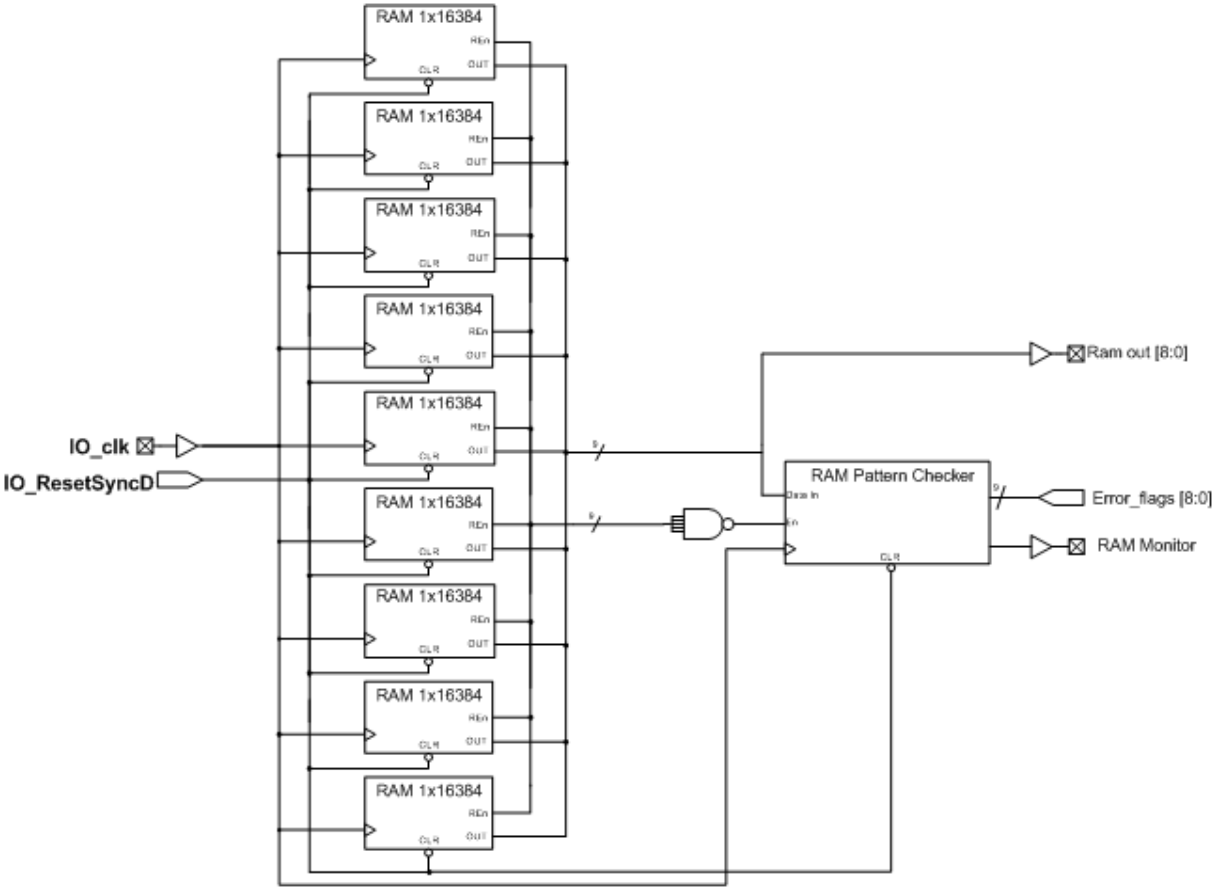

Figure B8 EAQ Block – SRAM Test (Top Level)

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