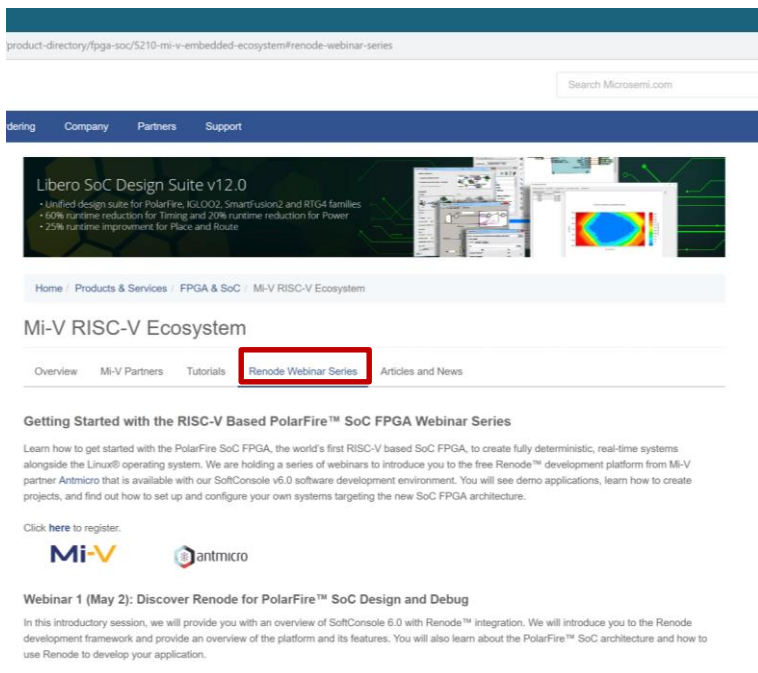


First / Second Thursdays

- Jan. 9 - Webinar 9: Getting Started with PolarFire® SoC**
- Feb. 13 - Webinar 10: Introduction to the PolarFire SoC Baremetal Library**
- Mar. 12 - Webinar 11: Handling Binaries**
- April 9 - Webinar 12: Two Baremetal Applications on PolarFire SoC**
- May 14 - Webinar 13: Linux on Renode**
- June 11 - Webinar 14: Building Applications for Linux on PolarFire SoC**
- July 9 - Webinar 15: Real-Time (AMP Mode) on PolarFire SoC**

Supporting Content

www.microsemi.com/Mi-V “Renode Webinar Series”



The screenshot shows the Microsemi website's navigation and content area. The top navigation bar includes links for "Ordering", "Company", "Partners", and "Support". Below this, a search bar is present. The main content area features a banner for "Libero SoC Design Suite v12.0" with bullet points: "Unified design suite for PolarFire, IGLOO2, SmartFusion2 and RTG4 families", "60% runtime reduction for Timing and 20% runtime reduction for Power", and "25% runtime improvement for Place and Route". Below the banner, a breadcrumb trail reads "Home / Products & Services / FPGA & SoC / Mi-V RISC-V Ecosystem". The "Mi-V RISC-V Ecosystem" section has a sub-navigation bar with "Overview", "Mi-V Partners", "Tutorials", "Renode Webinar Series" (highlighted with a red box), and "Articles and News". The "Renode Webinar Series" section is titled "Getting Started with the RISC-V Based PolarFire™ SoC FPGA Webinar Series" and contains introductory text about the series. At the bottom, there is a "Click here to register." link and logos for "Mi-V" and "antmicro".

product-directory/fpga-soc/5210-mi-v-embedded-ecosystem/renode-webinar-series

Search Microsemi.com

Ordering Company Partners Support

Libero SoC Design Suite v12.0

- Unified design suite for PolarFire, IGLOO2, SmartFusion2 and RTG4 families
- 60% runtime reduction for Timing and 20% runtime reduction for Power
- 25% runtime improvement for Place and Route

Home / Products & Services / FPGA & SoC / Mi-V RISC-V Ecosystem

Mi-V RISC-V Ecosystem

Overview Mi-V Partners Tutorials **Renode Webinar Series** Articles and News

Getting Started with the RISC-V Based PolarFire™ SoC FPGA Webinar Series

Learn how to get started with the PolarFire SoC FPGA, the world's first RISC-V based SoC FPGA, to create fully deterministic, real-time systems alongside the Linux® operating system. We are holding a series of webinars to introduce you to the free Renode™ development platform from Mi-V partner Antmicro that is available with our SoftConsole v6.0 software development environment. You will see demo applications, learn how to create projects, and find out how to set up and configure your own systems targeting the new SoC FPGA architecture.

Click [here](#) to register.

Mi-V antmicro

Webinar 1 (May 2): Discover Renode for PolarFire™ SoC Design and Debug

In this introductory session, we will provide you with an overview of SoftConsole 6.0 with Renode™ integration. We will introduce you to the Renode development framework and provide an overview of the platform and its features. You will also learn about the PolarFire™ SoC architecture and how to use Renode to develop your application.

Webinar 1: Discover Renode for PolarFire® SoC Design and Debug

Webinar 2: How to Get Started with Renode for PolarFire SoC

Webinar 3: Learn to Debug a Bare-Metal PolarFire SoC Application with Renode

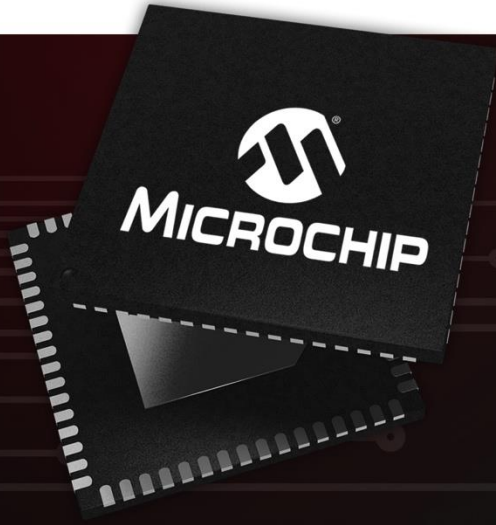
Webinar 4: Tips and Tricks for Even Easier PolarFire SoC Debug with Renode

Webinar 5: Add and Debug PolarFire SoC models with Renode

Webinar 6: Add and Debug Pre-Existing model in PolarFire SoC

Webinar 7: How to Write Custom Models

Webinar 8: What's New in SoftConsole v6.2



A Leading Provider of Microcontroller, Security,
Mixed-Signal, Analog & Flash-IP Solutions



Getting Started with the RISC-V Based PolarFire® SoC FPGA Webinar Series
Session 9: Getting Started with PolarFire® SoC

Hugh Breslin, Design Engineer
Thursday Jan. 9, 2019

Agenda

- **Getting Started with Libero SoC v12.3**
- **Creating a PolarFire SoC Design in Libero SoC v12.3**
- **Modifying the Renode Model and MPFS Blinky**



Getting Started with Libero SoC v12.3



Getting Started with Libero SoC v12.3

- www.microsemi.com/liberosoc
- Create a PolarFire SoC Project with an EAP license
- Libero SoC v12.3 released December 10th
- Libero SoC v12.0:
Software Tool of the Year – 2019 WEAA
- www.microsemi.com/polarfiresoc
- polarfiresoc@microchip.com



Getting Started with Libero SoC v12.3



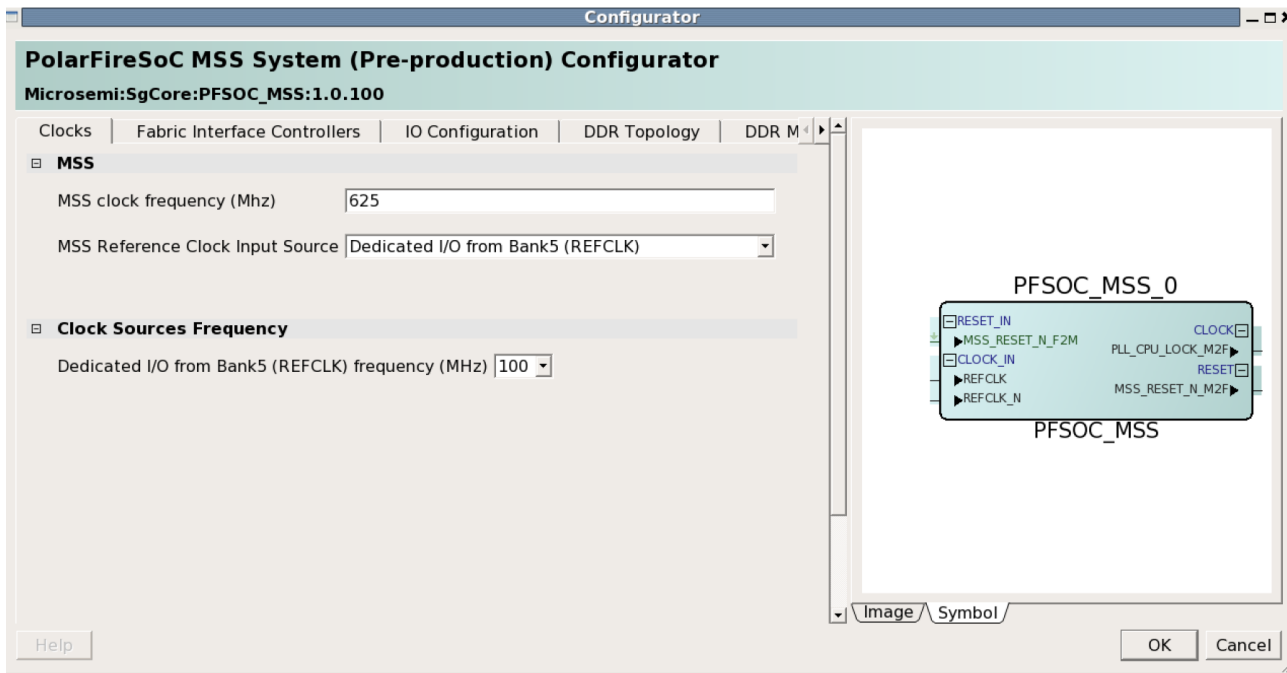
Getting Started with Libero SoC v12.3

Clocks tab:

Set MSS clock frequency

Select clock source

Set reference frequency



Getting Started with Libero SoC v12.3

Fabric Interface Controllers:

FIC 0 AXI4

- Master
- Slave

FIC 1 AXI4

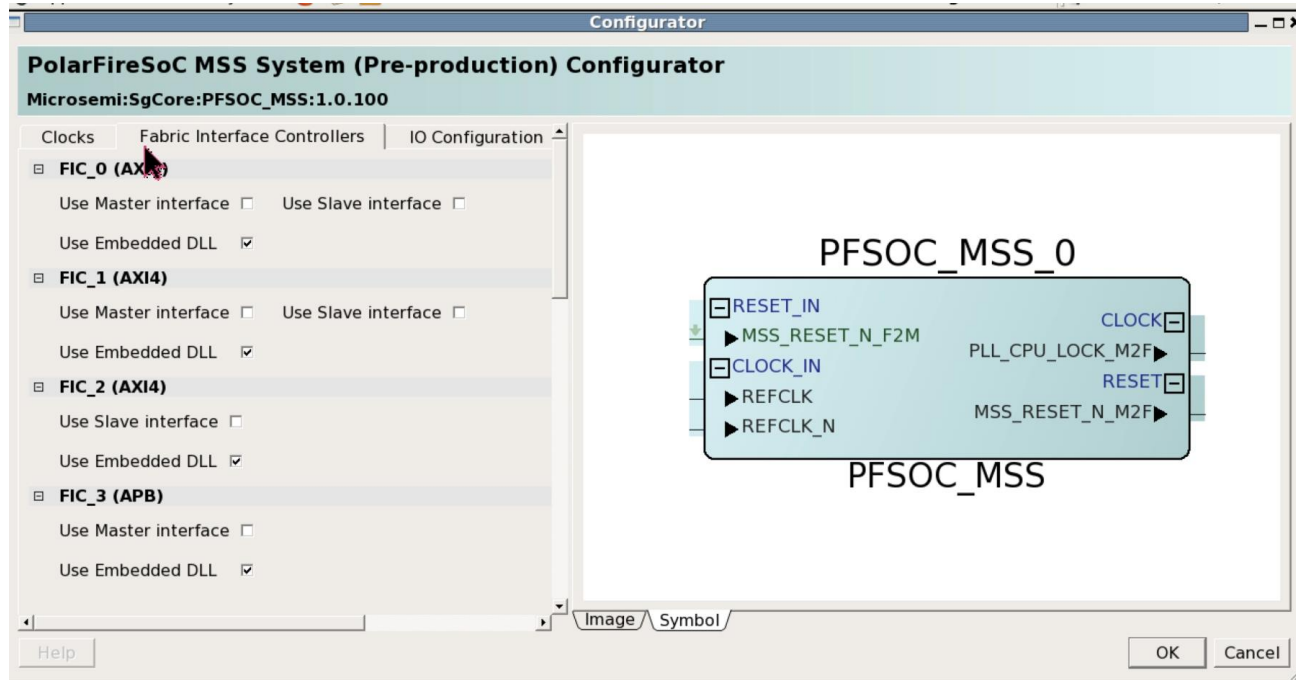
- Master
- Slave

FIC 2 AXI4

- Slave

FIC 3 APB

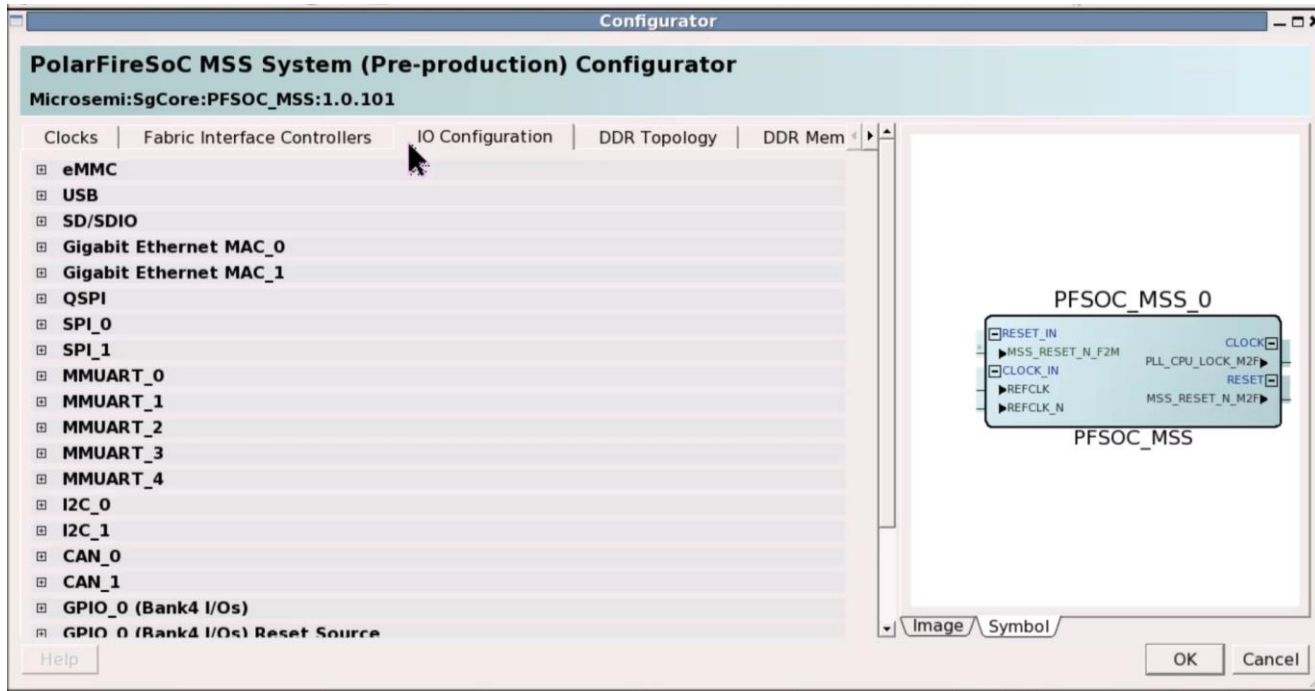
- Master



Getting Started with Libero SoC v12.3

IO Configurations Available:

- eMMC
- USB
- SD/SDIO
- GEM0 / 1
- QSPI
- SPI_0
- SPI_1
- MMUART_0
- MMUART_1
- MMUART_2
- MMUART_3
- MMUART_4
- I2C_0
- I2C_1
- CAN_0
- CAN_1
- GPIO_0 (Bank4 I/Os)
- GPIO_0 (Bank4 I/Os) Reset Source



Getting Started with Libero SoC v12.3

The “Image” tab highlights IOs in use and their configurations

Configurator

PolarFireSoC MSS System (Pre-production) Configurator

Microsemi:PgCore:PF50C_MSS:1.0.100

Clocks | Fabric Interface Controllers | **IO Configuration** | DDR Topology | DDR Memory

IO Configuration

IOs in Use:

- ☒ eMMC
- ☒ USB
- ☒ SD/SDIO
- ☒ Gigabit Ethernet MAC_0
- ☒ Gigabit Ethernet MAC_1
- ☒ QSPI
- ☒ SPI_0
- ☒ SPI_1
- ☒ MMUART_0
- ☒ MMUART_1
- ☒ MMUART_2
- ☒ MMUART_3
- ☒ MMUART_4
- ☒ I2C_0
- ☒ I2C_1
- ☒ CAN_0
- ☒ CAN_1
- ☒ GPIO_0 (Bank4 I/Os)
- ☒ GPIO_0 (Bank4 I/Os) Reset Source
- ☒ GPIO_1 (Bank2 I/Os)
- ☒ GPIO_1 (Bank2 I/Os) Reset Source
- ☒ GPIO_2 (Fabric)
- ☒ GPIO_2 (Fabric) Reset Source

| BANK | IO MUX | Package Pin | eMMC | USB | SD | MAC | QSPI | SPI | MMUART | I2C | CAN | GPIO |
|--------|--------|-------------|------------|-----------------|-----------------|---------------|---------------|-----------------|-----------------|-------------------|-------------------|-------------|
| BANK 0 | 0 | AAR | EMMC_CLK | | SD_CLK | | QSPI_CLK | SPI_0_CLK | MMUART_3_RXD | I2C_0_SCL | | GPIO_0_0 |
| | 1 | AA0 | EMMC_CMD | | SD_CMD | | | | MMUART_3_TXD | | | GPIO_0_1 |
| | 2 | AA7 | EMMC_DATA0 | | SD_DATA0 | | | | | I2C_0_SDA | | GPIO_0_2 |
| | 3 | V6 | EMMC_DATA1 | | SD_DATA1 | | | | MMUART_4_RXD | | CAN_0_TXBUS | GPIO_0_3 |
| | 4 | AA10 | EMMC_DATA2 | | SD_DATA2 | | | | MMUART_4_TXD | | CAN_0_RXBUS | GPIO_0_4 |
| | 5 | AA13 | EMMC_DATA3 | | SD_DATA3 | | | | MMUART_0_RXD(A) | | CAN_0_TX_EBL_N | GPIO_0_5 |
| | 6 | V10 | EMMC_STB0 | | SD_CD | | | | MMUART_0_TXD(A) | | | GPIO_0_6 |
| | 7 | V7 | EMMC_RSTN | | SD_WP | MAC_1_MDC | | | MMUART_2_RXD | I2C_1_SCL | | GPIO_0_7 |
| | 8 | V14 | EMMC_DATA4 | | SD_P0W | MAC_1_MDIO | QSPI_SS0 | | MMUART_2_TXD | I2C_1_SDA | | GPIO_0_8 |
| | 9 | V13 | EMMC_DATA5 | | SD_VOLT_SEL | MAC_0_MDC | QSPI_DATA0 | | MMUART_0_RXD(B) | | | GPIO_0_9 |
| | 10 | V8 | EMMC_DATA6 | | SD_VOLT_EN | MAC_0_MDIO | QSPI_DATA1 | | MMUART_0_TXD(B) | | | GPIO_0_10 |
| | 11 | V11 | EMMC_DATA7 | | SD_VOLT_CMD_DIR | | QSPI_DATA2 | SPI_0_DO | MMUART_1_RXD | | CAN_1_TXBUS | GPIO_0_11 |
| | BANK 1 | 12 | AA12 | | SD_VOLT_DIR_0 | | QSPI_DATA3 | SPI_0_DI | MMUART_1_TXD | | | CAN_1_RXBUS |
| 13 | | V12 | | SD_VOLT_DIR_1_3 | | | SPI_0_SS0 | | | | CAN_1_TX_EBL_N | GPIO_0_13 |
| 14 | | W6 | | USB_CLK | | | QSPI_CLK(A) | SPI_1_CLK(A) | | | | GPIO_1_0 |
| 15 | | V6 | | USB_DIR | | MAC_1_MDC(A) | SPI_1_DO(A) | MMUART_4_RXD | | | | GPIO_1_1 |
| 16 | | W8 | | USB_NXT | | MAC_1_MDIO(A) | SPI_1_DI(A) | MMUART_4_TXD | | | | GPIO_1_2 |
| 17 | | V8 | | USB_STP | | | SPI_1_SS0(A) | MMUART_0_RXD(A) | | | | GPIO_1_3 |
| 18 | | V4 | | USB_DATA0 | | | | MMUART_0_TXD(A) | | | | GPIO_1_4 |
| 19 | | U5 | | USB_DATA1 | | | | MMUART_1_TXD | I2C_0_SCL(A) | | | GPIO_1_5 |
| 20 | | W9 | | USB_DATA2 | | | | MMUART_2_RXD | I2C_0_SDA(A) | CAN_0_TX_EBL_N(A) | | GPIO_1_6 |
| 21 | | U7 | | USB_DATA3 | | | | MMUART_2_TXD | | | CAN_0_TXBUS(A) | GPIO_1_7 |
| 22 | | U6 | | USB_DATA4 | | | | MMUART_3_RXD | I2C_1_SCL(A) | | CAN_0_RXBUS(A) | GPIO_1_8 |
| 23 | | V7 | | USB_DATA5 | | MAC_0_MDC(A) | SPI_0_DI | MMUART_3_TXD | I2C_1_SDA(A) | | | GPIO_1_9 |
| BANK 2 | | 24 | V9 | | USB_DATA6 | | MAC_0_MDIO(A) | SPI_0_DO | | I2C_1_SCL(B) | | |
| | 25 | U9 | | USB_DATA7 | | | | | I2C_1_SDA(B) | | | GPIO_1_11 |
| | 26 | V14 | | SD_LED(A) | | | | | I2C_1_SCL(B) | | | GPIO_1_12 |
| | 27 | V13 | | SD_VOLT_0(A) | | | | | I2C_1_SDA(B) | CAN_1_TX_EBL_N(A) | | GPIO_1_13 |
| | 28 | W10 | | SD_VOLT_1(A) | MAC_1_MDC(B) | | | | MMUART_0_RXD(B) | | CAN_1_TXBUS(A) | GPIO_1_14 |
| | 29 | W11 | | SD_VOLT_2(A) | MAC_1_MDIO(B) | | | | MMUART_0_TXD(B) | | CAN_1_RXBUS(A) | GPIO_1_15 |
| | 30 | W14 | | | | | QSPI_CLK(B) | SPI_1_CLK(B) | | | | GPIO_1_16 |
| | 31 | W13 | | | | | QSPI_SS0 | SPI_1_SS0(B) | | | CAN_0_TXBUS(B) | GPIO_1_17 |
| | 32 | U11 | | SD_CLE | | | QSPI_DATA0 | SPI_1_DO(B) | | | CAN_0_RXBUS(B) | GPIO_1_18 |
| | 33 | U12 | | SD_LED(B) | | | QSPI_DATA1 | SPI_1_DI(B) | | | CAN_0_TX_EBL_N(B) | GPIO_1_19 |
| | 34 | V11 | | SD_VOLT_0(B) | | | QSPI_DATA2 | | | | CAN_1_TXBUS(B) | GPIO_1_20 |
| | 35 | U10 | | SD_VOLT_1(B) | MAC_0_MDC(B) | | QSPI_DATA3 | | MMUART_0_RXD(C) | I2C_0_SCL(B) | CAN_1_RXBUS(B) | GPIO_1_21 |
| | 36 | U14 | | SD_VOLT_2(B) | MAC_0_MDIO(B) | | | SPI_0_CLK | MMUART_0_TXD(C) | I2C_0_SDA(B) | CAN_1_TX_EBL_N(B) | GPIO_1_22 |
| 37 | V12 | | | | | QSPI_CLK(C) | | | | | GPIO_1_23 | |

Image / Symbol

Help

OK Cancel

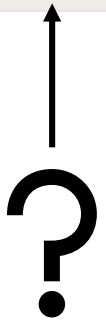


Getting Started with Libero SoC v12.3

PolarFireSoC MSS System (Pre-production) Configurator

Microsemi:SgCore:PFSOC_MSS:1.0.100

Clocks | Fabric Interface Controllers | IO Configuration | DDR Topology | DDR Memory Initialization | DDR Memory Timing | DDR Controller | Misc |



Getting Started with Libero SoC v12.3

Debug Trace:

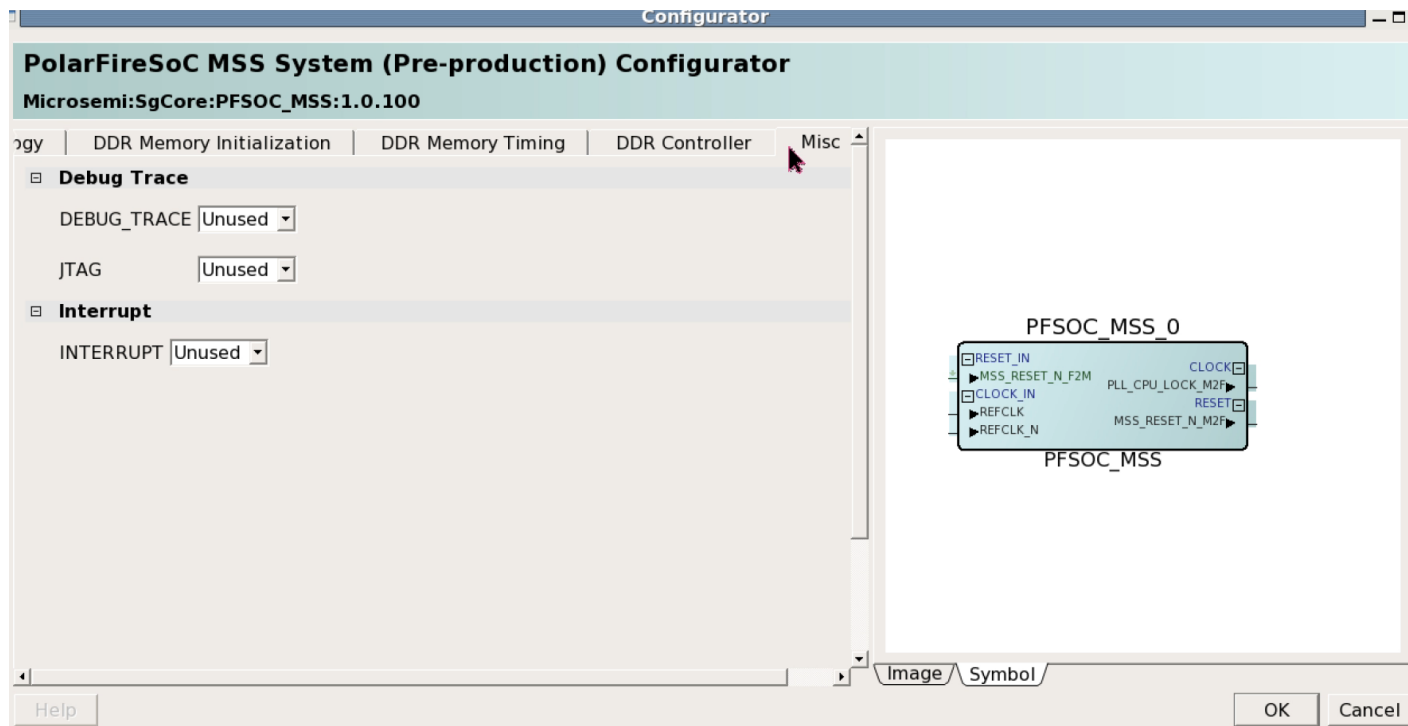
Expose UltraSoC
Debug pins to the
fabric

JTAG:

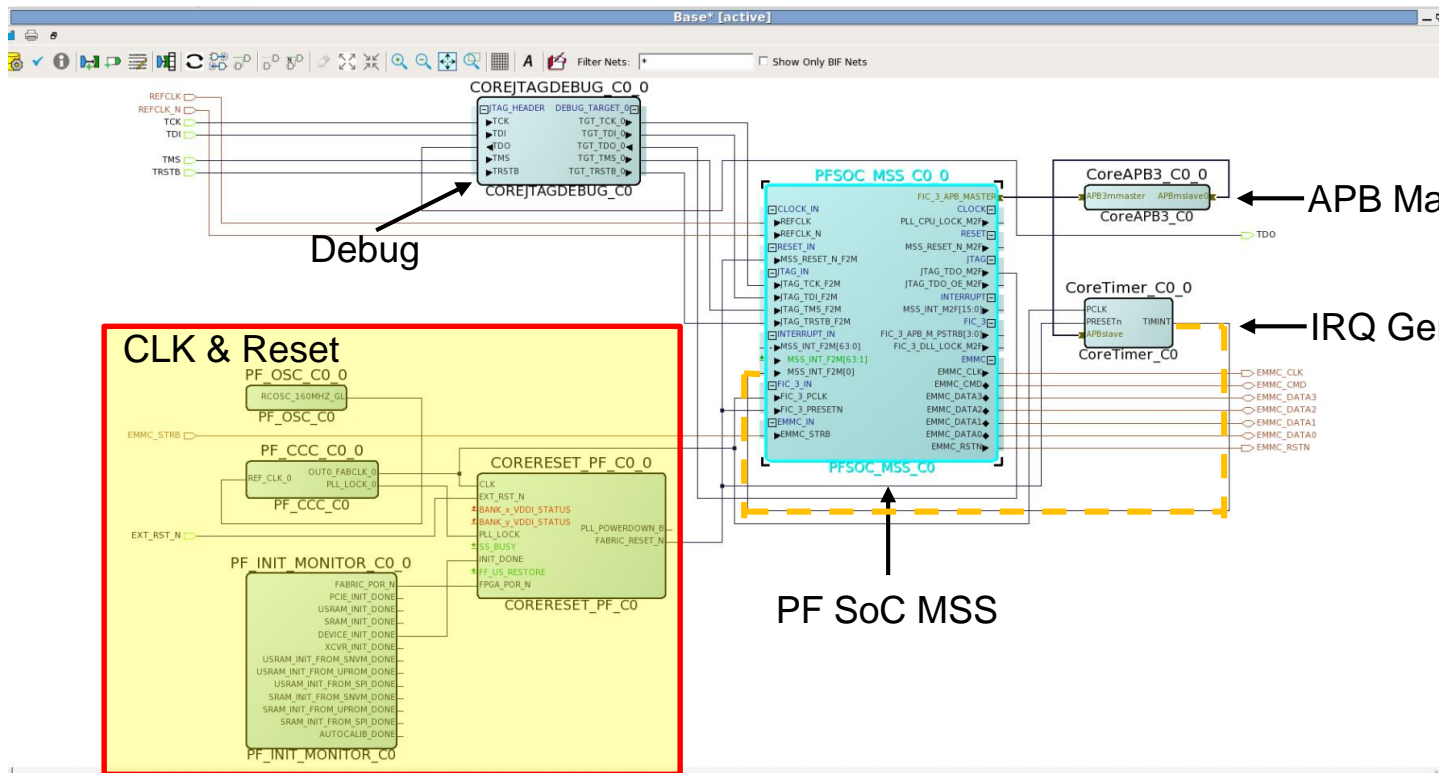
Expose fabric JTAG
debug pins

Interrupt:

Expose 64 interrupt
pins to the fabric



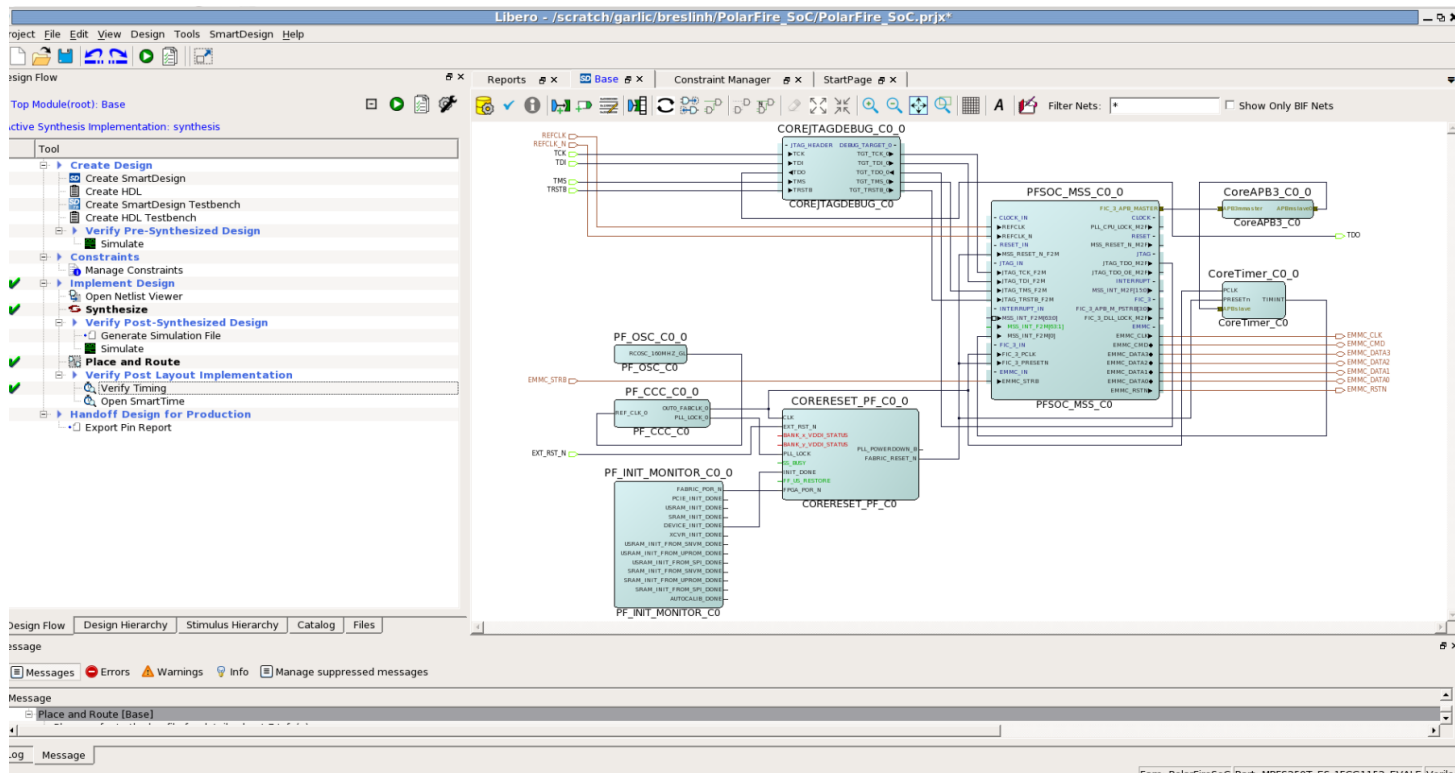
Getting Started with Libero SoC v12.3



Getting Started with Libero SoC v12.3

Currently Available:

- Synthesis
- Place and Route
- Timing Verification





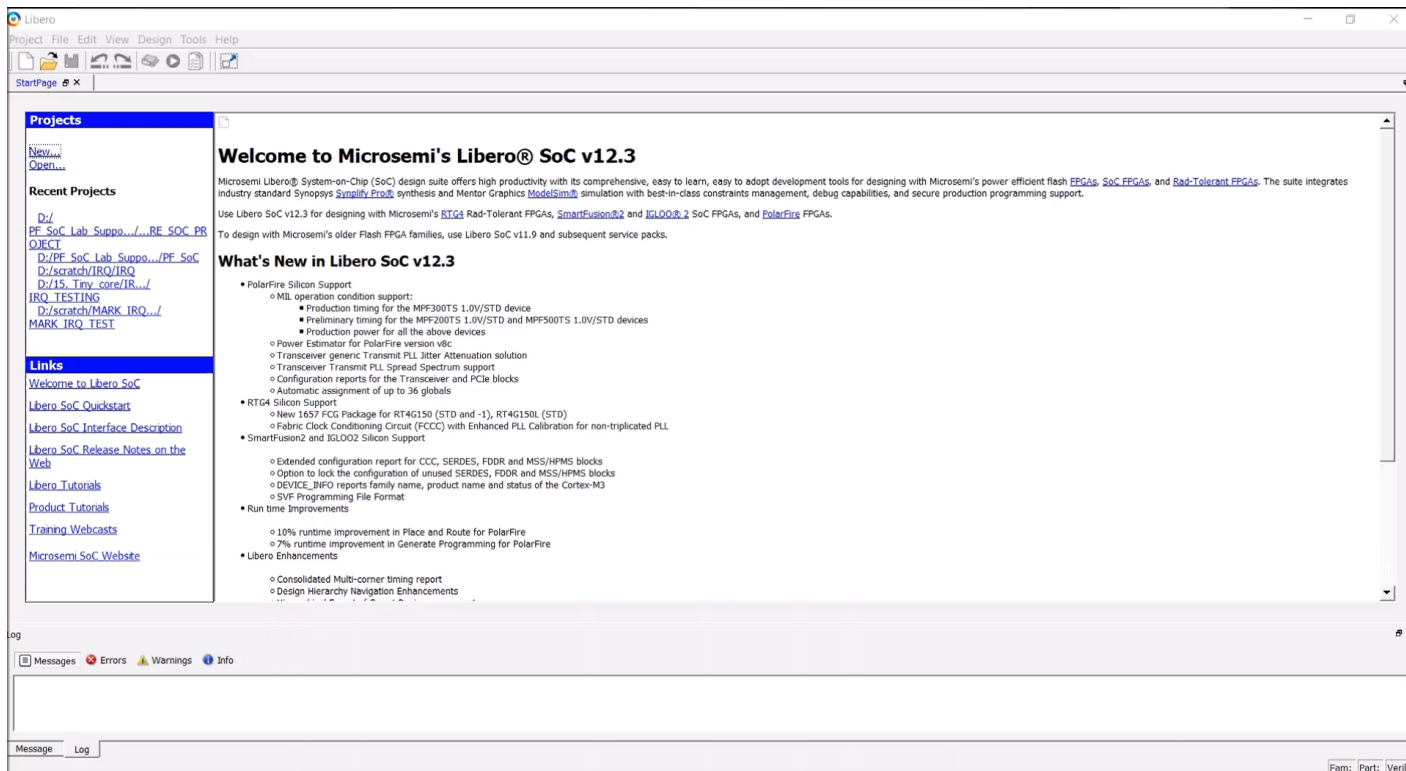
Creating a PolarFire SoC Design in Libero SoC v12.3



Creating a PolarFire SoC Design in Libero SoC v12.3

- **Create the Project**
- **Configure the MSS**
- **Configure Fabric Clock and Reset**
- **Add Debug**
- **Add an Interrupt Generating Timer**

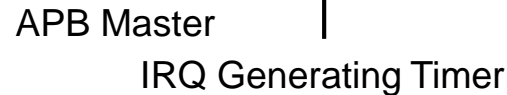
Creating a PolarFire SoC Design in Libero SoC v12.3





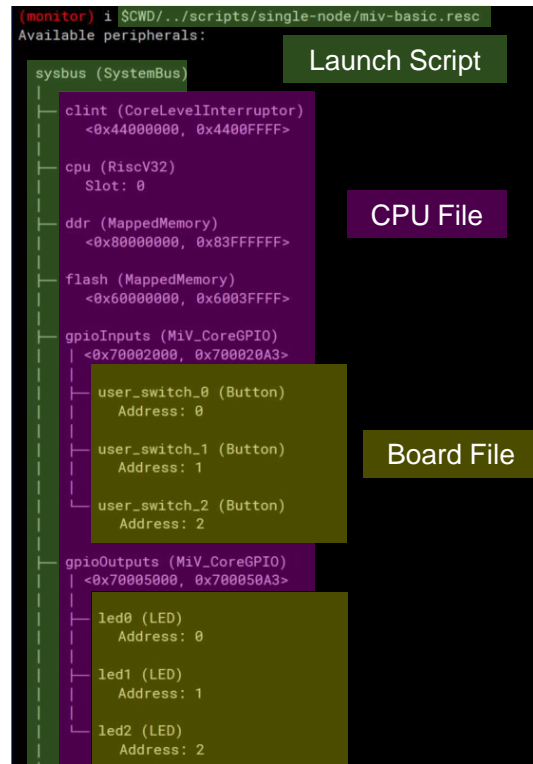
Modifying the Renode Model and MPFS Blinky





Modifying the Renode Model and MPFS Blinky

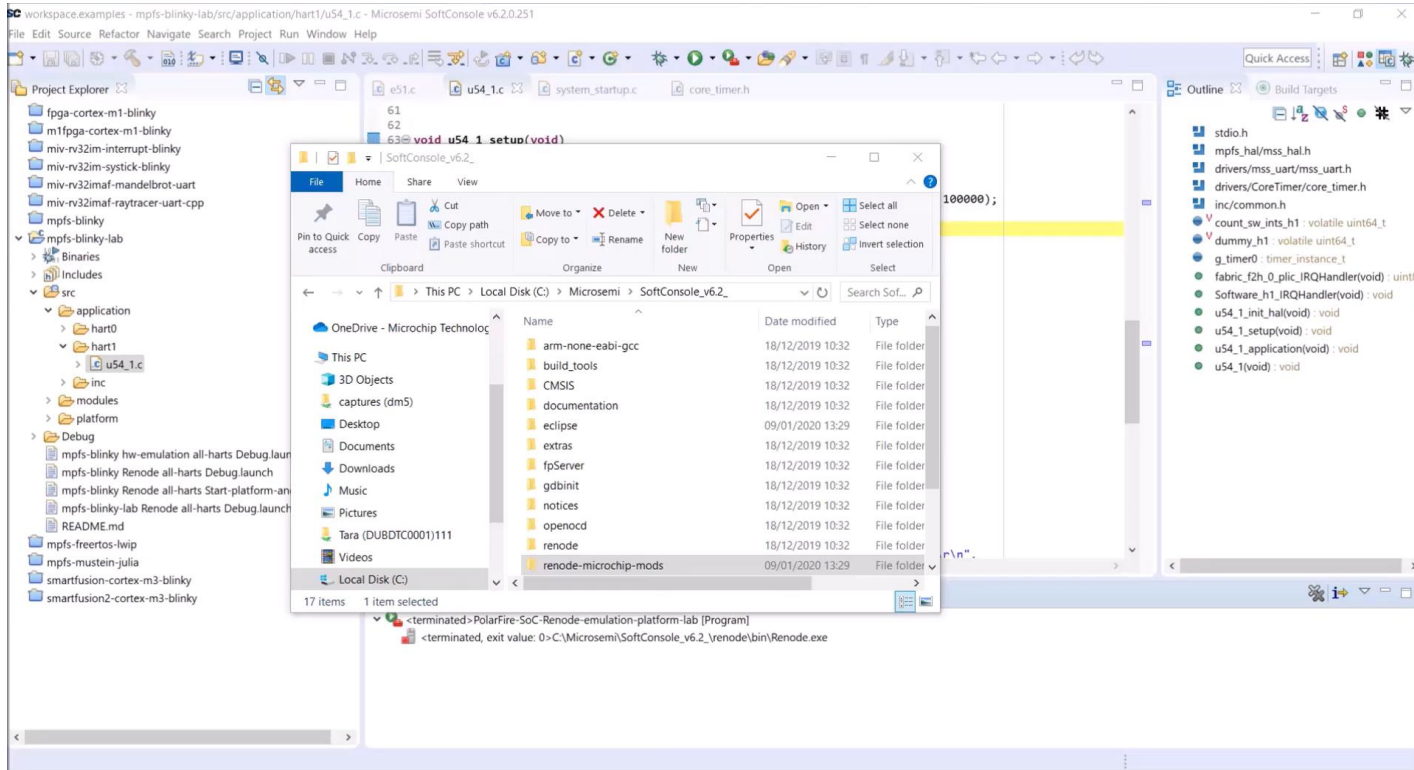
- The timer needs to be added to the CPU file
- It connects to sysbus directly – there is no need for an apb master
- The FIC3 address is 0x40_0000_0000
- The timer interrupt needs to be connected to the fabric interrupts



Modifying the Renode Model and MPFS Blinky

- **Drivers for the timer need to be added to the software project**
- **The timer needs to be configured and started**
- **The handler for the external interrupt to be used needs to be added to the software**

Modifying the Renode Model and MPFS Blinky



Agenda

- **Getting Started with Libero SoC v12.3**
- **Creating a PolarFire SoC Design in Libero SoC v12.3**
- **Modifying the Renode Model and MPFS Blinky**



Thank You

Any Questions?
