



Total Ionizing Dose Test Report

No. 18T-RTAX4000S-CQ352-DC2WR1

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I. Summary Table

The TID tolerance for each tested parameter is summarized below in Table 1. The overall tolerance is limited by the standby power-supply current (ICC). The room temperature annealing allowed by 1019.8 to anneal down ICC is performed for approximately 7 days. Every DUT passes the major specifications listed in the table for 300 krad (SiO₂) of irradiation.

Table 1 Tolerances for Each Tested Parameter

Parameter	Tolerance
1. Gross Functionality	Passed 300 krad (SiO ₂)
2. Power Supply Current (ICCA/ICCI)	Passed 300 krad (SiO ₂)
3. Input Threshold (VIL/VIH)	Passed 300 krad (SiO ₂)
4. Output Drive (VOL/VOH)	Passed 300 krad (SiO ₂)
5. Propagation Delay	Passed 300 krad (SiO ₂) for 10% degradation criterion
6. Transition Time	Passed 300 krad (SiO ₂)

II. Total Ionizing Dose (TID) Testing

This testing is designed on the basis of an extensive database (see, for example, TID data of antifuse-based FPGAs at <http://www.klabs.org> and <http://www.microsemi.com/soc>) accumulated from the TID testing of many generations of antifuse-based FPGAs.

A. Device-Under-Test (DUT) and Irradiation Parameters

Table 2 lists the DUT and irradiation parameters. During irradiation all inputs are grounded except for the inputs Burnin, oe_EAQ, enable_HSB and the utilized clocks (Rclock1-3 and Hclock1-4). The inputs Burnin, oe_EAQ and enable_HSB are set high to 3.3 V and a 1 KHz clock is provided to all clocks in order for the design to remain stable during irradiation. During anneal each input and output is tied to ground or VCCI through a 4.7 kΩ resistor. Appendix A contains the schematics of irradiation-bias circuits.

Table 2 DUT and Irradiation Parameters

Part Number	RTAX4000S
Package	CQFP352
Foundry	United Microelectronics Corp.
Technology	0.15 μm CMOS
DUT Design	MASTER_RTAX4000S_DESIGN_80_SP1
Die Lot Number	DC2WR1
Quantity Tested	6
Serial Number	300 krad: 12528, 12529 200 krad: 12526, 12527 100 krad: 12503, 12508
Radiation Facility	Defense Microelectronics Activity
Radiation Source	Co-60
Dose Rate (±5%)	10 krad (SiO ₂)/min
Irradiation Temperature	Room
Irradiation and Measurement Bias (VCCI/VCCA)	Static at 3.3 V / 1.5 V
I/O Configuration	Single ended: LVTTTL Differential pair: LVPECL

B. Test Method

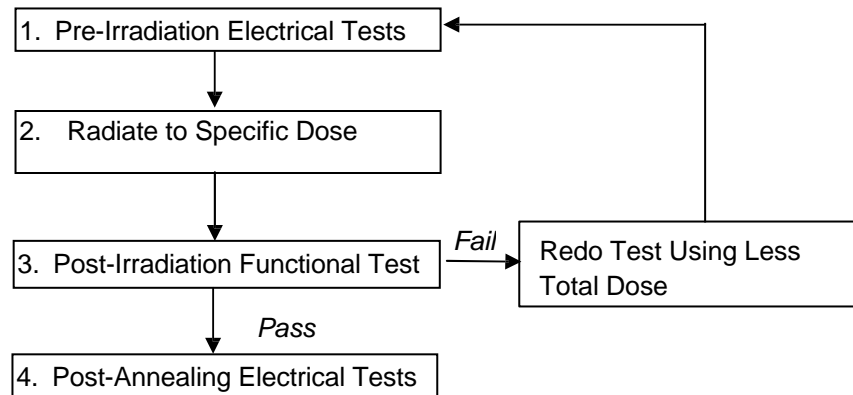


Figure 1 Parametric Test Flow Chart

The test method generally follows the guidelines in the military standard TM1019.8. Figure 1 is the flow chart showing the steps for parametric tests, irradiation, and post-irradiation annealing.

The accelerated aging, or rebound test mentioned in TM1019.8, is unnecessary because there is no adverse time-dependent effect (TDE) in Microsemi SoC Products Group products manufactured by sub-micron CMOS technology. Elevated temperature annealing actually reduces the effects originated from radiation-induced leakages. As indicated by testing data in the following sections, the predominant radiation effects in RTAX4000S are due to radiation-induced leakages.

Room temperature annealing is performed in this test; the duration is approximately 7 days.

C. Design and Parametric Measurements

The DUT uses a high utilization generic design (RTAX4000S_CQ352_MASTER) to evaluate total dose effects for typical space applications. The schematics of this design are documented in Appendix B.

The functionality is measured at 1 MHz and 50 MHz using the minimum and maximum power specifications shown in Table 3.

Table 3 Minimum and Maximum Power Specifications for RTAX-D Devices

Supply Voltage	Minimum	Recommended	Maximum
1.5 V Core	1.4 V	1.5 V	1.6 V
3.3 V I/O	3.0 V	3.3 V	3.6 V
3.3 V VCCDA I/O	3.0 V	3.3 V	3.6 V

The functionality test design is subdivided into two blocks, the EAQ (Enhanced Antifuse Qualification) and the QBI (Qualification Burn-In). The EAQ block includes three 1458-bit shift registers and tests the I/Os (1560 I/O registers and 520 I/Os) and RAM (1x16384 RAM). The QBI block tests all offered macros and I/O standards. The results from the functional tests are obtained from the following outputs: IO_Monitor_EAQ, RAM_Monitor_EAQ, Array_Monitor_EAQ, Global_Monitor_EAQ, C_test_mon_QBI, ALU_test_mon_QBI, Global_mon_QBI_TP, and Global_mon_QBI_BI. Details on the Functionality Test are shown in Appendix B.

ICC is measured on the power supply of the logic-array (ICCA) and I/O (ICCI) respectively. The input logic threshold (VIL/VIH) is tested on single-ended inputs Shiftin1, Shiftin2, Shiftin3, Shiftin4, Shiftin5, Shiftin7, Shiftin8, zoom_sel_n_1, zoom_sel_n_0, zoom, TOG_n, SEU_sel, Set_n, Resetn, oe_EAQ, enable_HSB, test_done_sel_2, IO_Pattern_Length_2, IO_Pattern_Length_1, IO_Pattern_Length_0, IO_Johnson, A_Johnson, A_Pattern_Length_1, and A_Pattern_Length_0. The output-drive voltage (VOL/VOH) is measured on single-ended outputs Array_out_EAQ_0, Array_out_EAQ_1, Array_out_EAQ_2, Global_Monitor_EAQ, Shiftout3, Shiftout7, Shiftout8, RAM_Monitor_EAQ, RAM_out_EAQ_0, RAM_out_EAQ_4, RAM_out_EAQ_8.

The propagation delays are measured on the outputs of five delay strings; each one comprises of 1,170 NAND4-inverters. There are 6 delay measurements: one measurement for each delay string and a total delay measurement obtained from cascading all the delay strings. The propagation delay is defined as the time delay from the triggering edge at the HClock1 input to the switching edge at the output. The delay measurements are taken for both rising and falling edges, the average reading of the two measurements is reported. The transition characteristics, measured on the output delay_out_SEU4, are shown as oscilloscope captures.

Table 4 lists measured electrical parameters and the corresponding logic design.

Table 4 Logic Design for Parametric Measurements

Parameters	Logic Design
1. Functionality	IO_Monitor_EAQ, RAM_Monitor_EAQ, Array_Monitor_EAQ, Global_Monitor_EAQ, C_test_mon_QBI, ALU_test_mon_QBI, Global_mon_QBI_TP, and Global_mon_QBI_BI
2. ICC (ICCA/ICCI)	DUT power supply
3. Input Threshold (VIL/VIH)	Single ended inputs (Shiftin1, Shiftin2, Shiftin3, Shiftin4, Shiftin5, Shiftin7, Shiftin8, zoom_sel_n_1, zoom_sel_n_0, zoom, TOG_n, SEU_sel, Set_n, Resetn, oe_EAQ, enable_HSB, test_done_sel_2, IO_Pattern_Length_2, IO_Pattern_Length_1, IO_Pattern_Length_0, IO_Johnson, A_Johnson, A_Pattern_Length_1, A_Pattern_Length_0)
4. Output Drive (VOL/VOH)	Single-ended outputs (Array_out_EAQ_0, Array_out_EAQ_1, Array_out_EAQ_2, Global_Monitor_EAQ, Shiftout3, Shiftout7, Shiftout8, RAM_Monitor_EAQ, RAM_out_EAQ_0, RAM_out_EAQ_4, RAM_out_EAQ_8)
5. Propagation Delay	String of NAND4-inverters. Measured from output delay_out_SEU4
6. Transition Characteristic	NAND4-inverter output (delay_out_SEU4)

III. Test Results

The test results mainly compare the electrical parameter measured pre-irradiation with the same parameter measured post-irradiation-and-annealing, or post-annealing.

A. Functionality

Every DUT passed the pre-irradiation and post-annealing functional tests.

B. Power Supply Current (ICCA and ICCI)

The logic-array power supply (VCCA) is 1.5 V, and the IO power supply (VCCI) is 3.3 V. Their standby currents, ICCA and ICCI, are monitored influx. Figure 2-7 show the influx ICCA and ICCI versus total dose for the DUTs.

Referring to TM1019.8 subsection 3.11.2.c, the post-irradiation-parametric limit (PIPL) for the post-annealing ICC, should be defined as the addition of highest ICCI, ICCDA, and ICCDIFFA values in Table 2-4 of the *RTAX-S/SL and RTAX-DSP Radiation-Tolerant FPGAs datasheet* posted on the Microsemi SoC Products Group website:

http://www.microsemi.com/soc/documents/RTAXS_DS.pdf

Therefore, the PIPL for ICCA is 600 mA, and the PIPL for ICCI is 60 mA.

Table 5 summarizes the pre-irradiation, post-irradiation right after irradiation and before anneal, and post-annealing ICCA and ICCI data.

Table 5 Pre-irradiation, Post Irradiation and Post-Annealing ICC

DUT	Total Dose	ICCA (mA)			ICCI (mA)		
		Pre-Irrad.	Post-Irrad.	Post-Ann.	Pre-Irrad.	Post-Irrad.	Post-Ann.
12503	100 krad	9.6	9.7	9.7	9.8	9.6	11.7
12508	100 krad	4.3	4.4	4.0	9.2	11.6	16.1
12526	200 krad	3.6	11.6	3.5	8.6	149	32.0
12527	200 krad	3.7	8.2	3.2	8.4	130	33.0
12528	300 krad	6.3	214	33.7	8.6	118	55.0
12529	300 krad	5.4	140	18.5	8.3	136	56.0

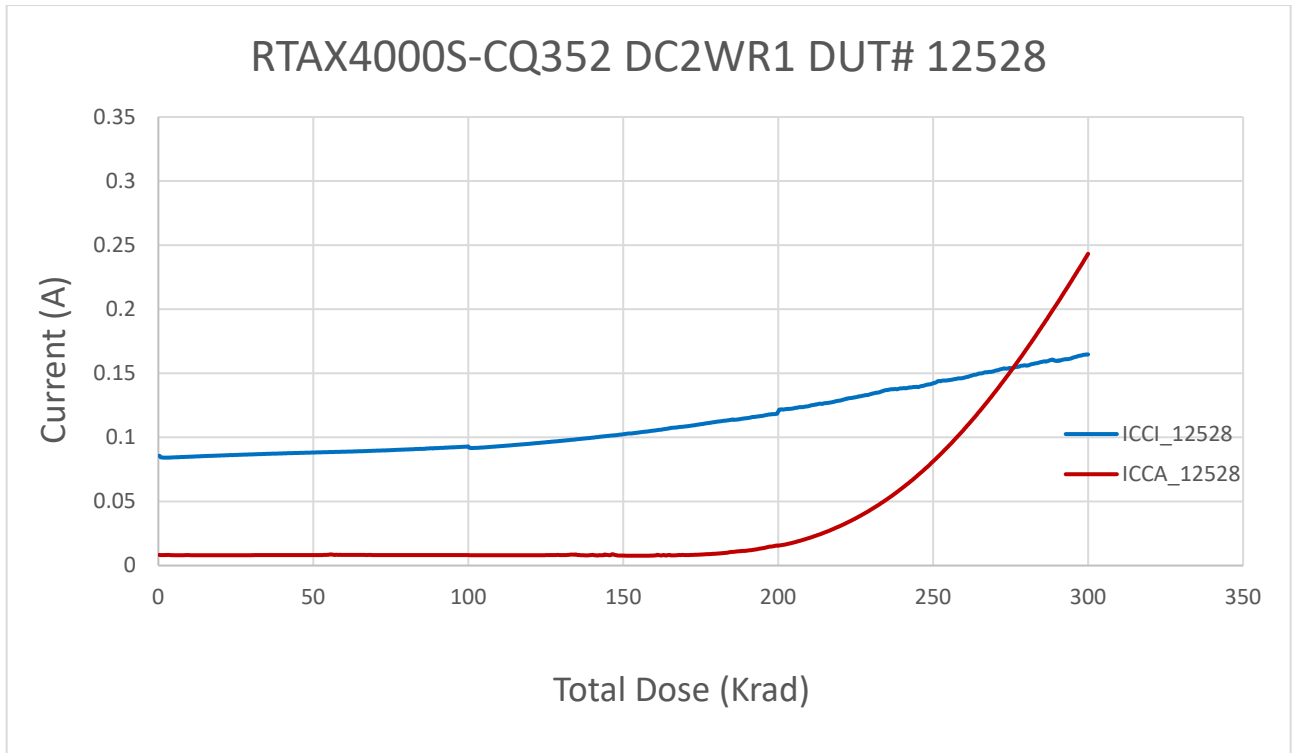


Figure 2 DUT 12528 Influx ICCI and ICCA

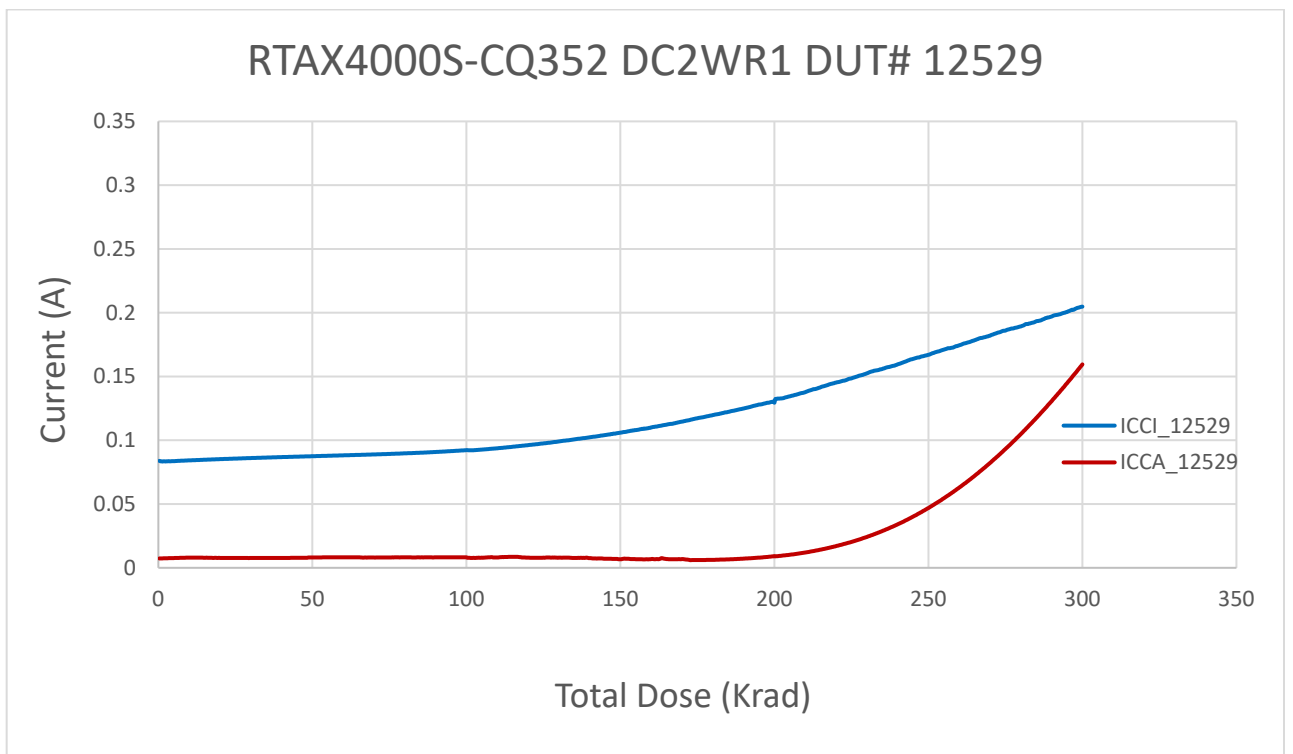


Figure 3 DUT 12529 Influx ICCI and ICCA

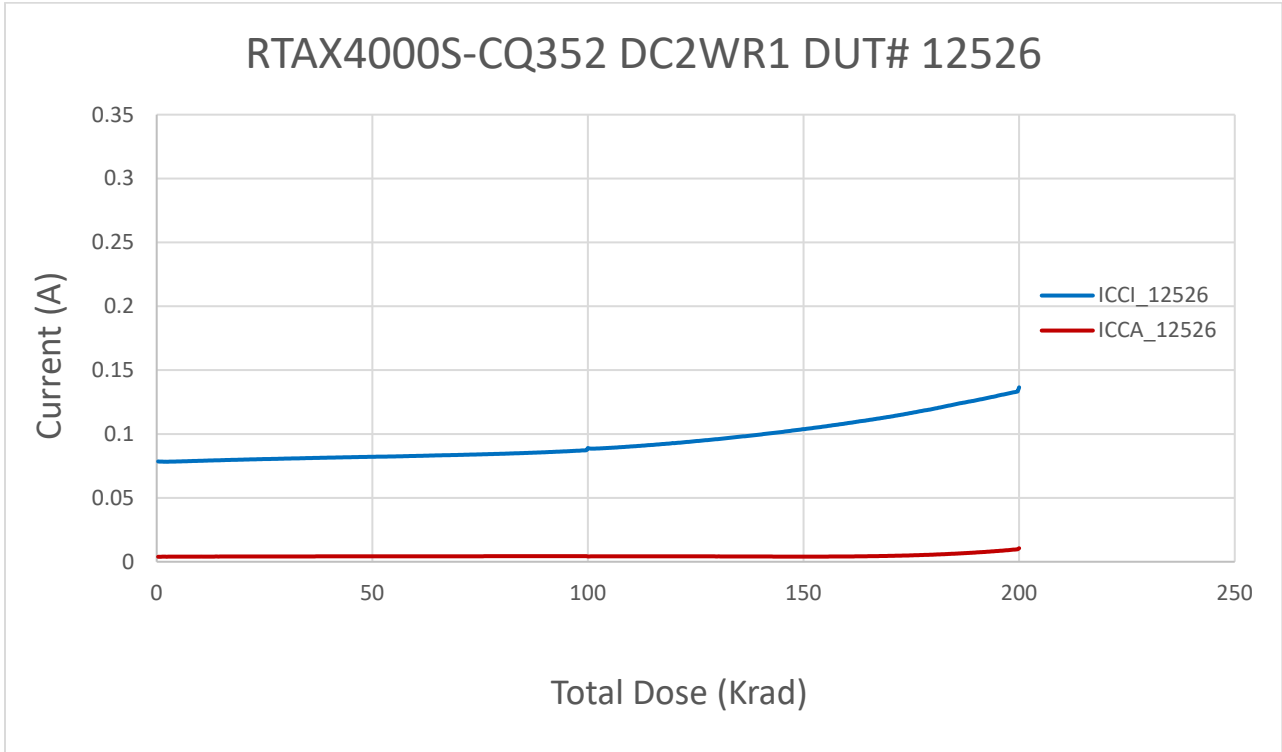


Figure 4 DUT 12526 Influx ICCI and ICCA

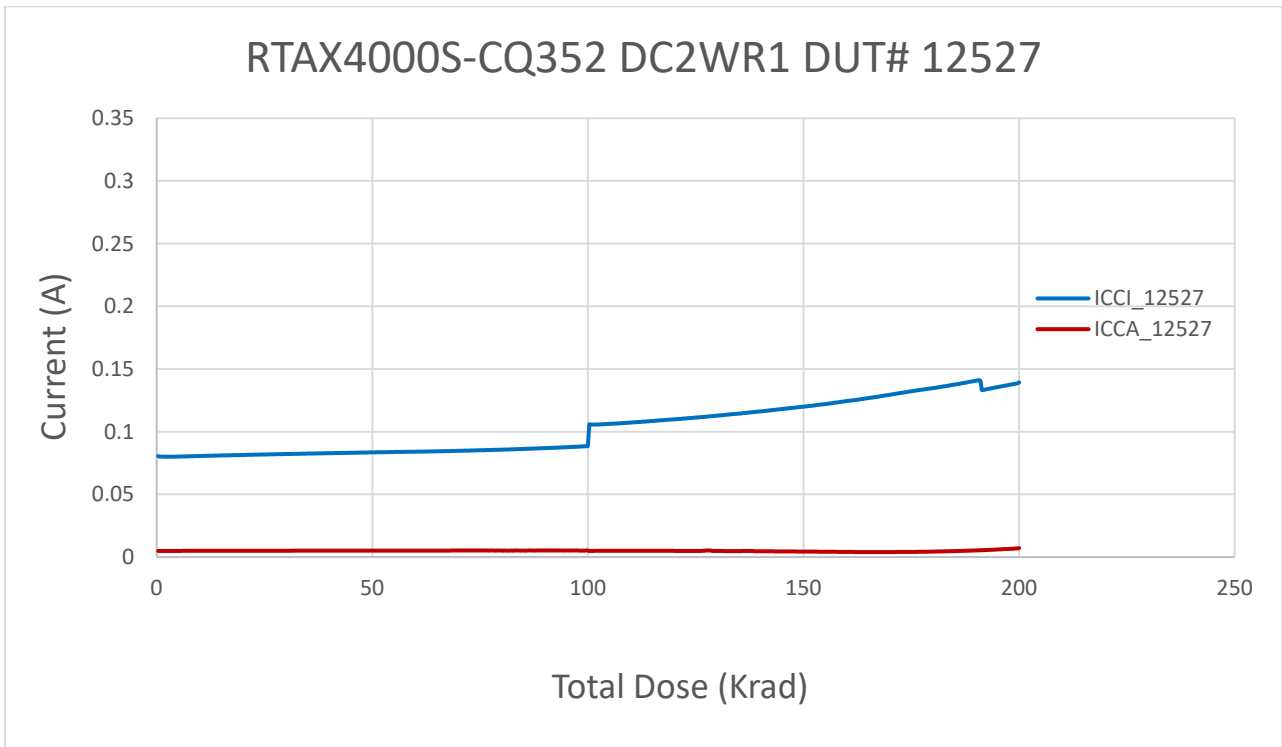


Figure 5 DUT 12527 Influx ICCI and ICCA

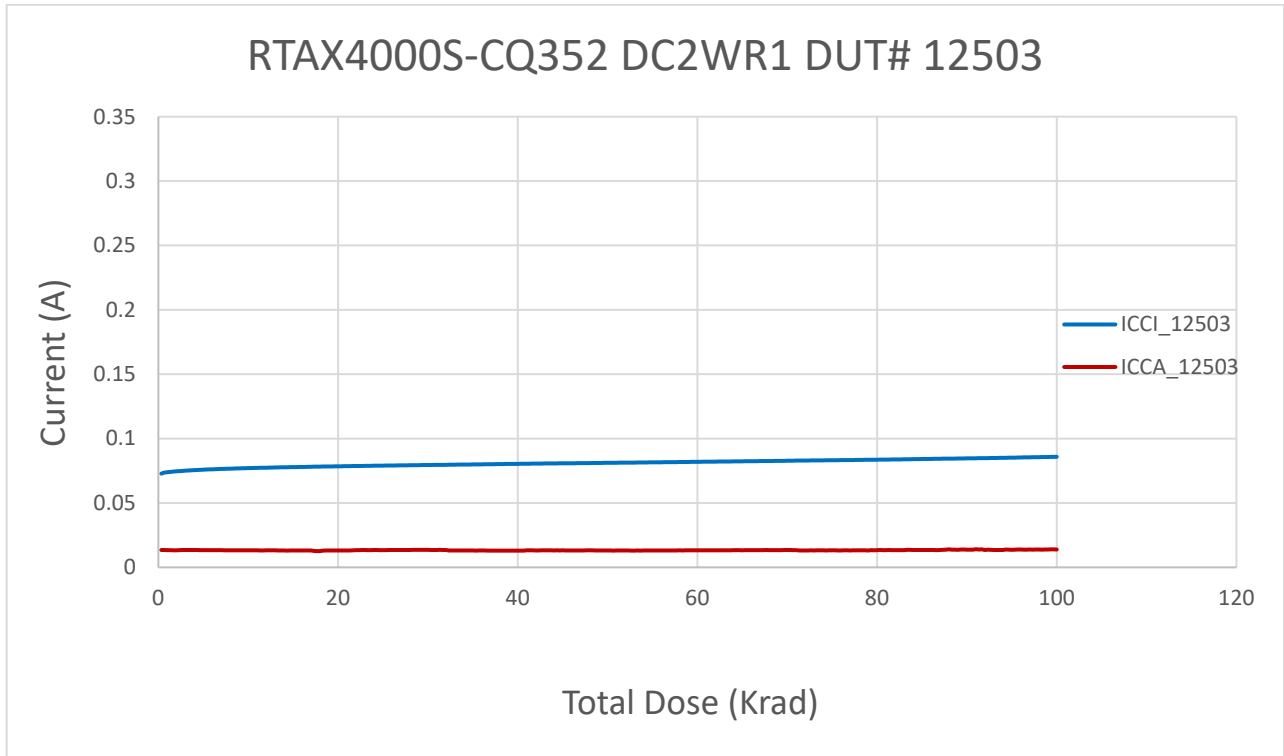


Figure 6 DUT 12503 Influx ICCI and ICCA

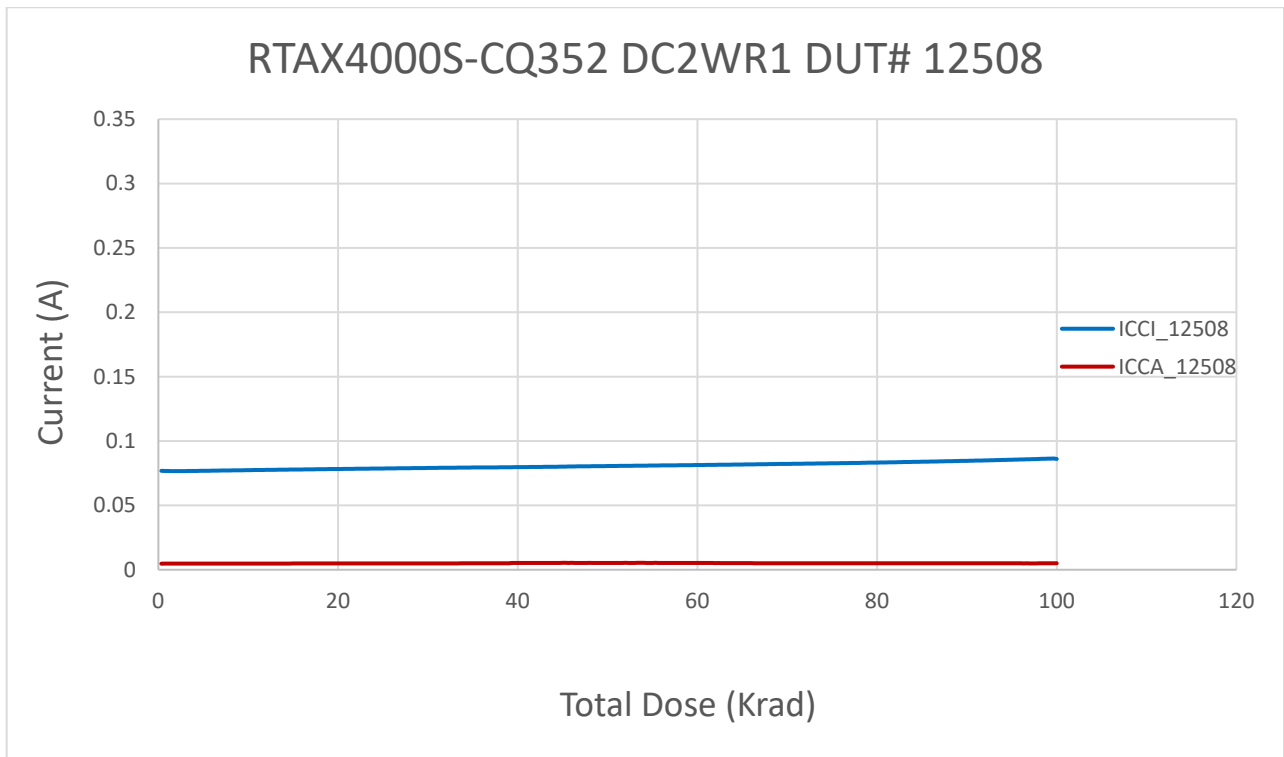


Figure 7 DUT 12508 Influx ICCI and ICCA

C. Single-Ended 3.3 V LVTTTL Input Logic Threshold (VIL/VIH)

The input switching threshold, or trip point, is defined as the applied input voltage at which the output of the design often just input and output buffers starts to switch: VIH is the input trip point when the input is going high to low; VIL is the input trip point when the input is going low to high. The difference between the pre-irradiation and post-annealing data is usually negligibly small. The pre-irradiation and post-annealing single-ended VIL and VIH are tested and recorded as pass or fail. In each case, the pre-irradiation and post-annealing both passed with respect to the specification.

D. Output-Drive Voltage (VOL/VOH)

The pre-irradiation and post-annealing VOL/VOH are listed in Tables 6 and 7. The post-annealing data are within the specification limits; in each case, the radiation-induced degradation is within 10%.

Table 6 Pre-Irradiation and Post-Annealing VOL (mV)

Pin \ DUT(Dose)	12528 (300 krad)		12529 (300 krad)		12526 (200 krad)		12527 (200 krad)		12503 (100 krad)		12508 (100 krad)	
	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an
Array_out_EAQ_0	145.6	147.7	147.4	153.4	148.7	152.3	147.3	166.3	146.9	183.6	148.5	176.5
Array_out_EAQ_1	182.6	174.6	184.2	176.1	185.8	177.5	185.1	178.0	183.3	177.9	184.8	179.8
Array_out_EAQ_2	183.2	172.6	184.0	173.9	185.5	175.5	184.3	175.1	184.4	176.5	185.1	177.8
Global_Monitor_EAQ	175.6	173.6	177.1	174.8	178.7	176.6	178.3	176.1	176.5	176.9	178.5	178.8
Shiftout3	199.8	179.1	199.8	178.8	203.9	182.3	201.3	181.9	199.8	181.6	206.7	185.9
Shiftout7	195.2	186.6	194.6	185.8	197.9	189.3	196.6	188.4	194.1	188.5	199.4	192.3
Shiftout8	193.6	188.5	195.6	188.4	199.4	191.4	196.6	189.8	194.4	190.5	197.8	193.1
RAM_Monitor_EAQ	186.4	188.3	187.4	189.3	189.0	190.5	188.4	191.9	186.5	197.0	188.6	197.0
RAM_out_EAQ_0	200.9	177.0	202.0	177.7	204.5	179.7	201.9	179.4	200.2	178.7	204.4	180.9
RAM_out_EAQ_4	148.0	140.5	148.2	140.5	152.6	144.3	149.8	144.4	148.2	142.9	152.3	146.3
RAM_out_EAQ_8	187.1	193.7	188.4	194.8	189.8	196.4	188.0	199.4	187.5	220.5	190.1	224.0

Table 7 Pre-Irradiation and Post-Annealing VOH (V)

Pin \ DUT(Dose)	12528 (300 krad)		12529 (300 krad)		12526 (200 krad)		12527 (200 krad)		12503 (100 krad)		12508 (100 krad)	
	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an
Array_out_EAQ_0	2.764	2.750	2.763	2.748	2.763	2.751	2.762	2.732	2.762	2.726	2.762	2.737
Array_out_EAQ_1	2.726	2.723	2.725	2.722	2.725	2.724	2.723	2.722	2.725	2.725	2.724	2.724
Array_out_EAQ_2	2.726	2.725	2.725	2.723	2.726	2.727	2.725	2.725	2.724	2.726	2.724	2.727
Global_Monitor_EAQ	2.733	2.724	2.732	2.723	2.730	2.726	2.730	2.723	2.731	2.726	2.730	2.725
Shiftout3	2.705	2.716	2.705	2.719	2.704	2.719	2.704	2.718	2.706	2.722	2.701	2.719
Shiftout7	2.709	2.709	2.710	2.712	2.709	2.712	2.709	2.711	2.711	2.714	2.708	2.712
Shiftout8	2.706	2.705	2.709	2.707	2.706	2.707	2.707	2.707	2.708	2.710	2.708	2.710
RAM_Monitor_EAQ	2.722	2.710	2.721	2.709	2.720	2.711	2.720	2.708	2.721	2.708	2.720	2.708
RAM_out_EAQ_0	2.706	2.719	2.706	2.718	2.706	2.722	2.706	2.722	2.708	2.725	2.706	2.724
RAM_out_EAQ_4	2.764	2.764	2.765	2.766	2.762	2.765	2.763	2.766	2.765	2.769	2.762	2.767
RAM_out_EAQ_8	2.722	2.705	2.722	2.704	2.721	2.706	2.720	2.701	2.721	2.695	2.719	2.697

E. Propagation Delay

Table 8 lists the pre-irradiation and post-annealing propagation delays. The results show small radiation effects; in any case, the percentage change is well below 10%.

Table 8 Radiation-Induced Propagation Delay Degradations

Delay (μ s)							
	DUT	Total Dose	Pre-rad	100 krad	200 krad	300 krad	Post-ann
	12503	100 krad	6.55	6.53	-	-	6.50
	12508	100 krad	6.81	6.80	-	-	6.75
	12526	200 krad	6.67	6.66	6.78	-	6.59
	12527	200 krad	6.99	6.96	7.07	-	6.89
	12528	300 krad	6.69	6.68	6.75	7.61	6.70
	12529	300 krad	6.97	6.96	7.06	7.60	6.93
Radiation Δ (%)							
	DUT	Total Dose	Pre-rad	100 krad	200 krad	300 krad	Post-ann
	12503	100 krad	-	-0.31 %	-	-	-0.76 %
	12508	100 krad	-	-0.15 %	-	-	-0.88 %
	12526	200 krad	-	-0.15 %	1.65 %	-	-1.20 %
	12527	200 krad	-	-0.43 %	1.14 %	-	-1.43 %
	12528	300 krad	-	-0.15 %	0.90 %	13.75 %	0.15 %
	12529	300 krad	-	-0.14 %	1.29 %	9.04 %	-0.57 %

F. Transition Time

Figure 8a to Figure 19b show the pre-irradiation and post-annealing transition edges. In each case, the radiation-induced transition-time degradation is not observable.

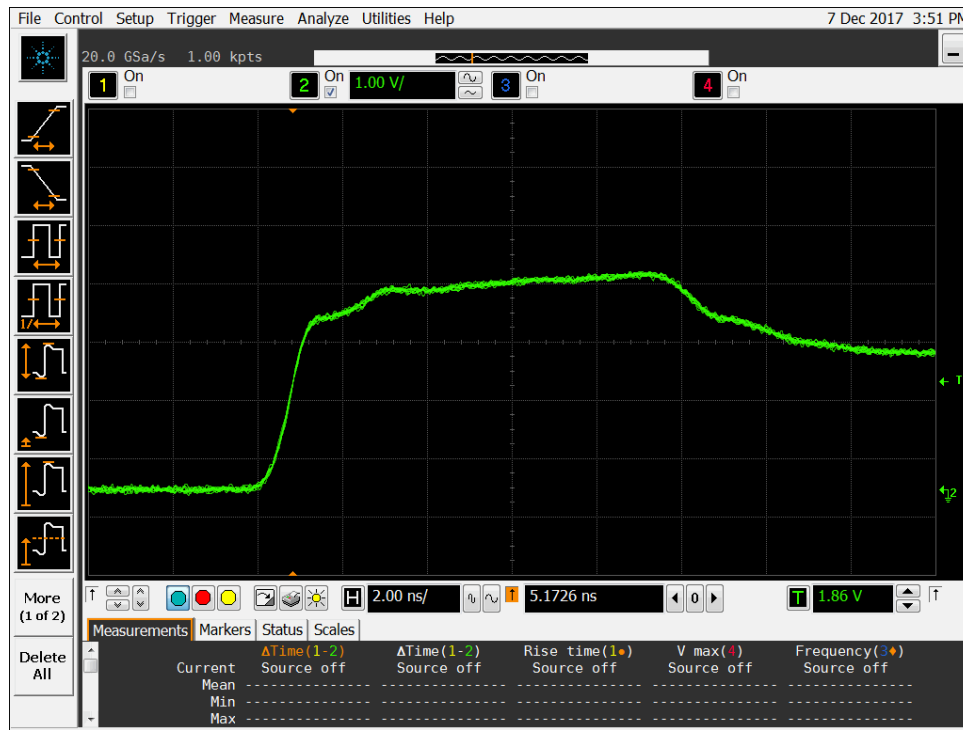


Figure 8a DUT 12528 Pre-Irradiation Rising Edge.

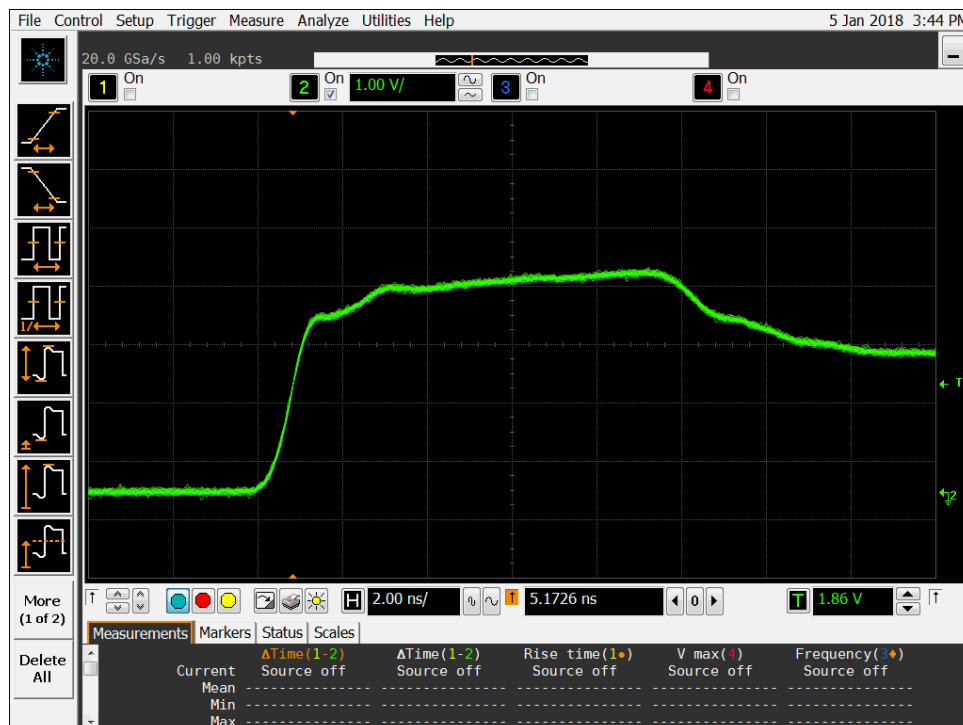


Figure 8b DUT 12528 Post-Annealing Rising Edge.

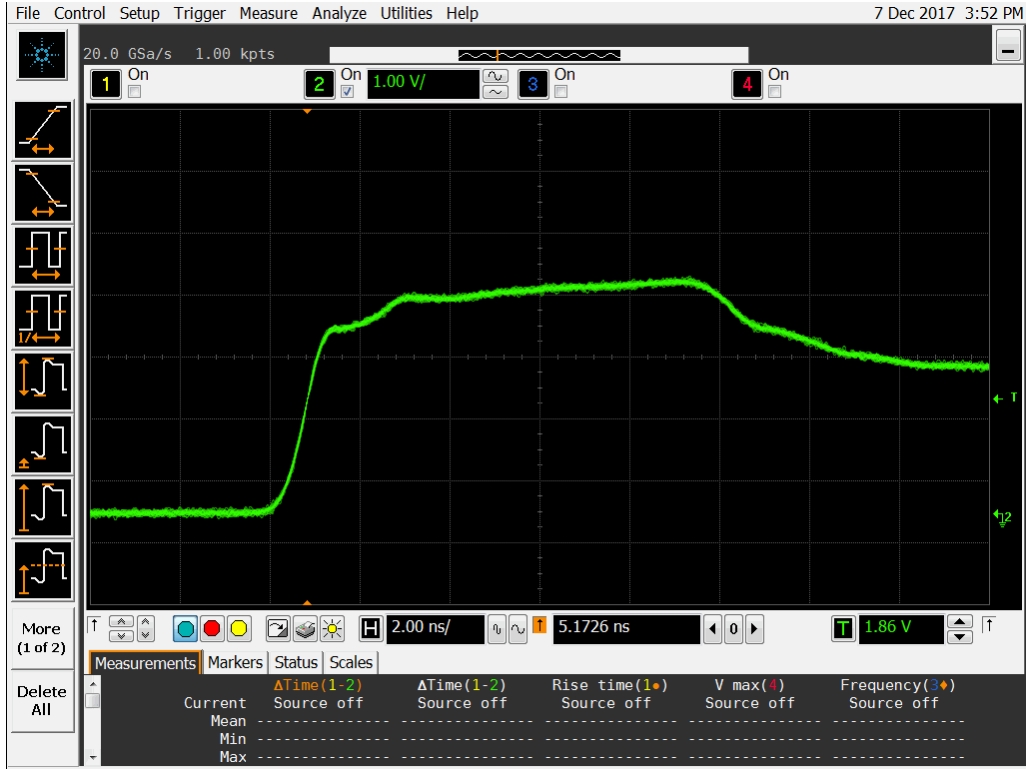


Figure 9a DUT 12529 Pre-irradiation Rising Edge.

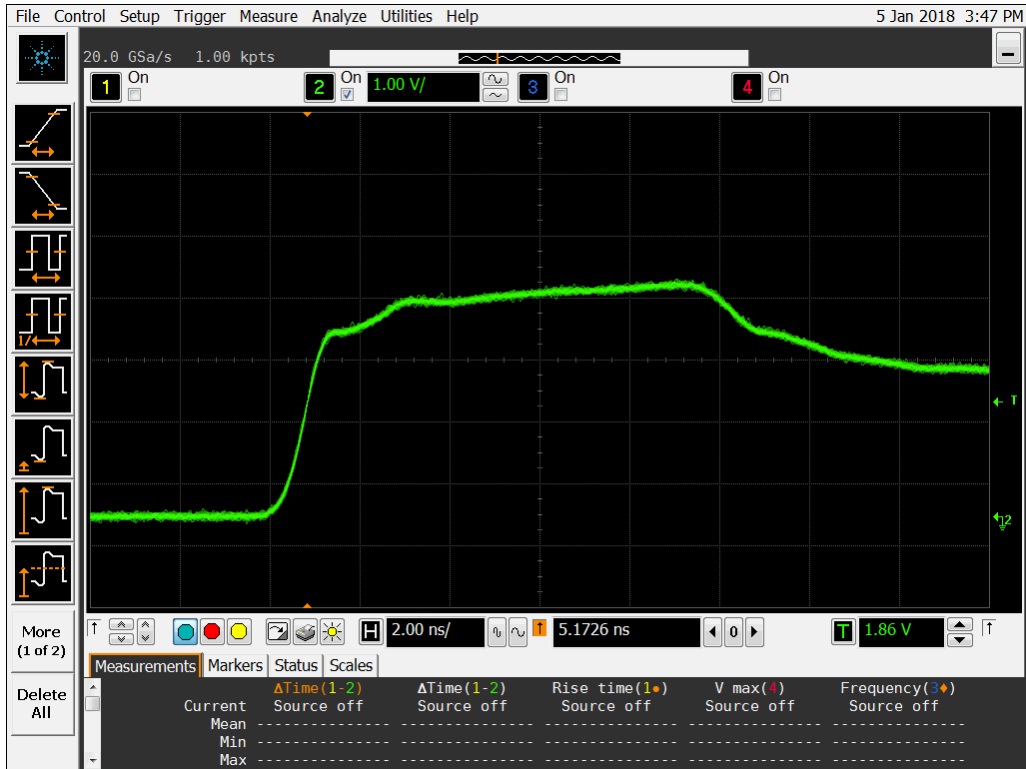


Figure 9b DUT 12529 Post-Annealing Rising Edge.



Figure 10a DUT 12526 Pre-Irradiation Rising Edge.

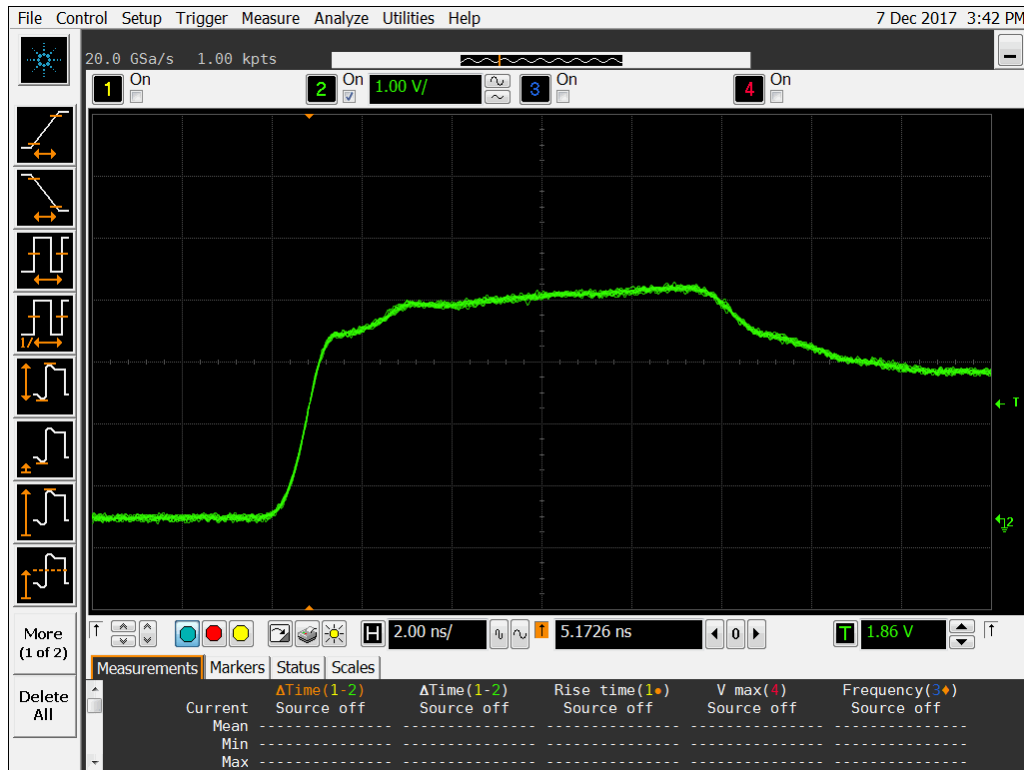


Figure 10b DUT 12526 Post-Annealing Rising Edge.

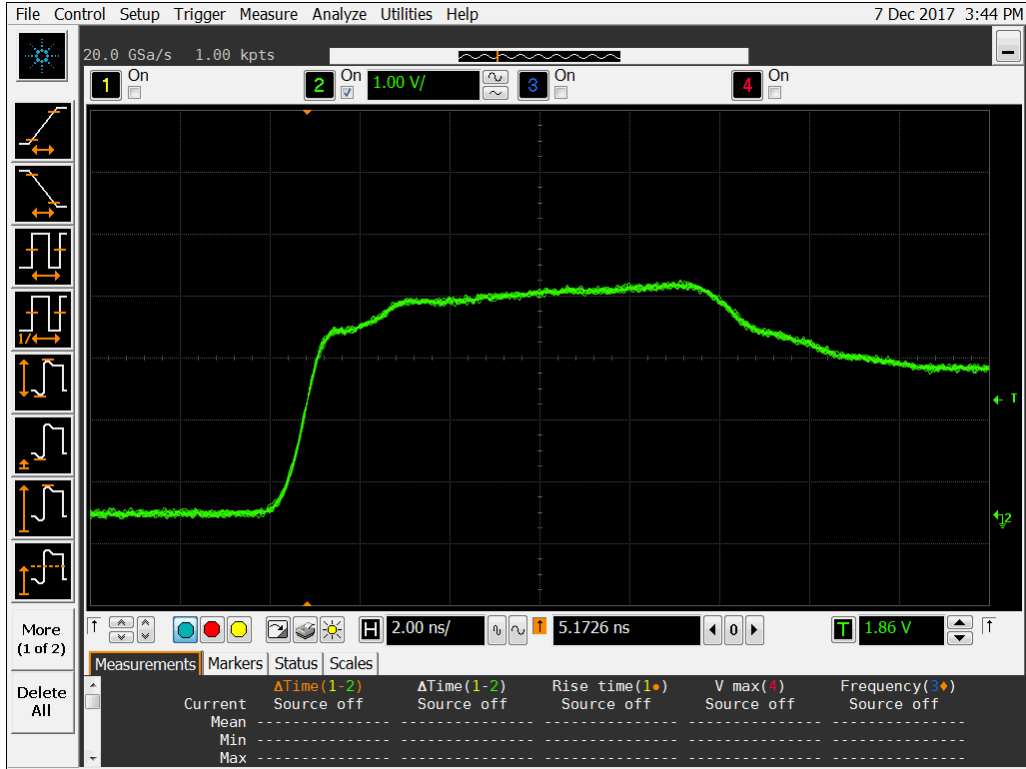


Figure 11a DUT 12527 Pre-Irradiation Rising Edge.

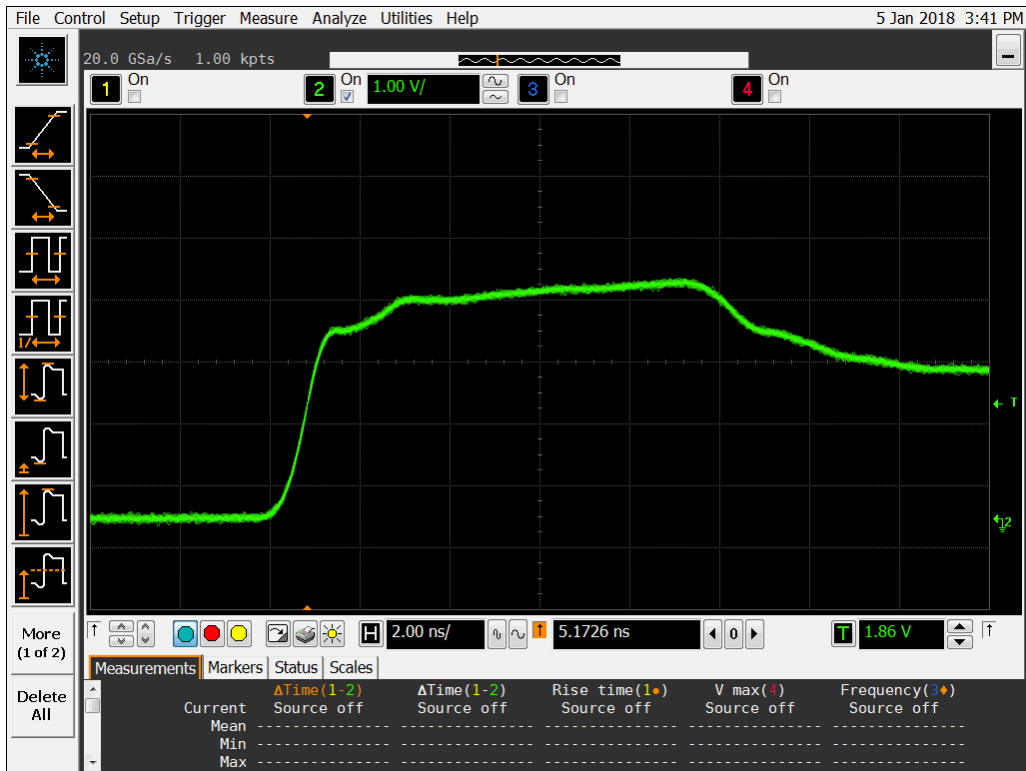


Figure 11b DUT 12527 Post-Annealing Rising Edge.

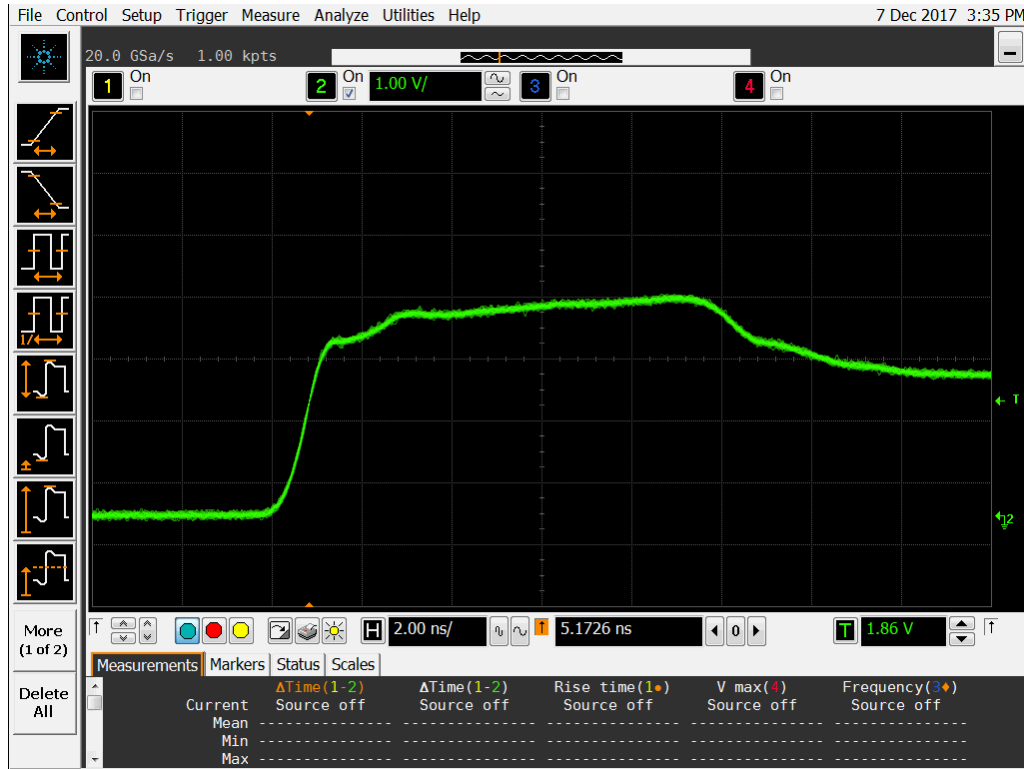


Figure 12a DUT 12503 Pre-Irradiation Rising Edge.

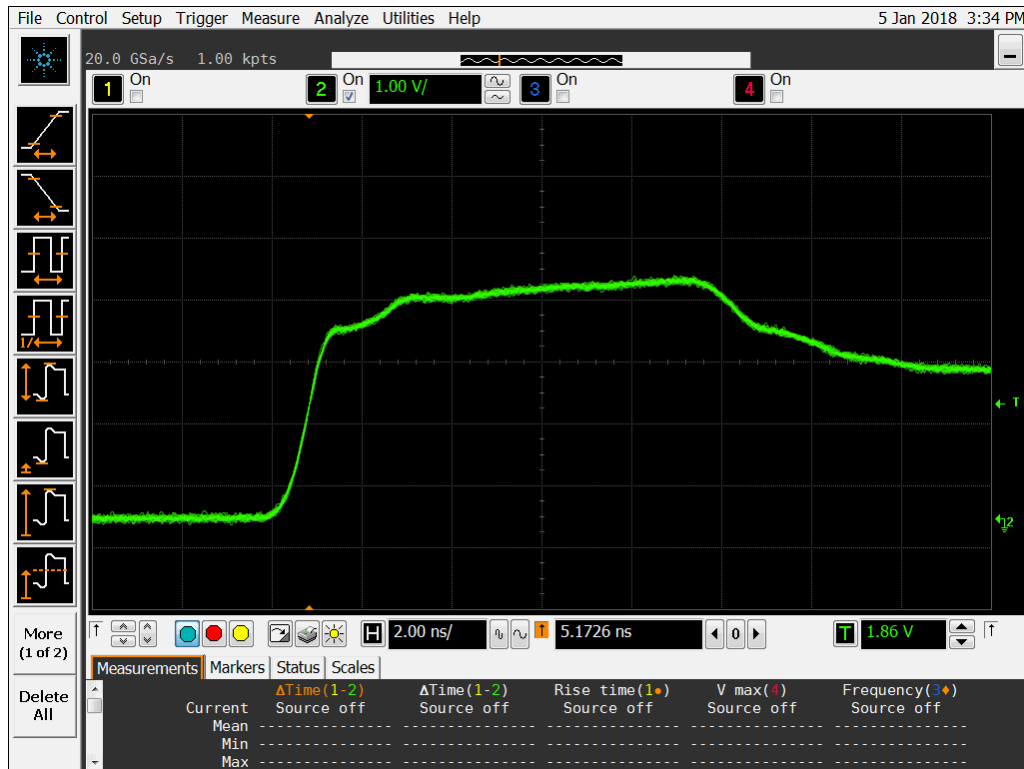


Figure 12b DUT 12503 Post-Annealing Rising Edge.

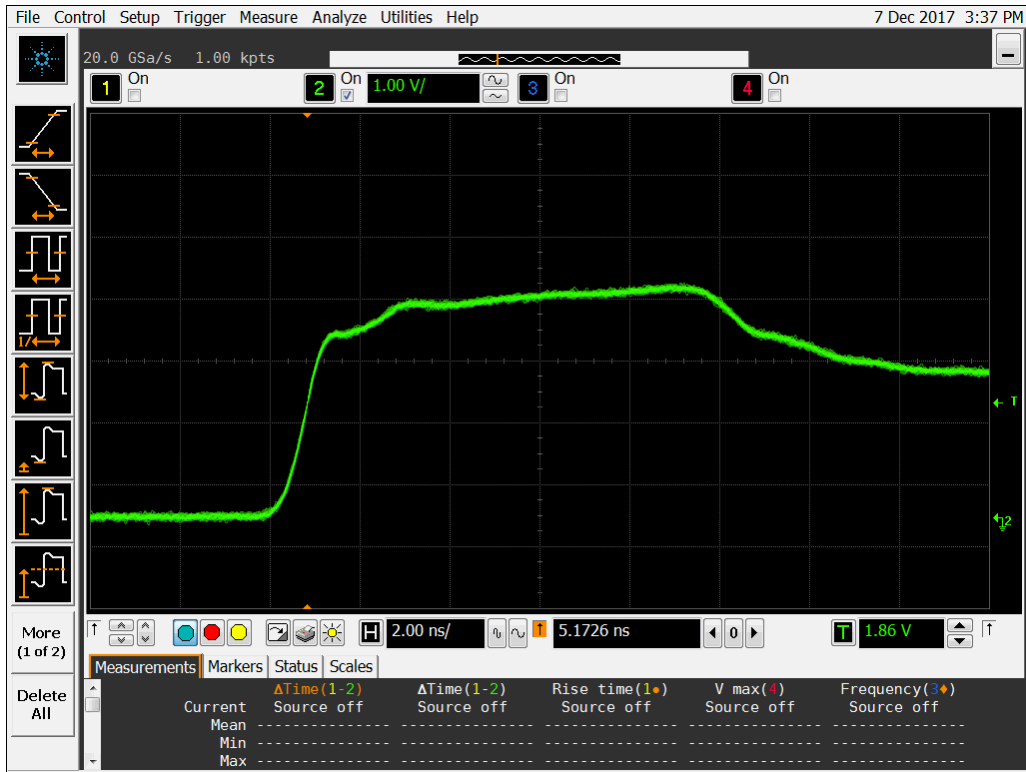


Figure 13a DUT 12508 Pre-Irradiation Rising Edge.

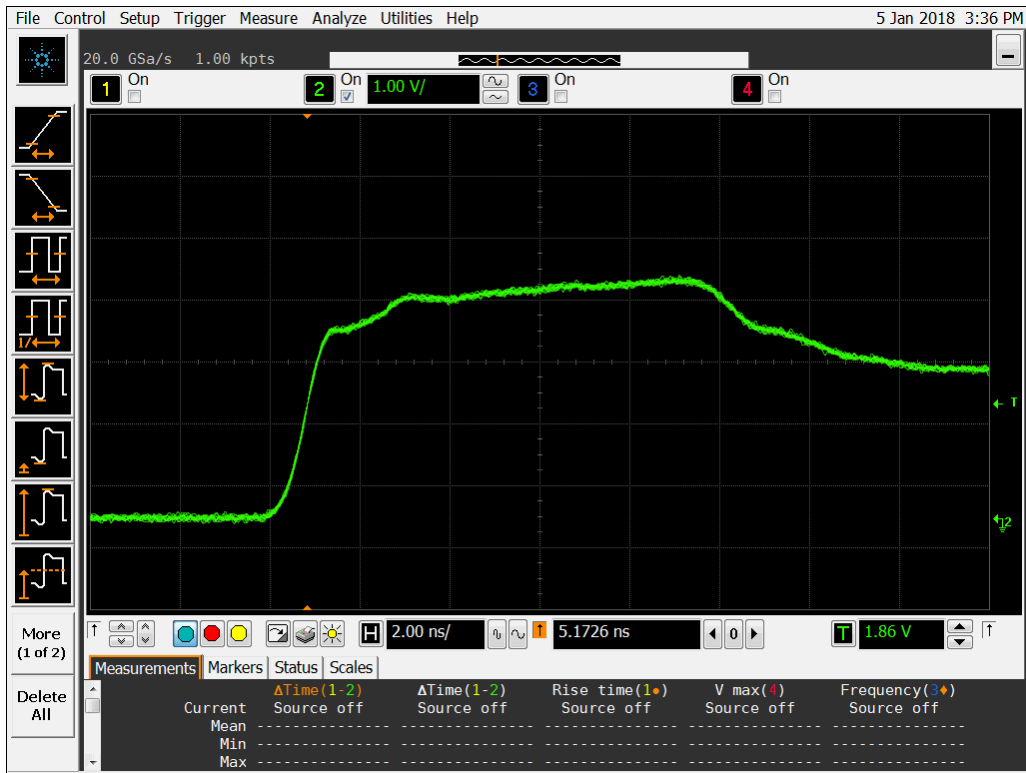


Figure 13b DUT 12508 Post-Annealing Rising Edge.

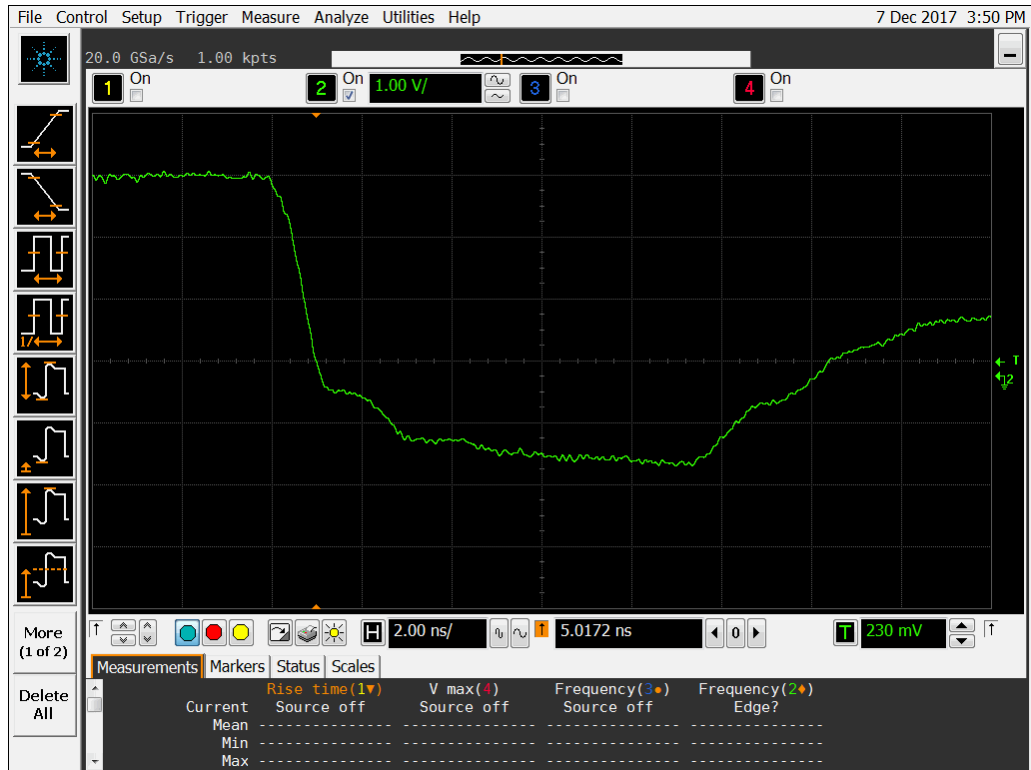


Figure 14a DUT 12528 Pre-Irradiation Falling Edge.

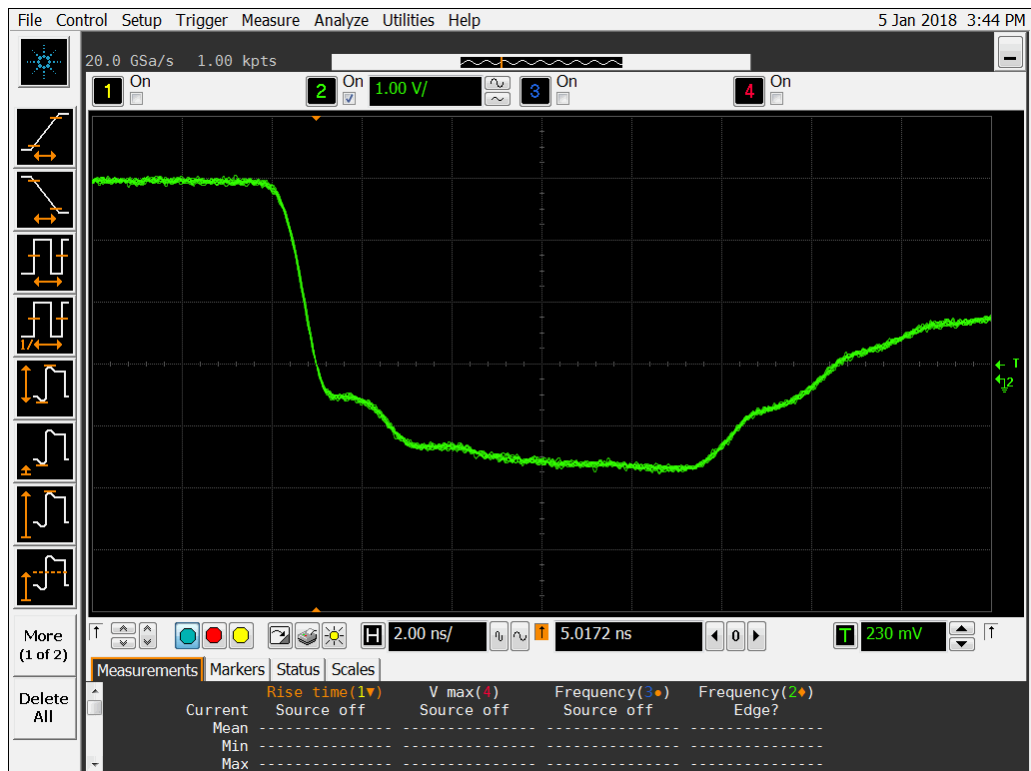


Figure 14b DUT 12528 Post-Annealing Falling Edge.

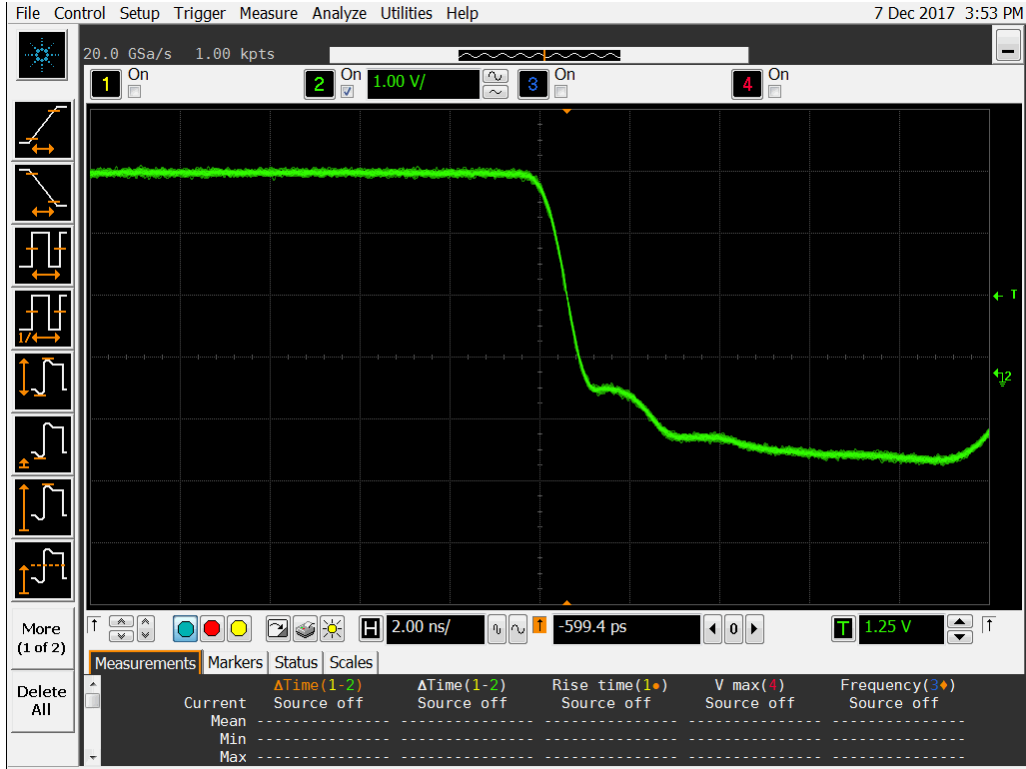


Figure 15a DUT 12529 Pre-Irradiation Falling Edge.

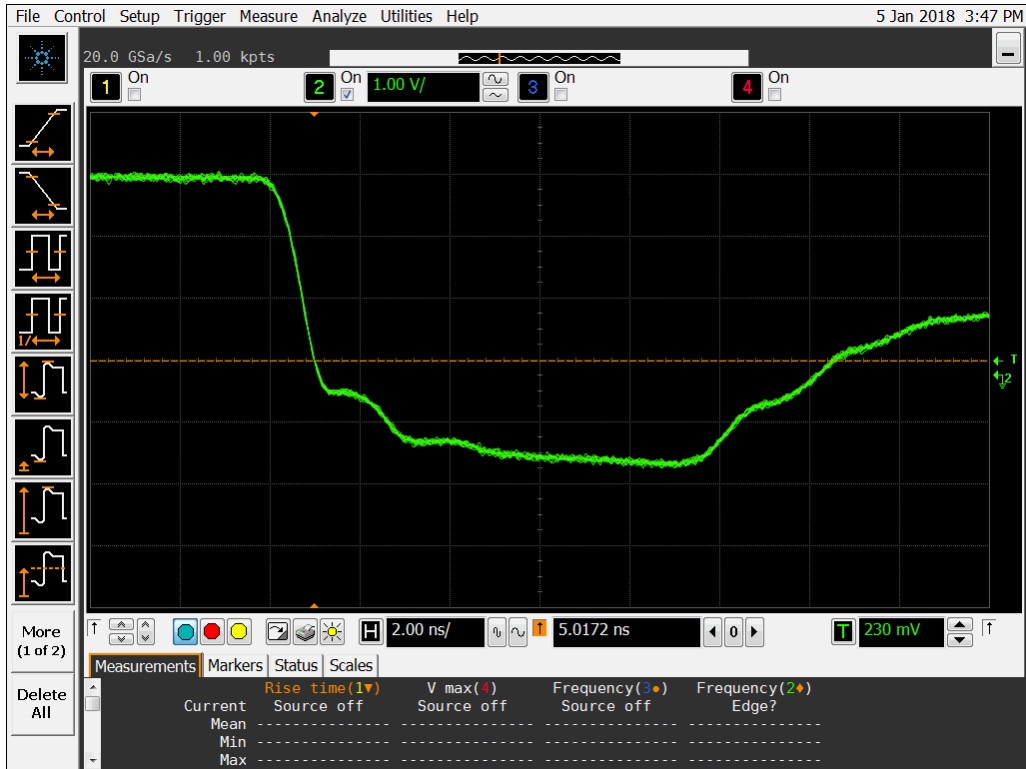


Figure 15b DUT 12529 Post-Annealing Falling Edge.

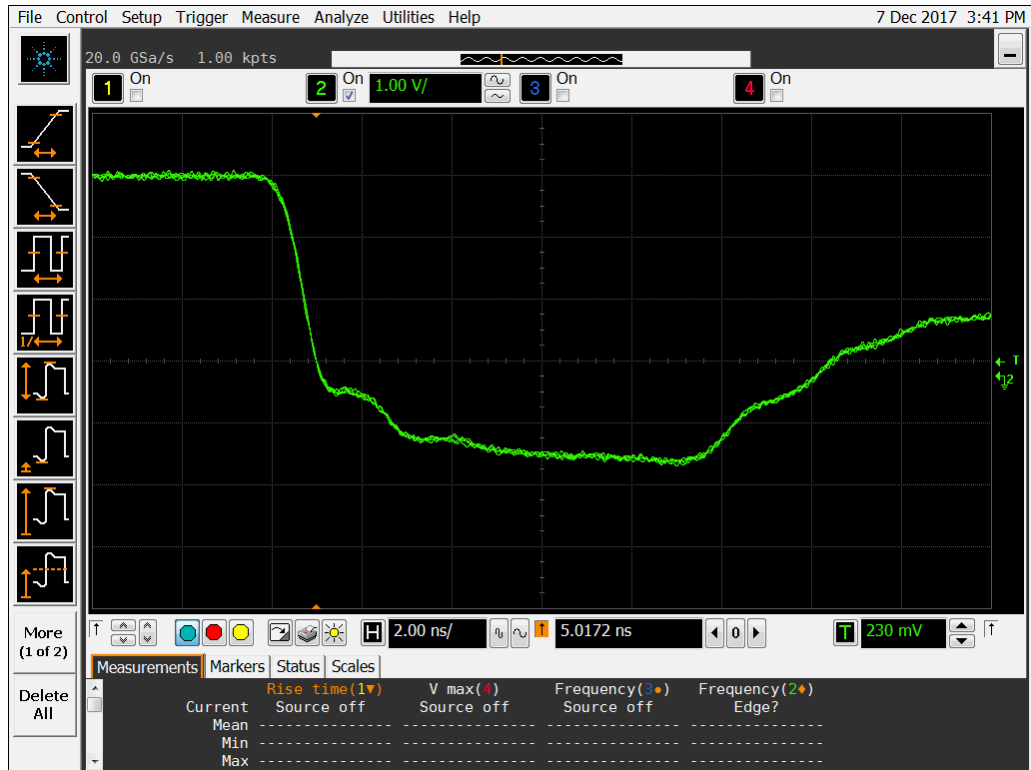


Figure 16a DUT 12526 Pre-Irradiation Falling Edge.

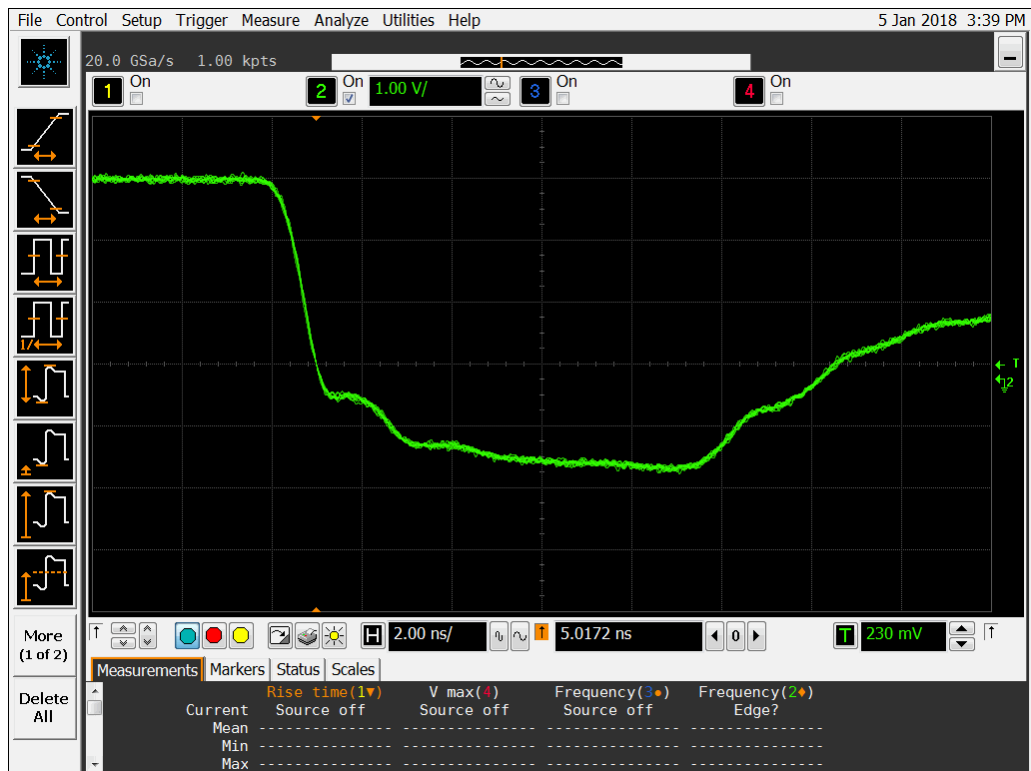


Figure 16b DUT 12526 Post-Annealing Falling Edge.

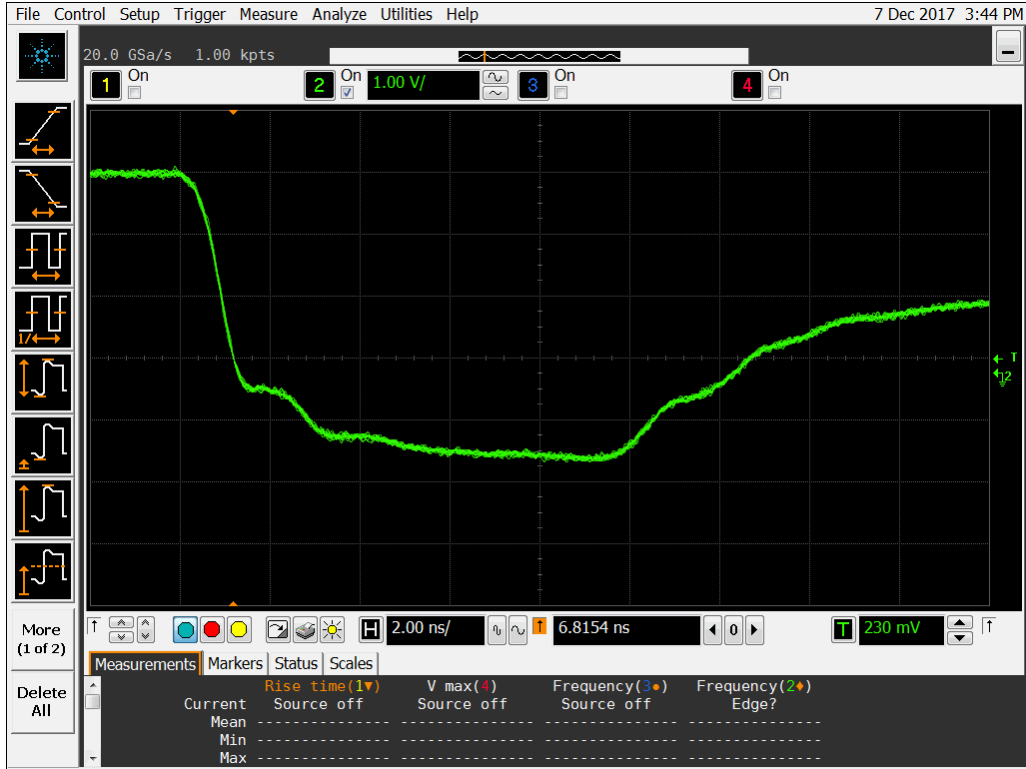


Figure 17a DUT 12527 Pre-Irradiation Falling Edge.

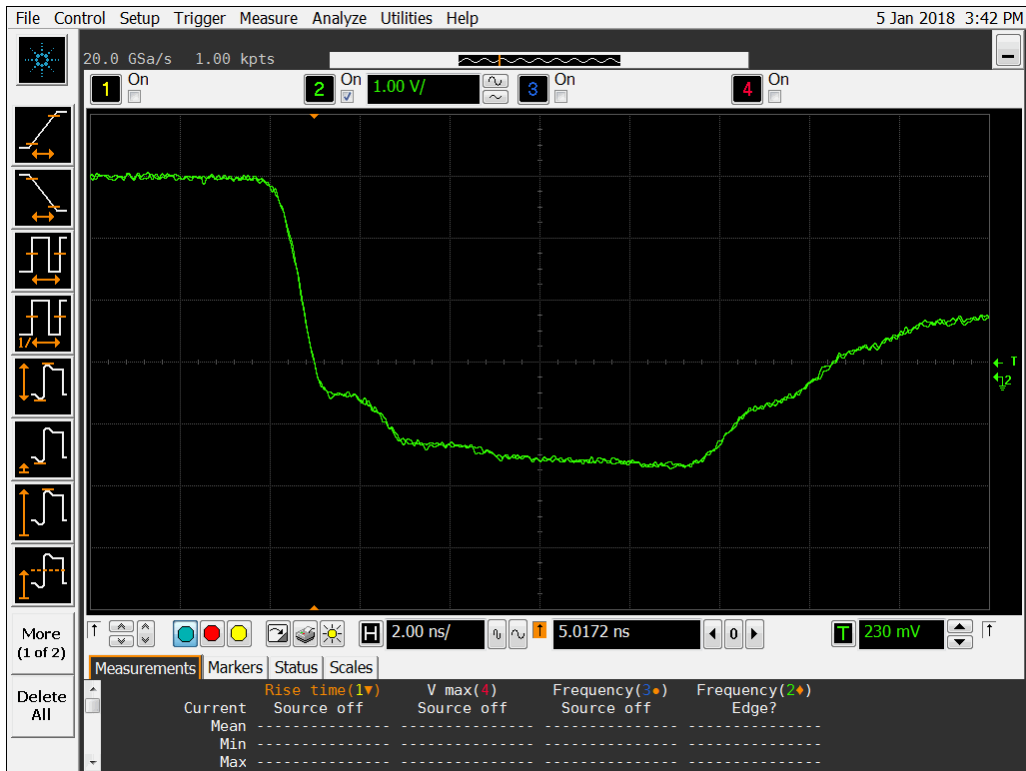


Figure 17b DUT 12527 Post-Annealing Falling Edge.

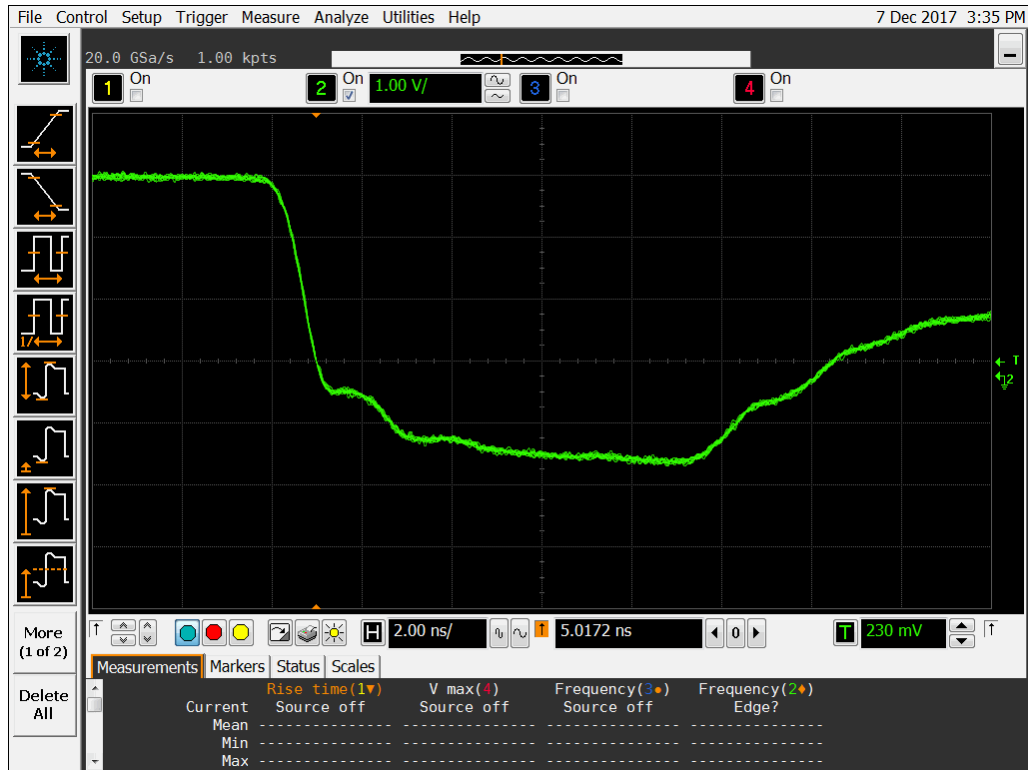


Figure 18a DUT 12503 Pre-Irradiation Falling Edge.

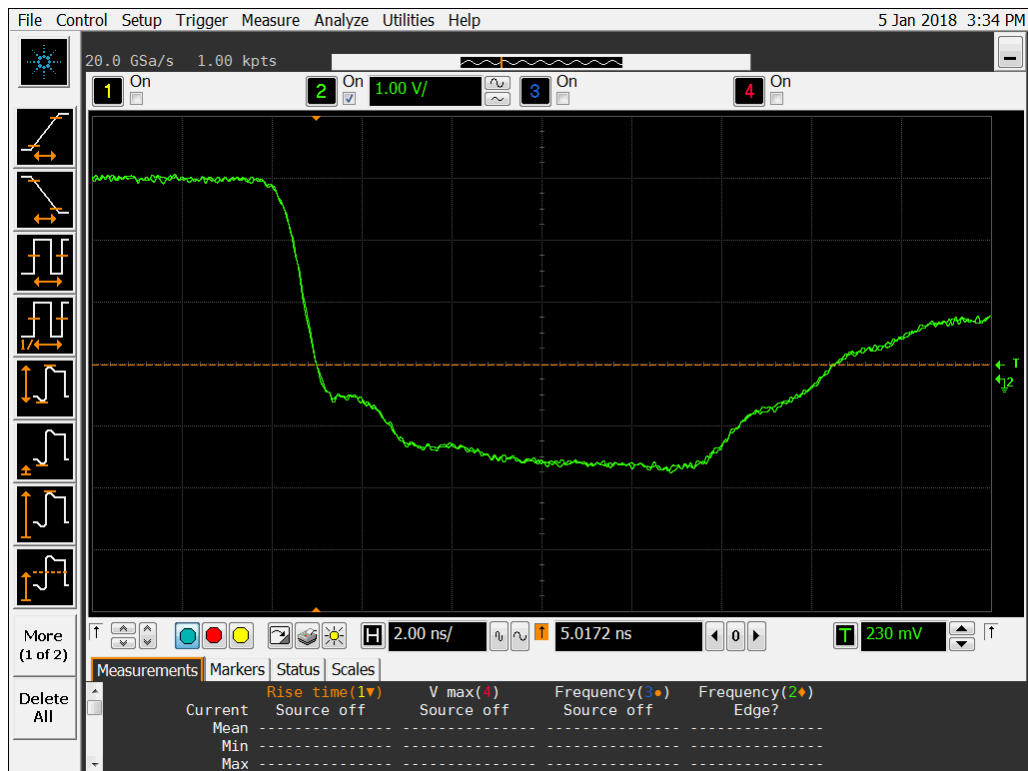


Figure 18b DUT 12503 Post-Annealing Falling Edge.

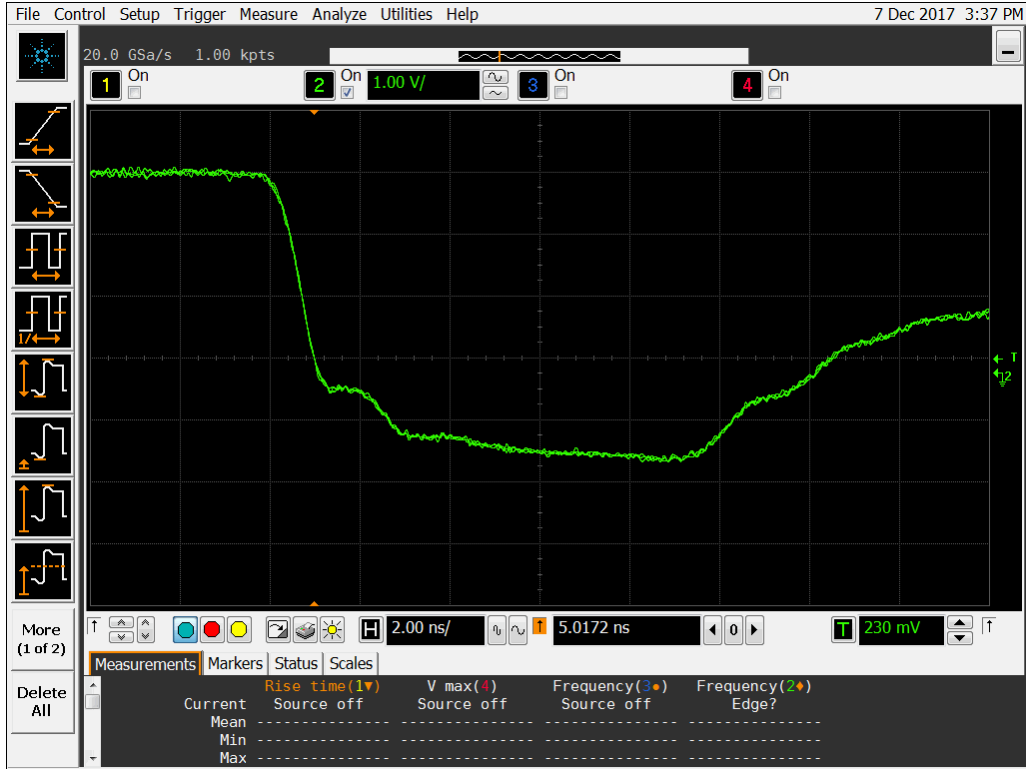


Figure 19a DUT 12508 Pre-Irradiation Falling Edge.

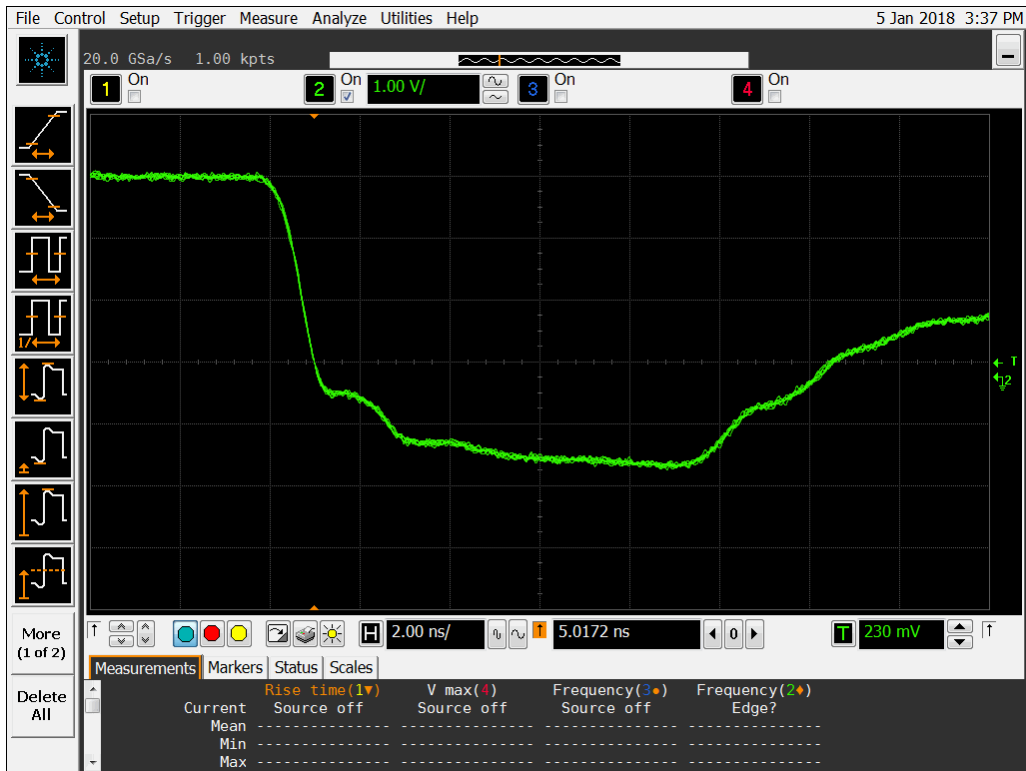


Figure 19b DUT 12508 Post-Annealing Falling Edge.

Appendix A: DUT Bias Diagram

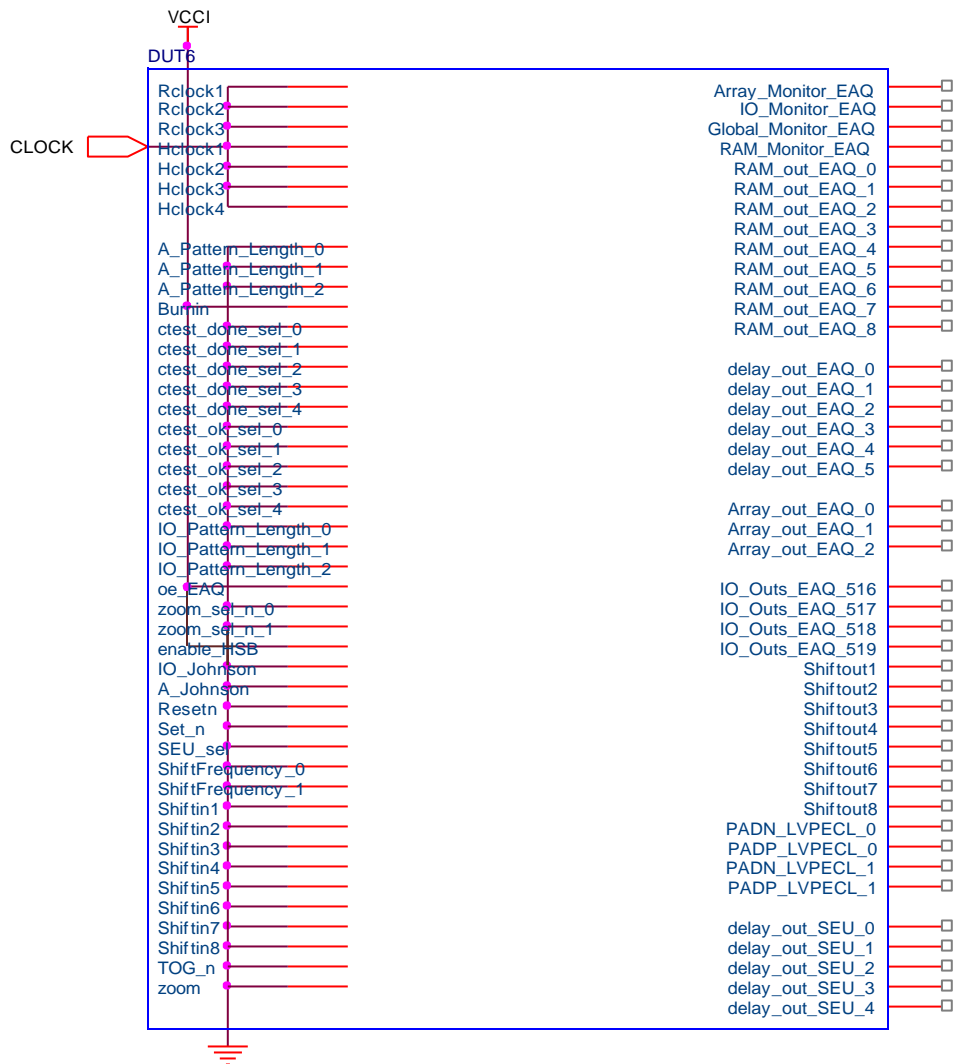


Figure A1 I/O Bias During Irradiation

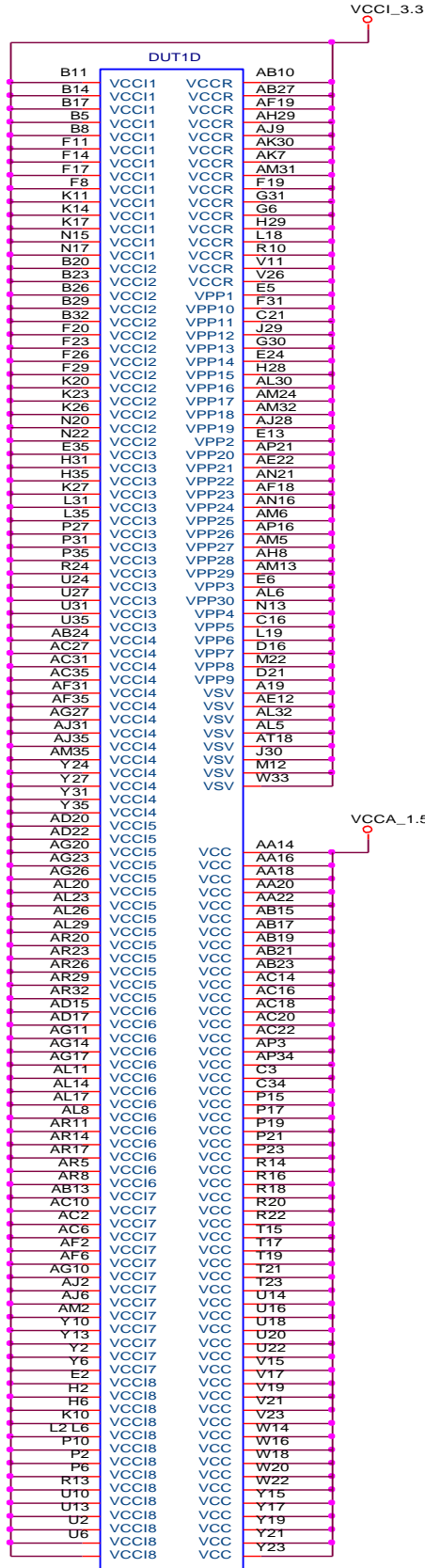


Figure A2 Power supply, Ground and Special Pins Bias During Irradiation

Appendix B: Functionality Tests

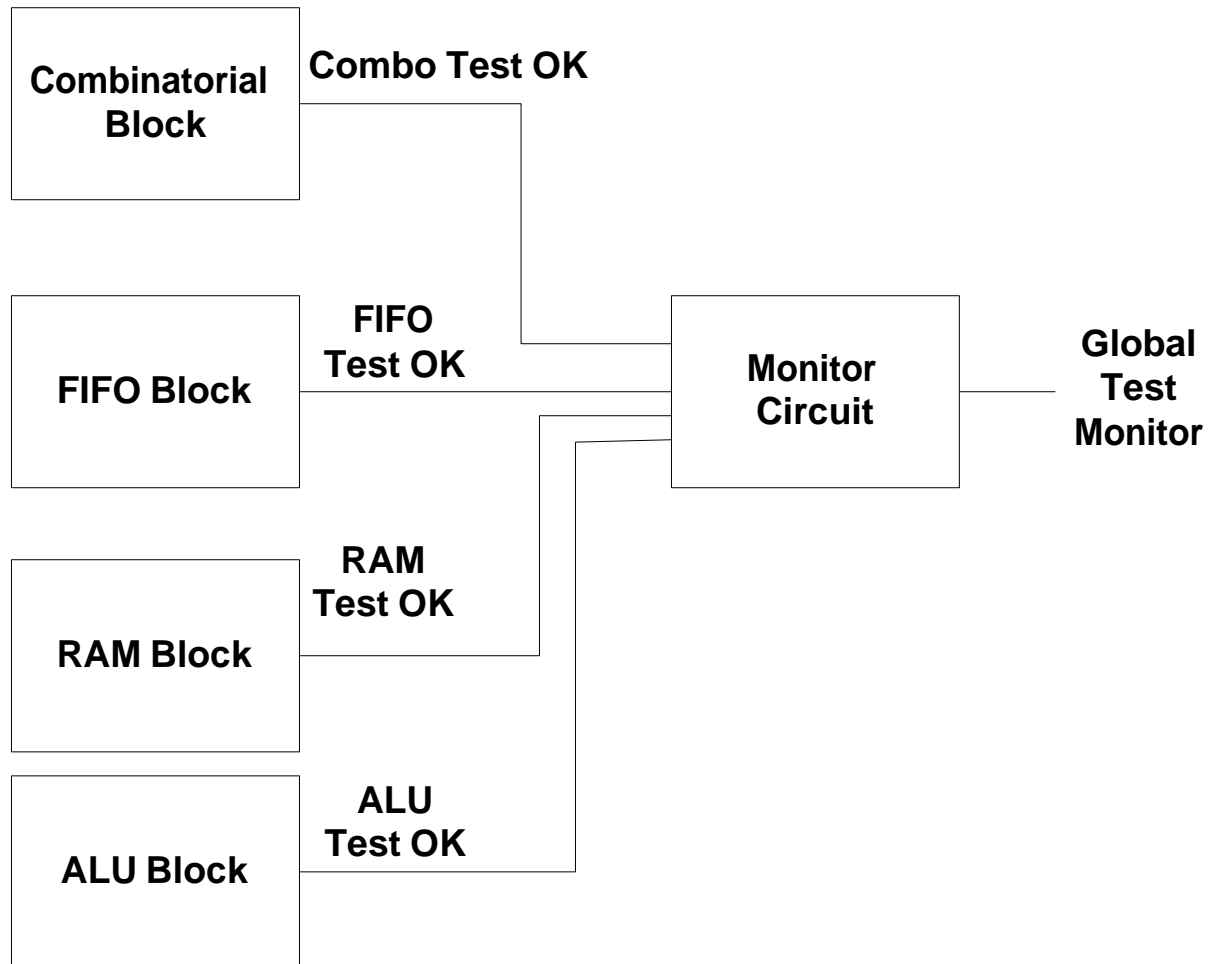


Figure B1 QBI Block – Top-Level Design

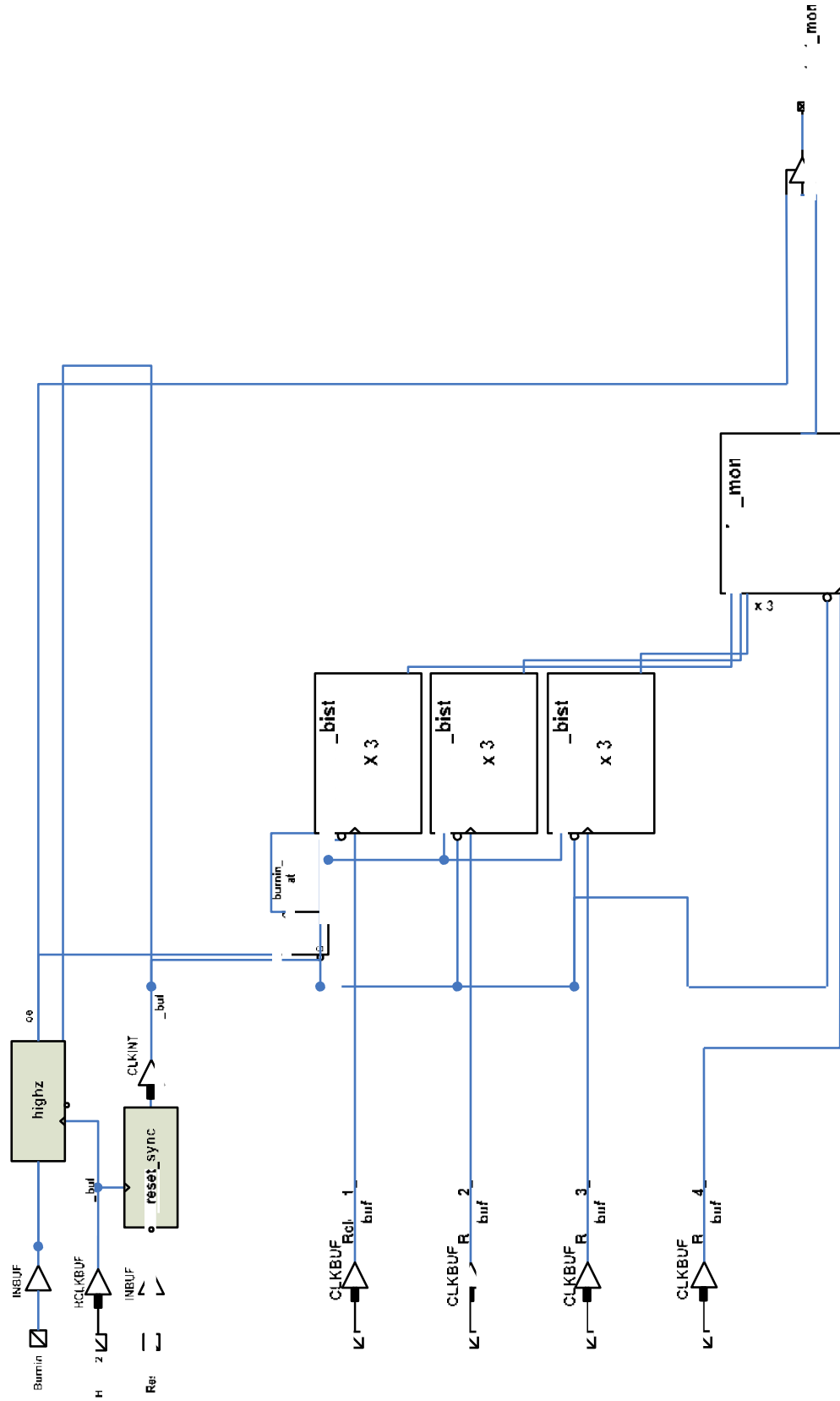


Figure B2 QBI Block – Combinatorial Test (Top Level)

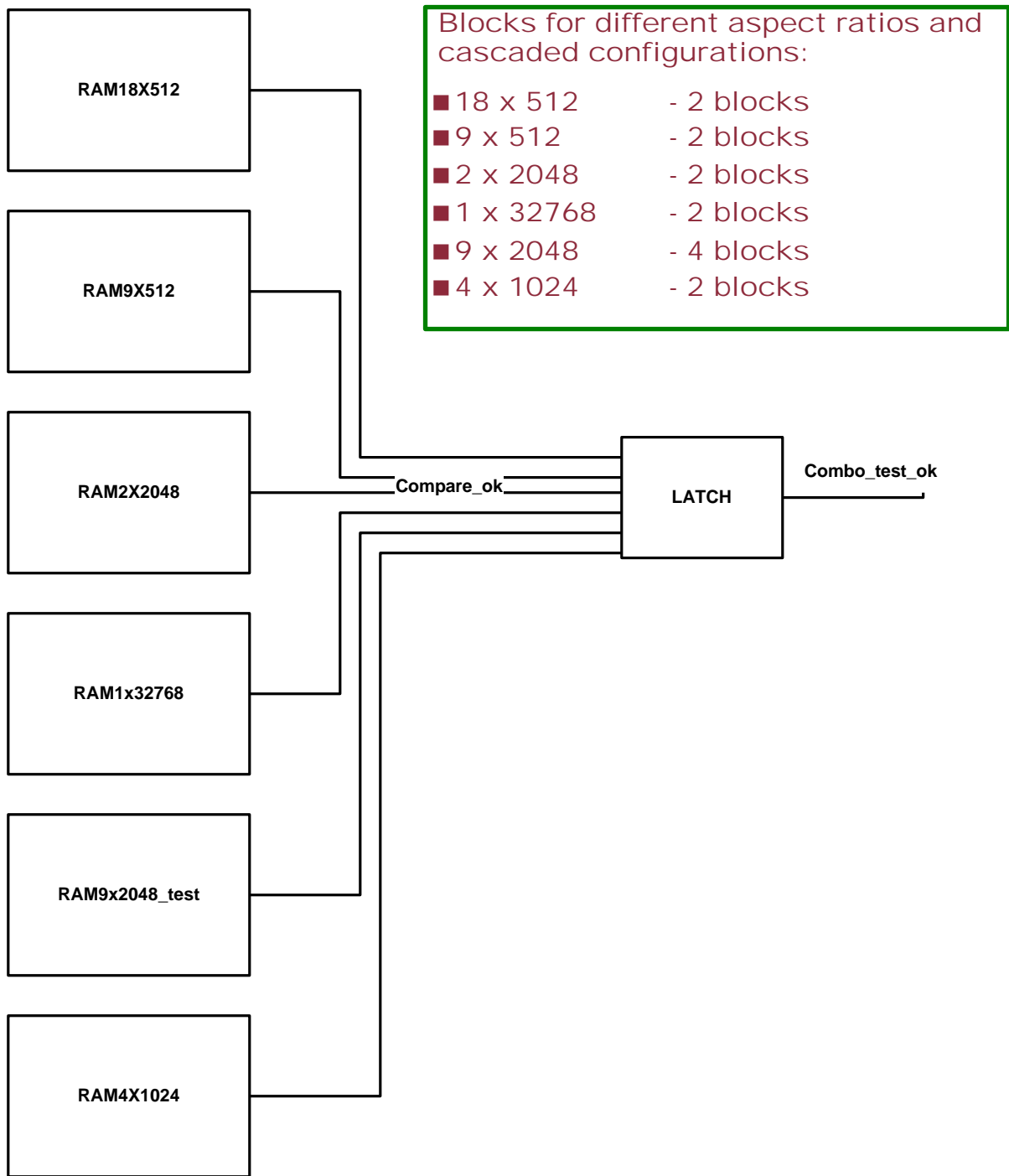


Figure B3 QBI Block – RAM Test (Top Level)

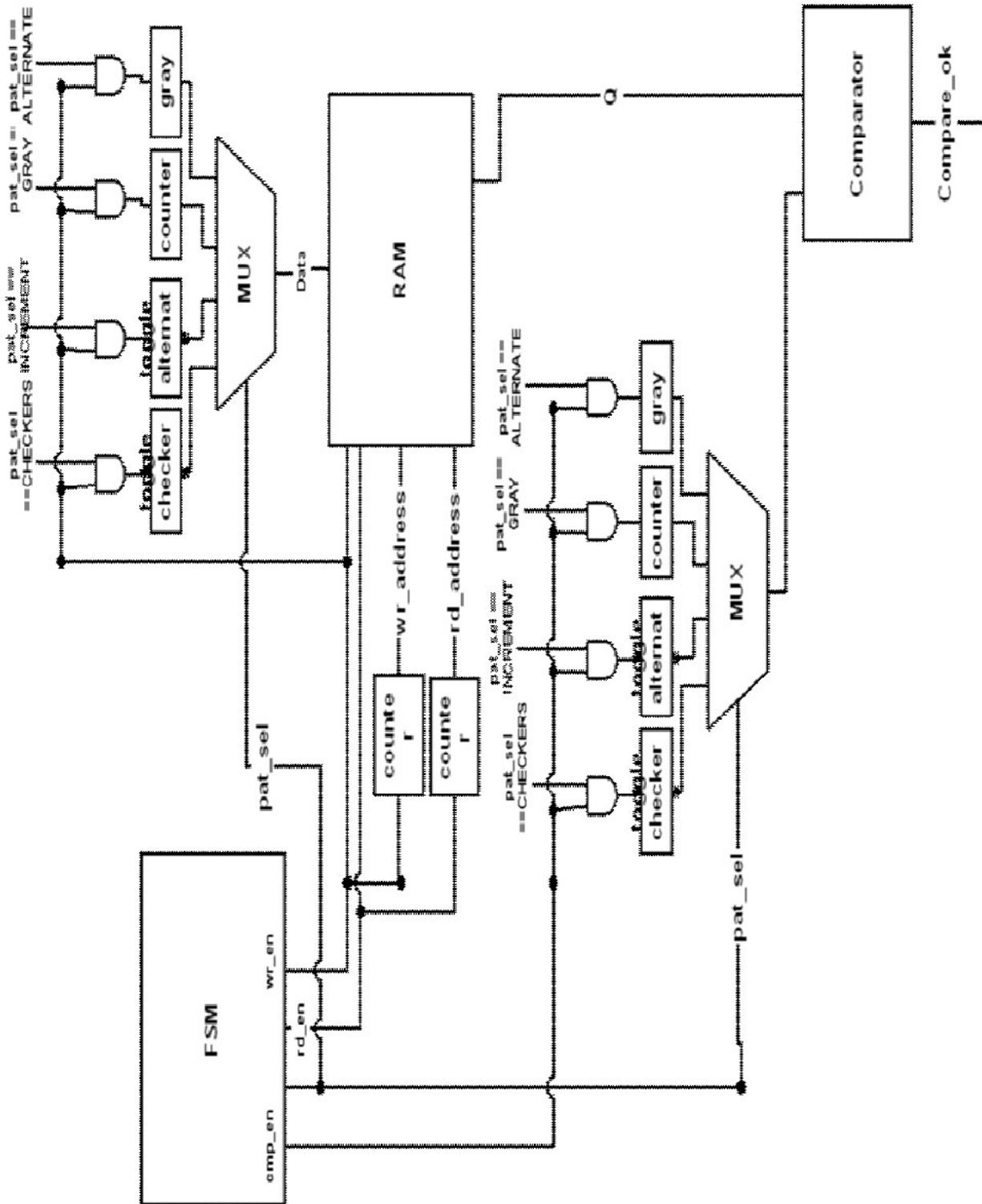


Figure B4 QBI Block – RAM Block

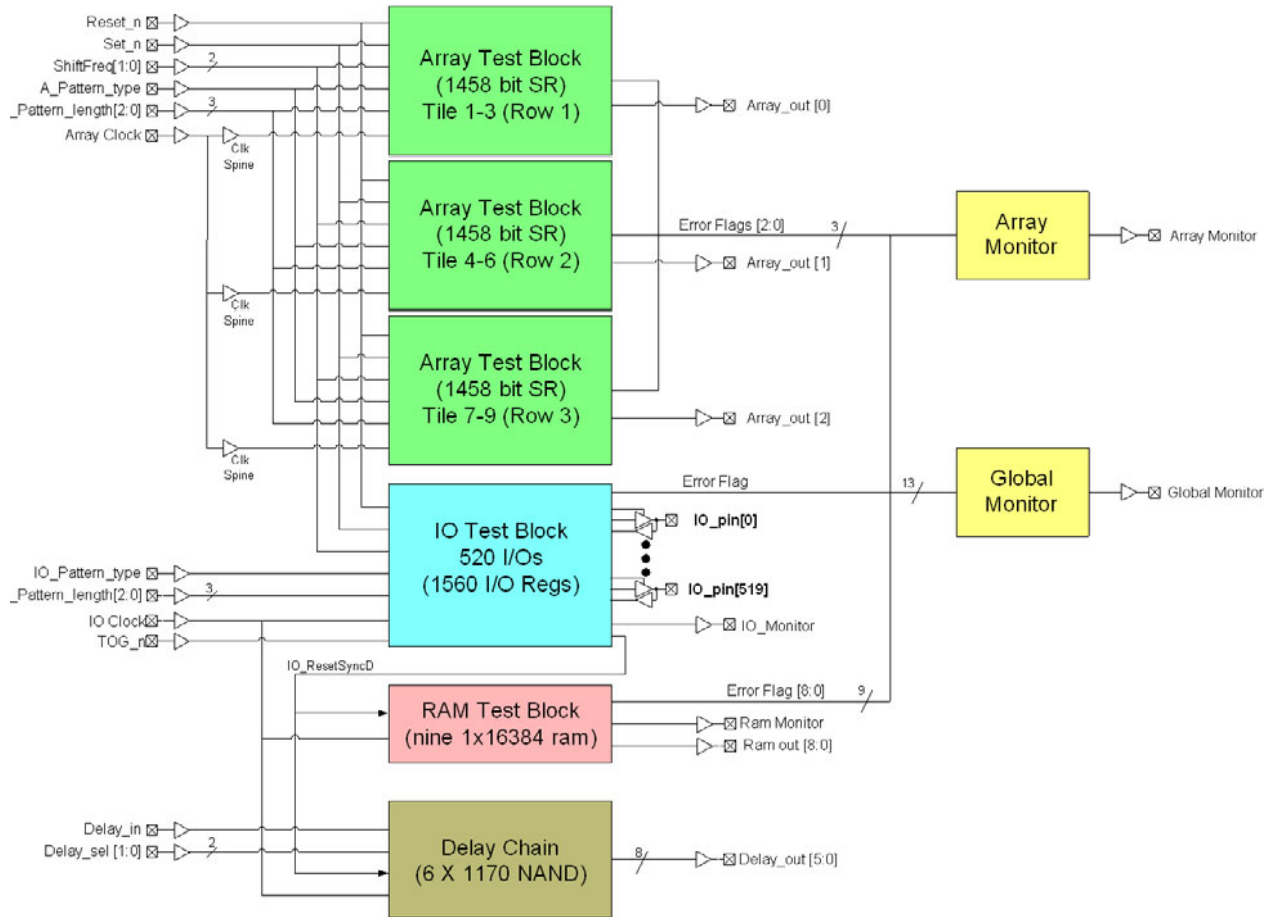


Figure B5 EAQ Block – Top Level

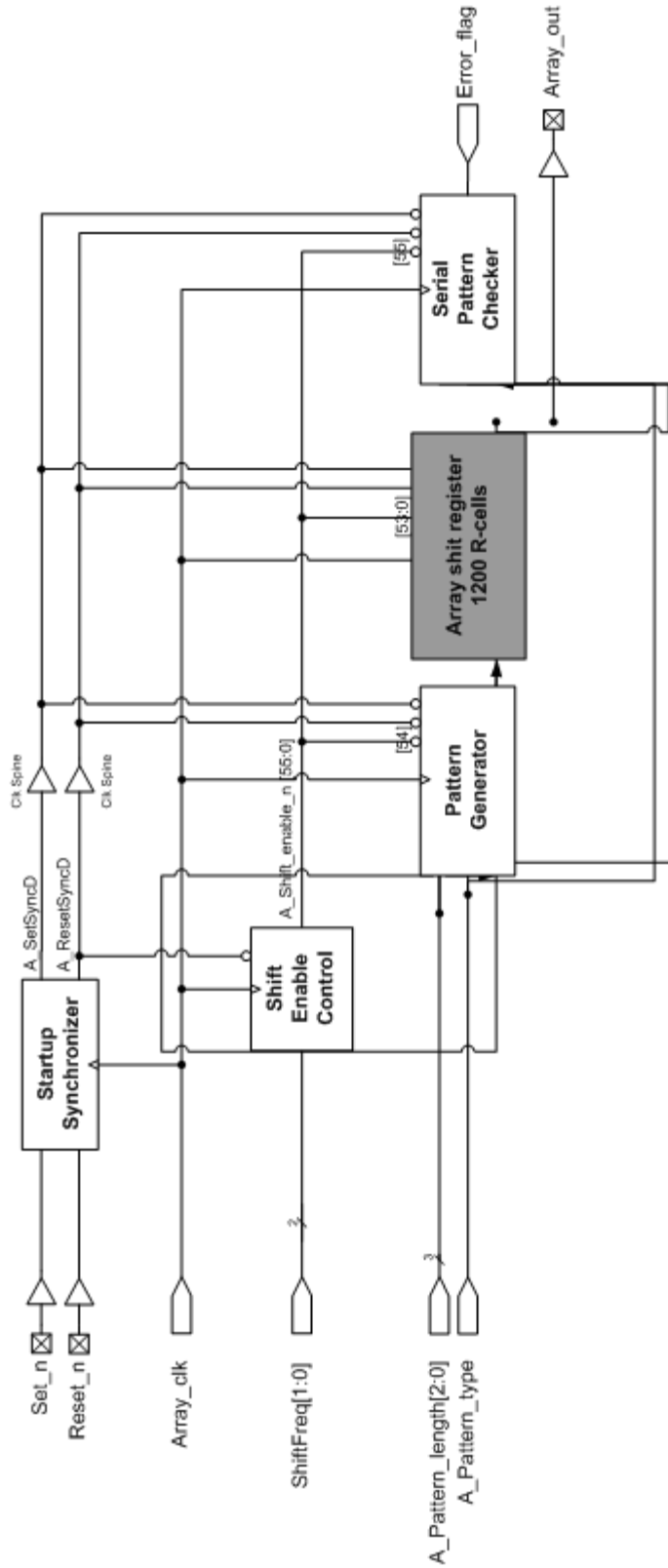


Figure B6 EAQ Block – Array Test (Shift Register)

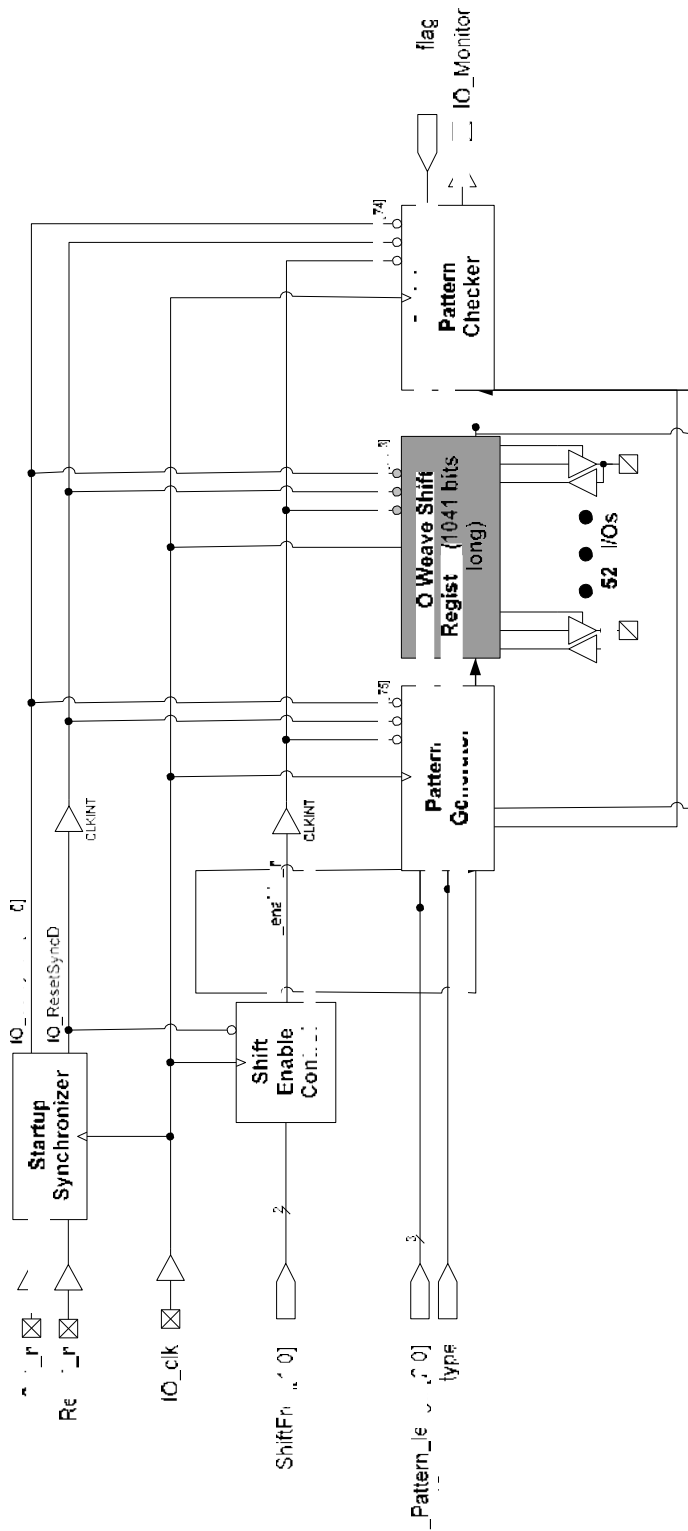


Figure B7 EAQ Block – I/O Test (Top Level)

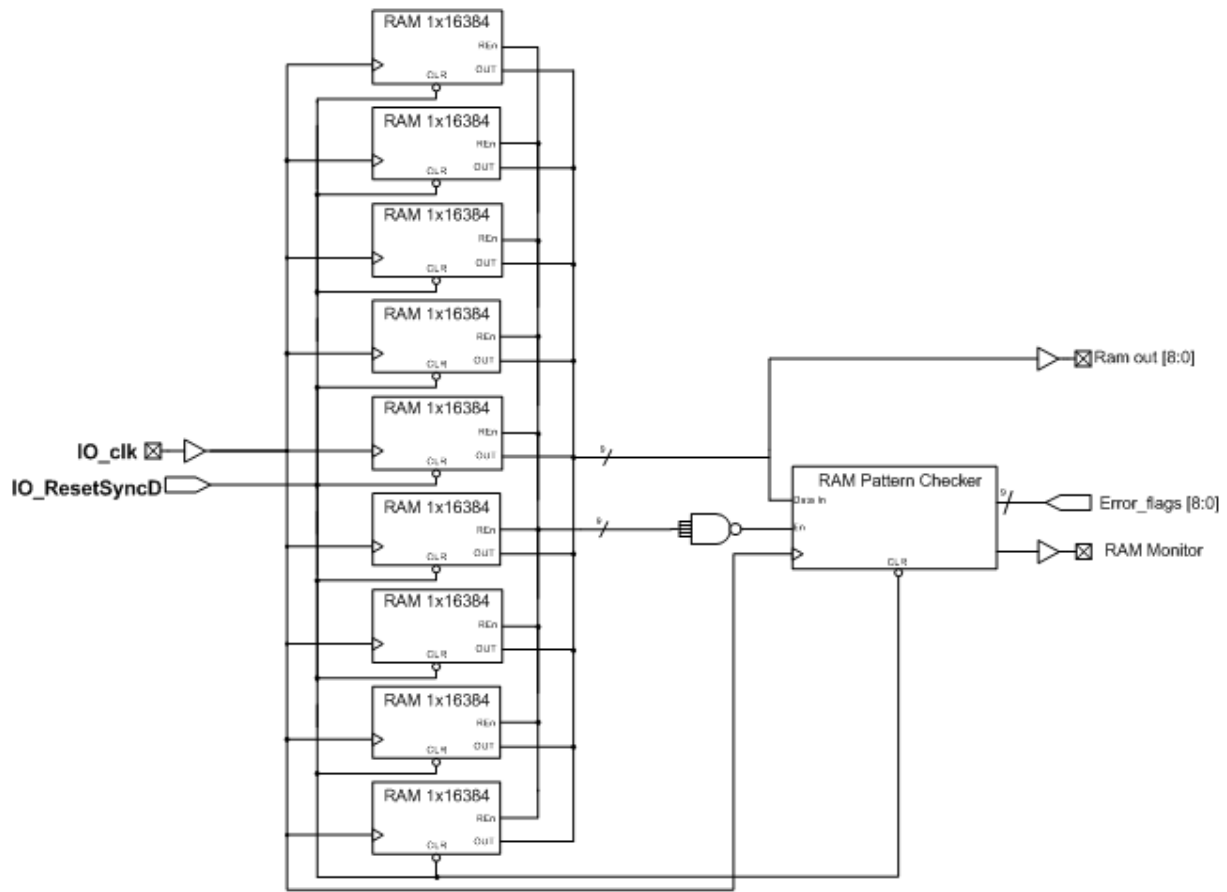


Figure B8 EQ Block – SRAM Test (Top Level)



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