



RTG4 TMR-PLL, Single-PLL, In-beam-POR and Program-Verify Testing Report

February 27, 2020

Nadia Rezzak, J.J. Wang, Paco Mok, Alex Cai

I. TEST OBJECTIVE

Heavy Ion testing is performed on Microsemi's RT4G150 device. The objectives are to test the single event effects (SEE) of TMR-PLL, Power-On-Reset (POR) and Program-Verify.

II. DEVICE UNDER TEST

Table 1 lists the facility and Device under test (DUT) parameters.

Table 1. Heavy Ion Testing Parameters

Condition	Setting
Beam Energy	25 MeV/Nucleon
Temperature	Room Temperature
Bias	1.2V, 2.5V & 3.3V
Sample Preparation	Back grinded RTG4 Rev C unit (production version), DUT#8565 thickness is 68 μm .

III. TEST METHODS

The test generally follows the guidelines of two SEE testing standards: ASTM standard F1192M-95, "Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation on Semiconductor Devices," and JEDEC standard JESD57, "Test Procedures for the Measurement of Single-Event Effects in Semiconductor Devices from Heavy Ion Irradiation."

1. Facility

The cyclotron laboratory at Texas A&M University (TAMU) in College Station TX, provides the heavy-ion source. In this report, the SEE testing uses the 25 MeV/n beam line.

2. Irradiation

Table 2 list the ions and their respective LETs.

Table 2. Ion and LET

Ion-Tilt	LET
Ne-(0)	1.9
Ar-(0)	6.6
Kr-(0)	23.3
Ag-(0)	37.3
Xe-(0)	46.4

IV. DUT DESIGN

1. TMR-PLL

The RTG4 PLL is configured into two modes: 1) TMR mode using PLL internal Feedback, and 2) single mode (Non TMR mode) using CCC internal feedback. In both modes, the monitored signals are the lock signal, and the heartbeat signal to identify that the output clock is toggling. The integrity of the TMR-PLL output clocks was also monitored.

The main goal is to validate that the Auto Reset circuit implemented in Libero SoC v11.9 successfully recovers all TMR-PLL loss of lock and to monitor the TMR-PLL output clock integrity. Previous PLL tests, as described in the [RTG4 PLL and Internal Oscillator SEE Report](#), indicated that when the TMR-PLL voted lock was lost, it never recovered unless a reset to the PLL was issued. By implementing the Auto Reset circuit to the TMR-PLL, its loss of lock cross section and error rate are reduced.

A. TMR-PLL Mode Tested in Two Configurations:

1. TMR-PLL 50 MHz External Reference Clock: The 50 MHz off-chip clock is not irradiated (Fig 1).
2. TMR-PLL Internal Reference OSC-Clock: The 50 MHz on-chip Oscillator clock is irradiated (Fig 2).

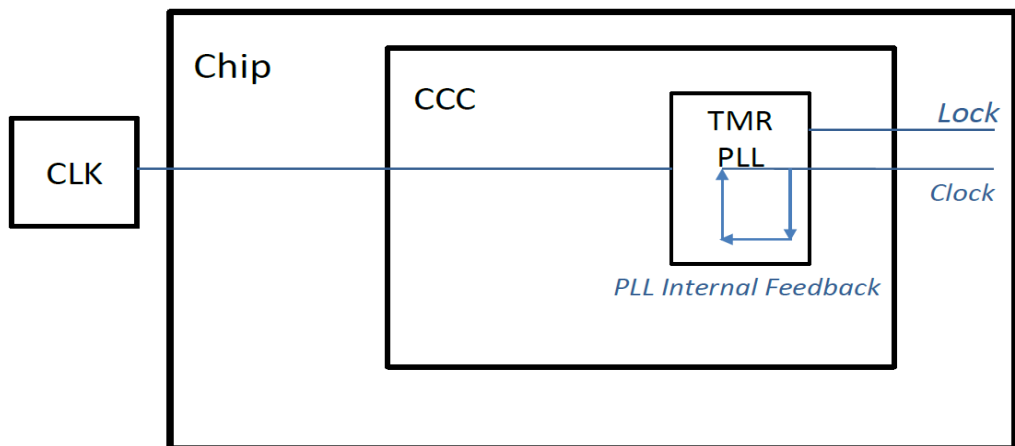


Fig 1. Block diagram shows a 50MHz external clock feeding into TMR-PLL with PLL-internal feedback.

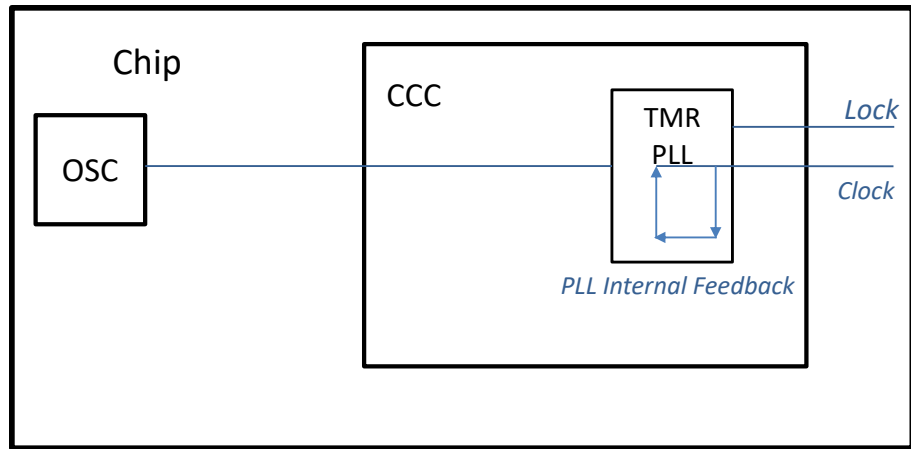


Fig 2. Block diagram shows an internal 50MHz oscillator feeding into TMR-PLL with PLL-internal feedback.

B. The Single-PLL Mode Tested in Three Configurations:

1. Single-PLL External 50MHz Reference Clock: The 50 MHz off-chip clock is not irradiated (Fig 3).
2. Single-PLL External 20MHz Reference Clock: The 20 MHz off-chip clock is not irradiated (Fig 3).
3. Single-PLL Internal Reference OSC-Clock: The 50 MHz on-chip Oscillator clock is irradiated (Fig 4).

Test configuration 2 above is to compare data with [previous Single-PLL mode testing](#) using external 20 MHz clock.

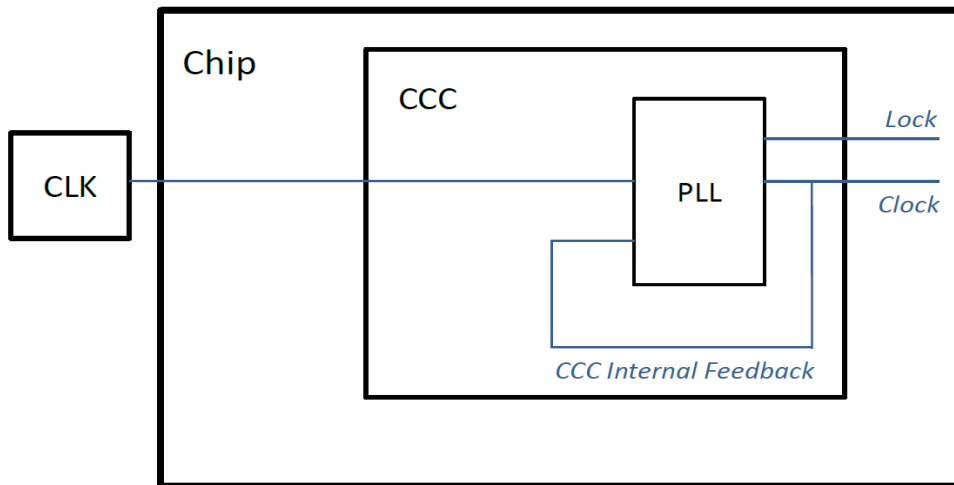


Fig 3. Block diagram illustrates an external clock feeding into single PLL with CCC-internal feedback.

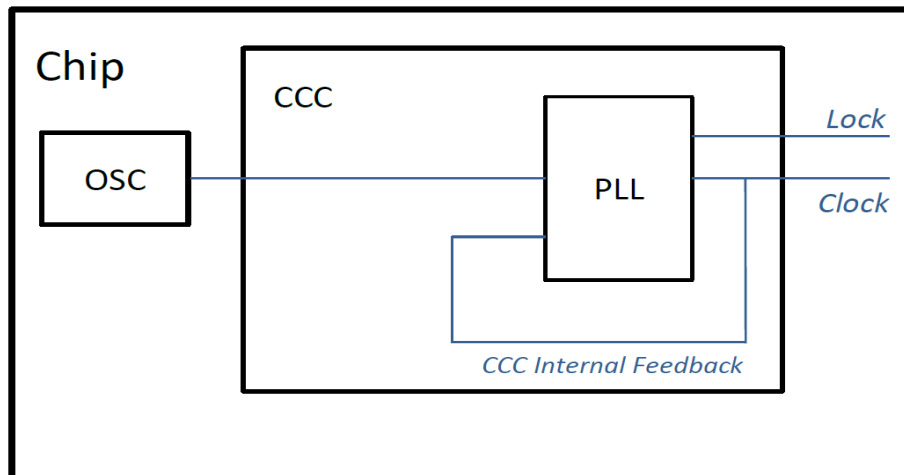


Fig 4. Block diagram shows an internal oscillator feeding into single PLL with CCC-internal feedback.

2. POR and In-beam Program-Verify

The Power-On-Reset (POR) test consists of performing 10 consecutive power cycles in-beam while monitoring the chip's functionality.

In-beam Program-Verify test starts with an in-beam program followed by a stand-alone verify also in-beam. To match the space environment, the beam-flux has to be reduced to the lowest possible allowed by the test facility, which is approximately 35 ions/cm²/s. Since previous In-beam Program-Verify testing data at higher beam-flux of 10³ ions/cm²/s indicated the failure to complete the Program-Verify processes was non-destructive, a LET of 37 MeV-cm²/mg is considered sufficient for this test.

V. HEAVY-ION TESTING RESULTS

1. TMR-PLL Weibull Curves

Fig 5 shows the TMR-PLL loss-of-lock recovered cross sections versus LET using external clock and using internal-OSC clock. The Auto Reset circuit implemented in Libero design successfully recovered all loss of lock. Fig 1 shows the PLL configuration with the 50-MHz external clock and Fig 2 shows the PLL configuration with the on-chip 50-MHz oscillator. The extracted Weibull parameters are summarized in Tables 1 and 2.

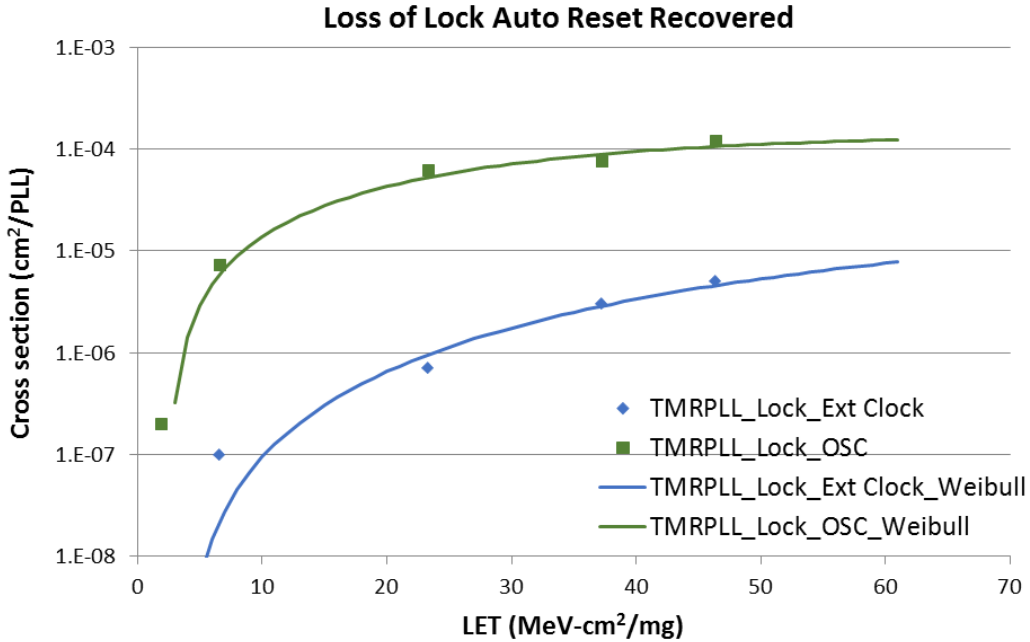


Fig 5 TMR-PLL loss-of-lock Auto Reset recovered Results.

Table 1. TMR-PLL Lock Ext Clock Auto Reset Recovered Weibull Parameters

L0	W	S	A0
2	80	2.2	2.00E-05

Table 2. TMR-PLL Lock OSC Auto Reset Recovered Weibull Parameters

L0	W	S	A0
1.4	34	1.5	1.38E-04

2. TMR-PLL Output Clock Integrity

The output clock integrity is only monitored during loss of lock events. As shown in Fig 6, the majority of the events shows less than 10% (50 MHz) frequency change (yellow) after loss-of-lock occurs (green). Two instances show more than 10% frequency change as shown in Fig 7. Finally, loss of output clock is shown in Fig 8.

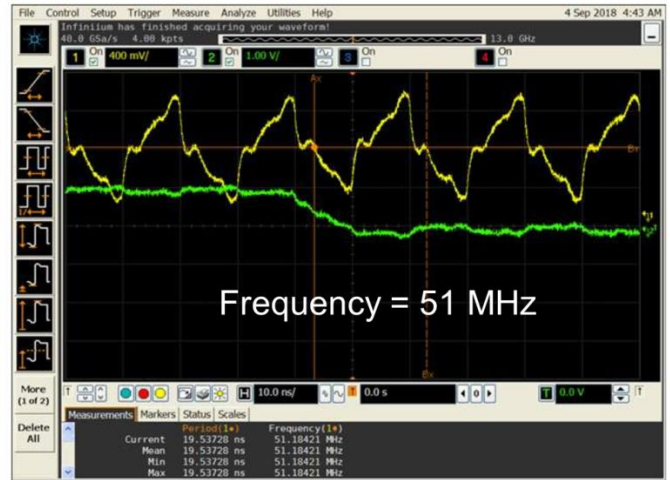
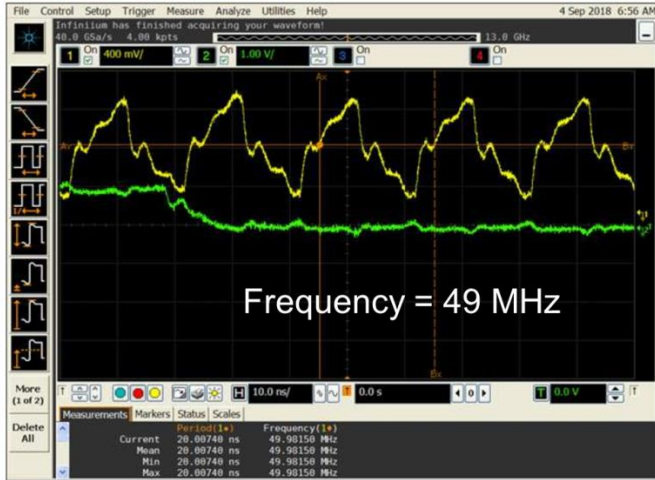


Fig 6. Clock output (yellow) frequency, triggered when loss-of-lock event occurs (green signal drops low). Two instances show less than 10% frequency change: 50 to 49 and 51 MHz.

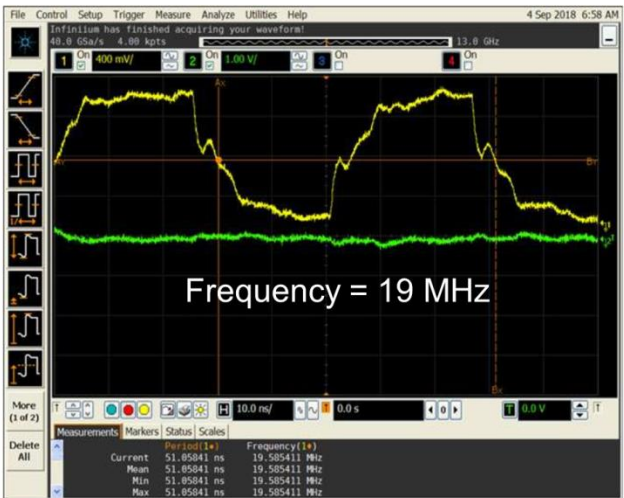
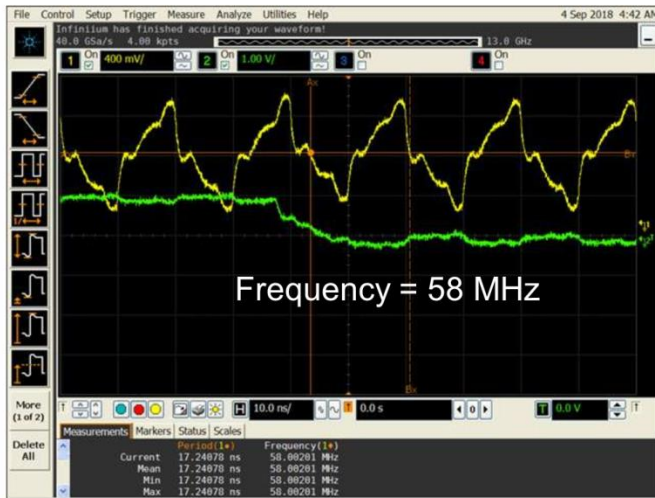


Fig 7. Clock output (yellow) frequency, triggered when loss-of-lock event occurs (green signal drops low). Two instances show more than 10% frequency change, from 50 to 58 and 19 MHz.

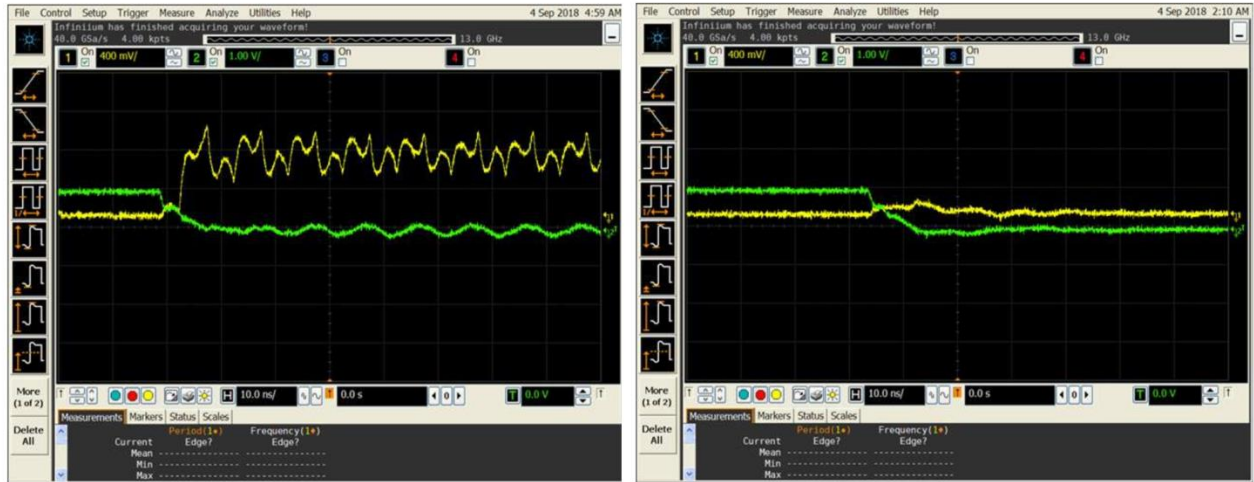


Fig 8. Clock output (yellow) frequency, triggered when loss-of-lock event occurs (green signal drops low). The two instances show a loss of output clock before loss-of-lock event occurred.

In conclusion, the output clock integrity during loss of lock events is unpredictable, however the majority of the events show less than 10% frequency change.

IV. Single-PLL

There are two modes of failure observed when testing the Single-PLL:

- 1) Loss-of-lock:
 - a. The output clock goes out of phase with respect to the input reference clock.
 - b. This mode of failure is self-recoverable (no reset is required for the output to be brought back into phase).
- 2) Loss-of-output:
 - a. The output of the PLL stops toggling and an asynchronous reset to the PLL is required to recover.
 - b. The output stopped toggling can be identified by a significant decrease in current across the chip as well as data stopped flopping through shift register chains.

Fig 9 shows the Single-PLL loss-of-lock and loss-of-output cross sections for different reference clocks: an external 20 MHz, external 50 MHz and on-chip 50 MHz oscillator. The results are consistent with previous Single-PLL using 20 MHz external clock as the reference, no significant difference between 50 MHz and 20 MHz external clock, especially at higher LETs. All loss-of-lock observed are self-recoverable and all loss-of-output can be recovered by a PLL reset or power cycle up to the maximum LET tested here of 46.4 MeV-cm²/mg. Tables 3-8 summarize the Weibull parameters.

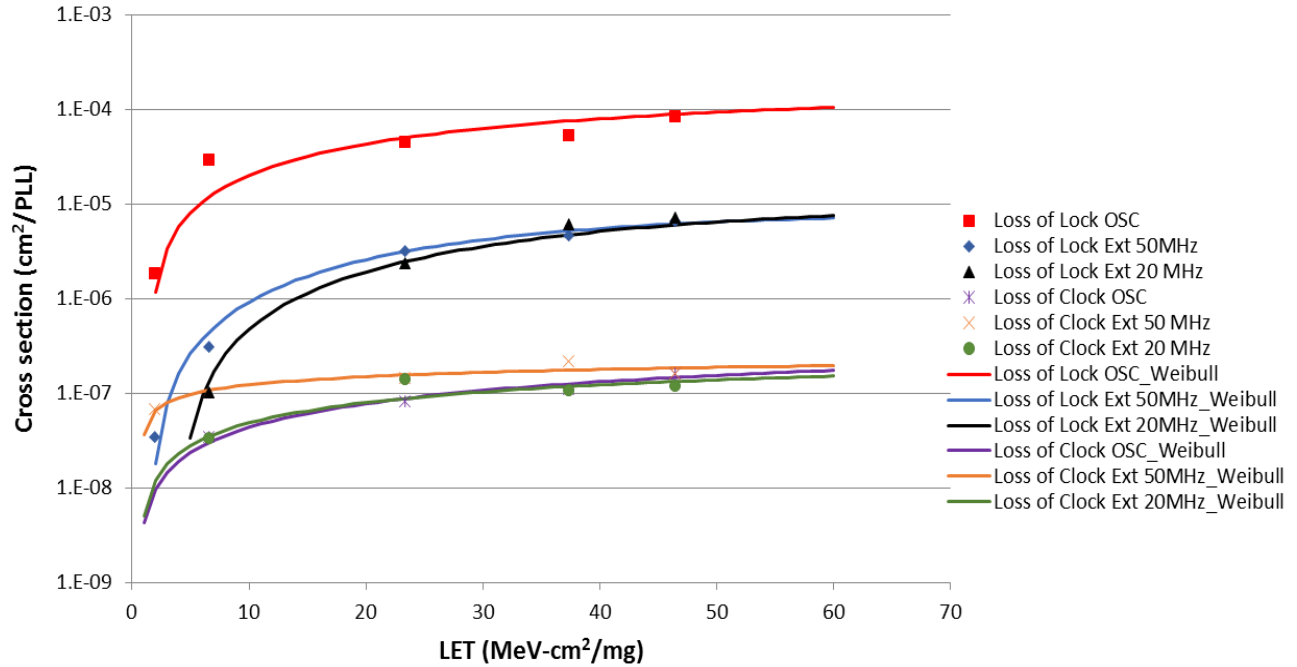


Fig 9. Single-PLL loss-of-lock and loss-of-output cross sections versus LET and Weibull curves for different reference clocks.

Table 3. Single-PLL Loss-of-Lock External 50 MHz Weibull Parameters

L0	W	S	A0
1.4	35	1.52	8.00E-06

Table 4. Single-PLL Loss-of-Lock External 20 MHz Weibull Parameters

L0	W	S	A0
4	45	1.5	1.00E-05

Table 5. Single-PLL Loss-of-Lock OSC 50 MHz Weibull Parameters

L0	W	S	A0
1.4	50	1.1	1.5E-04

Table 6. Single PLL Loss-of-Clock External 50 MHz Weibull Parameters

L0	W	S	A0
0.8	70	0.36	3.20E-07

Table 7. Single PLL Loss-of-Clock External 20 MHz Weibull Parameters

L0	W	S	A0
0.5	65	0.8	2.50E-07

Table 8. Single PLL Loss-of-Clock OSC 50 MHz Weibull Parameters

L0	W	S	A0
0.3	95	0.9	3.60E-07

3. POR Test

The POR test consists of performing 10 consecutive power cycles in-beam. The average flux is 46 ions/cm²/s and the LET is 37 MeV-cm²/mg. All 10 power cycles were successfully performed.

4. In-Beam Program-Verify

In-beam programming passed 2 out of 10 times. Standalone verify was performed after programming passed; all verify failed in-beam but passed off-beam. The results are summarized in Table 9.

Table 9. In-Beam Programming and Verify Summary

Attempt	1	2	3	4	5	6	7	8	9	10
Program	Fail	Fail	Fail	Pass	Fail	Fail	Fail	Pass	Fail	Fail
Verify				Fail (beam ON) Pass (beam OFF)	Pass	Pass	Pass	Fail (beam ON) Pass (beam OFF)	Pass	Pass

Please note that the in-beam program-verify test has also been performed in proton environment. In-beam programming passed 10 out of 10 times and after each programming success, a standalone verify was performed; all 10 out of 10 verify passed. The test and results will be published in a future report.

VI. ORBITAL UPSET RATE

The Weibull-fit parameters in Tables 1-8 are used to calculate the orbital upset rates in GEO-synchronous orbit, Solar-min, and 100 Mil aluminum shielding.

Table 10. Orbital Upset Rates

PLL Mode	GEO Solar Min Orbital Upset Rate	GEO Solar Min Orbital Upset Rate per year
50MHz External-Clock-PLL TMR Mode Reset Recoverable Upset Rate	5.26E-6 upset/PLL/day	1 loss of lock every 520 years
OSC-Clock-PLL TMR Mode Reset Recoverable Upset Rate	3.75E-4 upset/PLL/day	1 loss of lock every 7 years
20MHz External-Clock-PLL Single Instance Self-Recover Upset Rate	9.40E-6 upset/ PLL/day	1 loss of lock every 291 years
50MHz External-Clock-PLL Single Instance Self-Recover Upset Rate	1.97E-5 upset/ PLL/day	1 loss of lock every 139 years
OSC-Clock-PLL Single Instance Self-Recover Upset Rate	5.35E-4 upset/ PLL/day	1 loss of lock every 5 years
20MHz External-Clock-PLL Single Instance Loss of Output Upset Rate	2.21E-7 upset/ PLL/day	1 loss of output every 12,397 years
50MHz External-Clock-PLL Single Instance Loss of Output Upset Rate	1.08E-6 upset/ PLL/day	1 loss of output every 2,537 years
OSC-Clock-PLL Single Instance Loss of Output Upset Rate	2.21E-7 upset/ PLL/day	1 loss of output every 12,397 years

The two clock sources used during the PLL testing are not equivalent, the 20MHz and 50MHz external clocks were not irradiated, while the 50MHz on-chip Oscillator was irradiated. We are planning to test the radiation performance of the on-chip Oscillator on its own.

VII. REVISION HISTORY

2/27/2020 Initial version