# UG0811 User Guide SmartTime Static Timing Analyzer Libero SoC v12.1 and later

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# About SmartTime

SmartTime is the Libero SoC gate-level static timing analysis tool. With SmartTime, you can perform complete timing analysis of your design to ensure that you meet all timing constraints and that your design operates at the desired speed with the right amount of margin across all operating conditions.

Note: Creation and Editing of timing constraints are done in a separate Timing Constraints Editor. See the Timing Constraints Editor User Guide for help with creating and editing timing constraints.

### Static Timing Analysis (STA)

Static timing analysis (STA) offers an efficient technique for identifying timing violations in your design and ensuring that it meets all your timing requirements. You can communicate timing requirements and timing exceptions to the system by setting timing constraints. A static timing analysis tool will then check and report setup and hold violations as well as violations on specific path requirements.

STA is particularly well suited for traditional synchronous designs. The main advantage of STA is that unlike dynamic simulation, it does not require input vectors. It covers all possible paths in the design and does all the above with relatively low run-time requirements.

The major disadvantage of STA is that the STA tools do not automatically detect false paths in their algorithms as it reports all possible paths, including false paths, in the design. False paths are timing paths in the design that do not propagate a signal. To get a true and useful timing analysis, you need to identify those false paths, if any, as false path constraints to the STA tool and exclude them from timing considerations.

The SmartTime user interface provides efficient, user-friendly ways to define these critical false paths.

### **Timing Constraints**

SmartTime supports a range of timing constraints to provide useful analysis and efficient timing-driven layout.

### **Timing Analysis**

SmartTime provides a selection of analysis types that enable you to:

- · Find the minimum clock period/highest frequency that does not result in timing violations
- Identify paths with timing violations
- Analyze delays of paths that have no timing constraints
- Perform inter-clock domain timing verification
- · Perform maximum and minimum delay analysis for setup and hold checks

To improve the accuracy of the results, SmartTime evaluates clock skew during timing analysis by individually computing clock insertion delays for each register.

SmartTime checks the timing requirements for violations while evaluating timing exceptions (such as multicycle or false paths).

#### **SmartTime and Place and Route**

Because Libero SoC Place and Route uses SmartTime STA during timing-driven place-and-route in the background; your analysis and place and route constraints are always consistent.

#### **SmartTime and Timing Reports**

From SmartTime > Tools > Reports, the following report files can be generated:

- Timing Report (for both Max and Min Delay Analysis)
- Timing Violations Report (for both Max and Min Delay Analysis)
- Bottleneck Report
- Constraints Coverage Report



Combinational Loop Report

### **SmartTime and Cross-Probing into Chip Planner**

From SmartTime, you can select a design object and cross-probe the same design object in Chip Planner. Design objects that can be cross-probed from SmartTime to Chip Planner include:

- Ports
- Macros
- Timing Paths

### **SmartTime and Cross-Probing into Constraints Editor**

From SmartTime, you can cross-probe into the Constraints Editor. Select a Timing Path in SmartTime's Analysis View and add a Timing Exception Constraint (False Path, Multicycle Path, Max Delay, Min Delay). The Constraint Editor reflects the newly added timing exception constraint.

The Constraints Editor must be running for Cross-Probing to work.

#### See Also

Starting and Closing SmartTime Components of SmartTime Timing Analyzer Changing SmartTime Preferences

### **Design Flows with SmartTime**

You can access SmartTime in Libero SoC either implicitly or explicitly during the following phases of design implementation:

- During Place and Route When you select timing-driven place-and-route, SmartTime runs in the background to provide accurate timing information.
- After Place and Route Run SmartTime to perform post-layout timing analysis and adjust timing constraints. In the Libero SoC Design Flow window, expand Implement Design > Verify Post-Layout Implementation. You can:
  - Double-click Verify Timing to generate Timing Reports.
  - Right-click **Open SmartTime > Open Interactively** to run SmartTime.
- During Back-Annotation SmartTime runs in the background to generate the SDF file for timing simulation.

You can also run SmartTime whenever you need to generate timing reports, regardless of which design implementation phase you are in.

See Libero SoC User Guide for more information about Place and Route and Back-Annotation.

## Starting and Closing SmartTime

You must have completed Place and Route for your design before using SmartTime interactively. If your design has not yet been placed-and-routed, Libero SoC will complete that phase prior to starting SmartTime.

To open SmartTime interactively, in Implement Design > Verify Post Layout Implementation right-click Open SmartTime > Open Interactively.

SmartTime reads your design and displays post- or pre-layout timing information.

To close SmartTime, from the File menu, choose Exit.

### SmartTime Components

• The Maximum Delay Analysis View and the Minimum Delay Analysis View sour design



With SmartTime, you can:

- Browse through your design's various clock domains to examine the timing paths and identify those that violate your timing requirements
- Create customizable timing reports
- Navigate directly to the paths responsible for violating your timing requirements

# Setting SmartTime Options

You can modify SmartTime options for timing analysis by using the <u>SmartTime Options</u> dialog box.

#### To set SmartTime options:

From the SmartTime Maximum/Minimum Delay Analysis View window, choose Tools> Options.

The SmartTime Options dialog box has three categories: General, Analysis, and Advanced.

#### General

- 1. In the **General** category, select the settings for the operating conditions. SmartTime performs maximum or minimum delay analysis based on the Best, Typical, or Worst case.
- 2. Check or uncheck whether you want SmartTime to use inter-clock domains in calculations for timing analysis.
- 3. Click **Restore Defaults** only if you want the settings in the General pane to revert to their default settings.

#### Analysis

- 1. Click Analysis to display the options you can modify in the Analysis view.
- 2. Enter a number greater than 1 to specify the maximum number of paths to include in a path set during timing analysis.
- 3. Check or uncheck whether to filter the paths by slack value. If you check this box, you must then specify the slack range between minimum slack and maximum slack.
- 4. Check or uncheck whether to include clock network details.
- 5. Enter a number greater than 1 to specify the number of parallel paths in the expanded path.
- 6. Click **Restore Defaults** only if you want the settings in the Analysis View pane to revert to their default settings.

#### Advanced

- 1. Click Advanced to display advanced options.
- 2. Check or uncheck whether to use loopback in bidirectional buffers (bibufs) and/or break paths at asynchronous pins. Check or uncheck whether to disable non-unate arcs in the clock path.
- 3. Click Restore Defaults only if you want the settings in the Advanced pane to revert to their default settings.
- 4. Click OK.



Option Categories	General
<ul> <li>Select a category:</li> <li>General</li> </ul>	Operating Conditions
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	Clock Domains          Include inter-clock domains in calculations for timing analysis.         Include recovery and removal checks.
	Restore Defaults

Figure 1 · SmartTime Options Dialog Box – General Options for SmartFusion2, IGLOO2 and RTG4

Option Categories	General	
Select a category: General	Operating Conditions	
Analysis Advanced	Perform maximum delay analysis based on slow_lv_ht	▼ case
	Perform minimum delay analysis based on fast_hv_lt	▼ case
	Clock Domains	
	$\overrightarrow{\mathbf{v}}$ Include inter-clock domains in calculations for timing analysis.	
	Enable recovery and removal checks.	
		Restore Defaults

Figure 2 · SmartTime Options Dialog Box – General Options for PolarFire



Option Categories	Analysis View		
<ul> <li>Select a category: General</li> </ul>	Display of Paths		
Analysis	the time the subset of a state should be a sufficient to	100	
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	Filter the paths by slack value		
	Slack range from: ns	to:ns	
	$\overline{\left  \mathcal{Q} \right }$ Show dock network details in expanded path		
	Limit the number of parallel paths in expanded path to:	1	
		Restore Defaul	ts

Figure 3 · SmartTime Options Dialog Box – Analysis Options

Option Categories	Advanced		
<ul> <li>Select a category:</li> <li>General</li> <li>Analysis</li> <li>Advanced</li> </ul>	Special Situtations Use loopback in bi-directional buffers(bibufs)    Break paths at asynchronous pins   Disable non-unate arcs in dock network		
		Restore	Defaults

Figure 4 · SmartTime Options Dialog Box – Advanced Options

### See Also

SmartTime Options Dialog Box



# SmartTime Toolbar

The SmartTime toolbar contains commands for constraining or analyzing designs. Tool tips are available for each button.

lcon	Description
	Saves the changes
<u>1</u>	Undoes previous changes
2	Redoes previous changes
2	Opens the maximum delay analysis view
	Opens the minimum delay analysis view
<b>(10)</b>	Opens the manage clock domains manager
K	Opens the path set manager
8	Recalculates all

Table 1 · SmartTime Toolbar



# **SmartTime Timing Analyzer**

## SmartTime Timing Analyzer

The SmartTime Timing Analyzer is an interactive Static Timing Analysis tool. Click Open SmartTime in the Design Flow Window to invoke the SmartTime Timing Analyzer (**Design Flow Window > Open SmartTime > Open** Interactively).

# Components of the SmartTime Timing Analyzer

Use the SmartTime Timing Analyzer to visualize and identify timing issues in your design for the selected scenario. In this view, you can evaluate how far you are from meeting your timing requirements, create custom sets to track, set timing exceptions to obtain timing closure, and cross-probe paths with other tools.

The timing analysis view includes:

- Domain Browser: Enables you to perform your timing analysis on a per domain basis.
- Path List: Displays paths in a specific set in a given domain sorted by slack.
- Path Details: Displays detailed timing analysis of a selected path in the paths list.
- Analysis View Filter: Enables you to filter the content of the paths list.
- Path Slack Histogram: When a set is selected in the Domain Browser, the Path Slack Histogram displays a distribution of the path slacks for that set. Selecting one or multiple bars in the Path Slack Histogram filters the paths displayed in the Path List.

You can copy, change the resolution and the number of bars of the chart from the right-click menu.

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Figure 5 · SmartTime Timing Analyzer Components

## Analyzing Your Design

The timing engine uses the following priorities when analyzing paths and calculating slack:

- 1. False path
- 2. Max/Min delay
- 3. Multi-cycle path



#### 4. Clock

If multiple constraints of the same priority apply to a path, the timing engine uses the tightest constraint. You can perform two types of timing analysis: Maximum Delay Analysis and Minimum Delay Analysis.

#### To perform the basic timing analysis:

- 1. Open the Timing Analysis View using one of the following methods:
  - From the SmartTime **Tools** menu, choose **Timing Maximum Delay Analysis** or **Minimum Delay Analysis**.
  - Click the kinetic on for Maximum Delay Analysis or the kinetic on for Minimum Delay Analysis from the SmartTime window.
- Note: When you open the Timing Analyzer from Designer, the Maximum Delay Analysis window is displayed by default.

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		01 NF 161 K - dock reconvergence positivism 04 NF 160	Library setup time							

Figure 6 · Maximum Delay Analysis View

- 2. In the Domain Browser, select the clock domain. Clock domains with a vindicate that the timing requirements in these domains were met. Clock domains with an x indicate that there are violations within these domains. The Paths List displays the timing paths sorted by slack. The path with the lowest slack (biggest violation) is at the top of the list.
- 3. Select the path to view. The Path Details below the Paths List displays detailed information on how the slack was computed by detailing the arrival time and required time calculation. When a path is violated, the slack is negative and is displayed in red color.
- 4. Double-click the path to display a separate view that includes the path details and schematic.
- Note: In cases where the minimum pulse width of one element on the critical path limits the maximum frequency for the clock, SmartTime displays an icon for the clock name in the Summary List. Click on the icon to display the name of the pin that limits the clock frequency.
- 5. Repeat the above steps as required.

## Managing Clock Domains

In SmartTime, timing paths are organized by clock domains. By default, SmartTime displays domains with explicit clocks. Each clock domain includes at least three path sets:

- Register to Register
- External Setup (in the Maximum Analysis View) or External Hold (in the Minimum Analysis View)
- Clock to Out

You must select a path set to display a list of paths in that specific set.

#### To manage the clock domains:

1. Right-click anywhere in the Domain Browser, and choose **Manage Clock Domains**. The <u>Manage Clock</u> <u>Domains</u> dialog box appears (as shown below).



Tip: You can click the icon in the SmartTime window bar to display the Manage Clock Domains dialog box.

DQS[2]	^	Add	DQS[0]	
PLL_REF_CLK ddr_x32_0/CCC_0/pll_inst_0/OUT1	100		DQS[1] DQS[3]	
ddr_x32_0/CCC_0/pll_inst_0/OUT2		Move Down	The second second second	PHY_BLK_0/IOD_TRAINING_0/CC
ddr_x32_0/CCC_0/pll_inst_0/OUT3 ddr_x32_0/DDRPHY_BLK_0/IOD_TRAINING_0				
ddr_x32_0/DDRPHY_BLK_0/IOD_TRAINING_0		Move Up		
ddr_x32_0/DDRPHY_BLK_0/IOD_TRAINING_0 ddr_x32_0/DDRPHY_BLK_0/IOD_TRAINING_0				
ddr_x32_0/DDRPHY_BLK_0/IOD_TRAINING_0 ddr_x32_0/DDRPHY_BLK_0/IOD_TRAINING_0		Remove		
< >			<	>

Figure 7 · Manage Clock Domains Dialog Box

2. To add a new domain, select a clock domain from the **Available clock domains** list, and click **Add**. To add a non-explicit clock domain, click **New Clock**.

The Choose the Clock Source Pin dialog box opens, and you can select the clock source pin. You can choose to filter the available pins and search.



Filter available pins :	1. 	
Type :	Pattern :	
Clock Network	• •	Search
earch Results :		
CCC_0/clkint_0/U0_RGB1:A		-
CCC_0/clkint_0/U0_RGB1:Y		
CCC_0/clkint_0/U0_RGB1:Y.1		
CCC_0/clkint_0/U0_RGB1:Y.2		
CCC_0/clkint_0/U0_RGB1:Y.3		
CCC_0/clkint_0/U0_RGB1:Y.4		
CCC_0/clkint_0/U0_RGB1:Y.5		
CCC_0/clkint_0/U0_RGB1:Y.6		
CCC_0/clkint_0:A		
CCC_0/clkint_0:Y.2		
CCC_0/clkint_0:Y.3		
CCC_0/clkint_0:Y.4		
CCC_0/clkint_0:Y.5		
CCC_0/clkint_0:Y.6		
CCC_0/clkint_0_1:A		
CCC_0/clkint_0_1:Y		
DDR4_0/CCC_0/clkint_4/U0_RGB1:A		
•		•

Figure 8 · Choose Clock Source Pin Dialog Box

- 4. To remove a displayed domain, select a clock domain from the **Show the clock domains in this order** list, and click **Remove**.
- 5. To change the display order in the Domain Browser, select a clock domain from the **Show the clock** domains in this order list, and then use the **Move Up** or **Move Down** to change the order in the list.
- 6. Click **OK**. SmartTime updates the Domain Browser based on your specifications. If you have added a new clock domain, then it will include at least the three path sets as mentioned above.

#### See Also

Manage Clock Domains Dialog Box

# **Managing Path Sets**

You can create and manage custom path sets for timing analysis and tracking purposes. Path sets are displayed under the **Custom Path Sets** at the bottom of the Domain Browser.

#### To add a new path set:

- 1. Right-click anywhere in the Domain Browser, and choose **Add Set**. The <u>Add Path Analysis Set Dialog Box</u> appears (as shown below).
  - Tip: You can click the icon in the SmartTime window bar to display the Add Path Analysis Set dialog box.



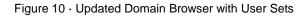
Add Path Analysis Set	8
lame :-	Trace from :- 📀 Source to sink 🗢 Sink to source
Source pins:	Sink Pins:
DFN1_0:CLK DFN1_1:CLK PF_CCC_C0_0/PF_CCC_C0_0/pll_inst_0:R	EF_CLK_0
Select All	Select All
Filter source pins:	Filter sink pins:
Pin Type: Registers by pin names	Pin Type: Registers by pin names      Filter
*	Filter Filter

Figure 9 · Add Path Analysis Set Dialog Box

- 2. Enter a name for the path set.
- 3. Select the source and sink pins. You can <u>use the filters</u> to control the type of pins displayed.
- 4. Click **OK**. The new path set appears under **User Sets** in the Domain Browser (as shown below).



e Edit View Tools Help					
m Delay Analysis View					
Analysis for scenario timing_analysis	From *	то (*			
ddr_x32_0/DDRPHY_BLK_0/LANE_3_CTR      Register     to Register	Customize table	Apply Filter	Store Filter	r Reset Filte	er
External Setup Clock to Output Register to Asynchronous	Source Pin	Sink Pin		ack ns)	
External Recovery Asynchronous to Register ddr_x32_0/CCC_0/pll_inst_0/OUT1 to ddr	1 CoreAXI4Interconnect_0/Ms Cor	reAXI4Interconnect_0/ax	0.958	4.952	
ddr_x32_0/DDRPHY_BLK_0/LANE_3_CTR Register to Register External Setup	Name Summary				1
Clock to Output Register to Asynchronous External Recovery	data required time data arrival time				
Asynchronous to Register ddr_x32_0/CCC_0/pll_inst_0/OUT1 to ddr	slack Data_arrival_time_calculation ddr_x32_0/CCC_0/pll_inst_0 ddr_x32_0/CCC_0/pll_inst_0	0/OUT1			
8	ddr_x32_0/CCC_0/clkint_4_ ddr_x32_0/CCC_0/clkint_4_	1:A			
2.952 3.952 4.952 5.952 6.952	ddr x32 0/CCC 0/clkint 4/				3



#### To remove an existing path set:

- 1. Select the path set from the User Sets in the Domain Browser.
- 2. Right-click the set to delete, and then choose Delete Set from the right-click menu.

#### To rename an existing path set:

- 1. Select the path set from **User Set** in the Domain Browser.
- 2. Right-click the set to rename, and then choose Rename Set from the right-click menu.
- 3. Edit the name directly in the Domain Browser.

#### See Also

Add Path Analysis Set Dialog Box Using Filters

# **Displaying Path List Timing Information**

The Path List in the Timing Analysis View displays the timing information required to verify the timing requirements and identify violating paths. The Path List is organized in a grid where each row represents a timing path with the corresponding timing information displayed in columns. Timing information is customizable; you can add or remove columns for each type of set.

By default, each type of set displays a subset of columns as follows:

- Register to Register: Source Pin, Sink Pin, Delay, Slack, Arrival, Required, Setup, Minimum Period, and Skew.
- External Setup: Source Pin, Sink Pin, Delay, Slack, Arrival, Required, Setup, and External Setup.
- Clock to Out: Source Pin, Sink Pin, Delay, Slack, Arrival, Required, and Clock to Out.
- Input to Output: Source Pin, Sink Pin, Delay, and Slack.
- Custom Path Sets: Source Pin, Sink Pin, Delay, and Slack.

You can add the following columns for each type of set:



- Register to Register: Clock, Source Clock Edge, Destination Clock Edge, Logic Stage Count, Max Fanout, Clock Constraint, Maximum Delay Constraint, and Multicycle Constraint.
- External Setup: Clock, Destination Clock Edge, Logic Stage Count, Max Fanout, Clock Constraint, Input Delay Constraint, Required External Setup, Maximum Delay Constraint, and Multicycle Constraint.
- Clock to Out: Clock, Source Clock Edge, Logic Stage Count, Max Fanout, Clock Constraint, Output Delay Constraint, Required Maximum Clock to Out, Maximum Delay Constraint, and Multicycle Constraint.
- Input to Output: Arrival, Required, Setup, Hold, Logic Stage Count, and Max Fanout.
- Custom Path Sets.

#### To customize the set of timing information in the Path List:

- 1. Select the set to customize.
- 2. Choose **Customize table** on the top left corner of path list to open the <u>Customize Paths List Table</u> dialog box.
- 3. To add one or more columns, select the fields to add from the Available fields list, and click Add.

Source Pin	Add	Arrival (ns)	
Sink Pin Delay		Required (ns) Setup (ns)	
(ns)	Move Down	Recovery (ns)	
Slack (ns)		External Setup (ns) External Recovery (ns)	
	Move Up	Logic Stage Count	
	Remove		

Figure 11 · Customize Paths List Table Dialog Box

- 4. To remove one or more columns, select the fields to remove from the **Show these fields in this order** list, and click **Remove**.
- 5. To change the order in which the fields appear, select fields in the **Show these fields in this order** list and click **Move Up** or **Move Down**.
- 6. Click **OK** to add or remove the selected columns. SmartTime updates the Timing Analysis View.

#### See Also

Customize Analysis View



# Displaying Expanded Path Timing Information

SmartTime displays the list of paths and the path details for all parallel paths.

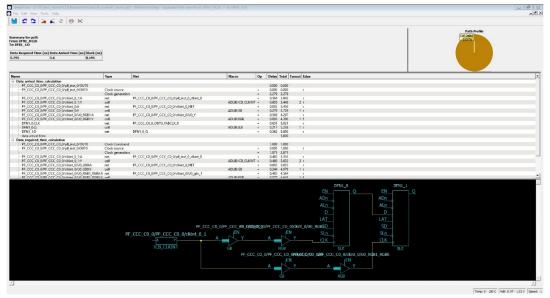
Analysis for scenario bining_analysis														
n.a	From *							то *						
Summary     Very PF_CCC_C0_0/PF_CCC_C0_0/pill	ut_0/0U Customize table													v Filter   Store Filter   Reset Filte
External Setup Clock to Output	CLISION OF GODE													Sole Plat Indec Plat
Register to Asynchronous External Recovery Asynchronous to Register	Setup (ns	) Minimum Period (ns)	Delay (ns)	Slack	(ns)	Sink Pin	Multicycle Constraint	estination Clock Ed	ax Delay	y Constraint (r	Clock Constrain	t (ns) Required (ns)		Logic Stage Count
REF_CLK_0	1 0.000	0.805 0.579		195	D	FN1_1:D		Rising			1.000	5.795	0	
Register to Register     External Setup     Clock to Output     Register to Asynchronous     Etlemal Recovery     Asynchronous to Register														
Pin to Pin	Name		Type	1	Vet			Macro	Op	Delay To	tal Fanout Ed	je		
- Input to Output	Summary													
X User Sets	data require data arrival									2	795 600			
	- deta amvel	time								2.	195			
	Data arrival ti	me calculation									190			
		0/PF_CCC_C0_0/pll_inst_0/0UT0								0.000 0.	000			
	- PF_CCC_C0	0/PF CCC C0 0/pll inst 0:0UT0	Clack sou	arce						0.000 0.	000 r			
1			Clock get							2.279 2.	279			
	- PF_CCC_C0	0/PF_CCC_C0_0/cRint_0_1:A	net	P	PF_CCC_C0_0	/PF_CCC_C0_0/pl	_inst_0_clkint_0		+	0.564 2.				
		0/PF_CCC_C0_0/clkint_0_1:Y	cell					ADUB/CB_CI		0.605 3.				
	- PF_CCC_C0	0/PF_CCC_C0_0/clkint_0.A	net	F	PF_CCC_C0_0	PF_CCC_C0_0/d	kint_0_NET			0.002 3.				
	PF_CCC_C0	0/PF_CCC_C0_0/clkint_0.Y	cell					ADLIB:GB		0.279 3.	729 1 r			
	- PF_CCC_CO	0/PF_CCC_C0_0/clkint_0/U0_RGB1A 0/PF_CCC_C0_0/clkint_0/U0_RGB1Y	cell		*_CCC_C0_0	PF_CCC_C0_0/d	kint_0/00_Y	ADUB:RGB	•	0.568 4.	297 r 390 1 f			
	DFN1_0:CU	UPPF CCC CU OPPRIANT OVDU RGB1:Y	cen			OUTO_FABCLK_C		ADUE:KGB		0.631 5				
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	Data_required	time_calculation												
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	PF_CCC_C0	0/PF_CCC_C0_0/pll_inst_0:OUT0	Clock sou							0.000 1.				
			Clock get							1.871 2.	871			
		0/PF_CCC_C0_0/clkint_0_1:A	net	F	*_CCC_C0_0	/PF_CCC_C0_0/pl	anst_0_clkint_0	10110-100 01		0.482 3.				
	PF_CCC_CC	0/PF_CCC_C0_0/clkint_0_1:Y 0/PF_CCC_C0_0/clkint_0/U0_GB0A	cell			PF_CCC_C0_0/d	In O ANT	ADUB/ICB_CI	KINT +	0.480 3.	833 2 r 835 r			
		0/PF_CCC_C0_0/clkint_0/U0_GB0X	cell		*	PPF_CCC_C0_0/d	OUT OTHER	ADUB:G8		0.244 4	850 f			
1	- PF CCC CD	0/PF_CCC_C0_0/clkint_0/U0_RGB1_R	680.A net			PF_CCC_C0_0/d	kint 0/00 abs 1	100000		0.485 4.	964 r			
	PF CCC CC	0/PF_CCC_C0_0/clkint_0/U0_RGB1_R	GBO.Y cell				and a subject of	ADUB:RGB		0.077 4				
	DFN1_1:CL	ĸ	net	F	F CCC CD 0	IPF_CCC_C0_0/d	kint_0/U0_RGB1_RGB0_rg			0.539 5.	180 r			
	- clock recon	wergence pessimism							+	0.615 5.				
	DFN1_1:D		Library se	tup time				ADUB:SLE	-		795			
	- data require	ed time								2	795			
0														
-0.805 0 0.195 1.1	5 2.195													

Figure 12 · Path List View

The Path List displays all parallel paths in your design. The Path Details grid displays the path details for all parallel paths.

#### To display the Expanded Path View:

From the Path List: double-click the path, or right-click a path and select **expand selected paths**. From the Expanded Path View: double-click the path, or right-click the path and select **expand path**.



#### Figure 13 · Expanded Path View

The Expanded Path Summary provides a summary of all parallel paths for the selected path. The Path Profile chart displays the percentage of time taken by cells and nets for the selected path. If no parallel path is selected in this view, the Path Profile shows the percentage for all paths. By default, SmartTime only shows one path for each Expanded Path. You can change this default in the <u>SmartTime Options</u> dialog box.

The Expanded Path View also includes a schematic of the path and a path profile chart for the paths selected in the Expanded Path Summary.



# **Using Filters**

You can use filters in SmartTime to limit the Path List content (that is, create a filtered list on the source and sink pin names). The filtering options appear on the top of the Timing Analysis View. You can save these filters one level below the set under which it has been created.

#### To use the filter:

- 1. Select a set in the Domain Browser to display a given number of paths, depending on your <u>SmartTime</u> <u>Options</u> settings (100 paths by default).
- 2. Enter the filter criteria in both the **From** and **To** fields and click **Apply Filter**. This limits the display to the paths that match your filter criteria.

From *	TO *		
Customize table	Apply Filter	Store Filter	Reset Filter

Figure 14 · Maximum Delay Analysis View

3. Click **Store Filter** to save your filter criteria with a special name. The **Create Filter Set** dialog box appears (as shown below).

	? <mark>×</mark>
ОК	Cancel
	ОК

Figure 15 · Create Filter Set Dialog Box

4. Enter a name for the filter, such as myfilter01, and click **OK**. Your new filter name appears below the set under which it was created.



laximum Delay Analysis View	_								
Analysis for scenario Primary									
🔺 💩 Summary	]								
⊿ v@ my_clk									
Register to Register									
my_filter01									
External Setup									
Clock to Output									
Register to Asynchronous	1								
External Recovery	I								
Asynchronous to Register	1								
4 🦐 Pin to Pin									
Input to Output									
4 ភ User Sets	1								
my_set	1								
	1								

Figure 16 · my\_filter01

num Delay Analysis View				
Analysis for scenario timing, analysis				
MAX Uning_analysis	From *	то *		
ි හි Summary				
	Customize table	Apply Fi	ter Store Filter	Reset Filter
× Register to Register				
External Setup Clock to Output		1		
Register to Asynchronous	Setup Minimum Delay (ns) Period (ns) (ns)	Slack	Sink Pin	
External Recovery		(ns)		
Asynchronous to Register	1 0.000 0.448 0.434	-0.348 DFN1_1:D		
🗏 🌫 Pin to Pin				
Input to Output	<			,
St. User Sets	Name	Type Net	Macro Op	Delay ^
	Summary			
	data required time			
	data arrival time			
3	slack			
	Data_arrival_time_calculation CLK			0.000
	CLK	Clock source		0.000
	CLK_ibuf/U_IOPAD:PAD	net CLK	1	0.000
2	CLK_ibuf/U_IOPAD:Y	cell	ADLIB:IOPAD_IN +	1.726
	CLK_ibuf/U_IOIN:YIN	net CLK_ibuf/YIN	+	0.000
	CLK_ibuf/U_IOIN:Y	cell	ADLIB:IOIN_IB_E +	0.409
	CLK_ibuf_RNIVQ04:A	net CLK_ibuf_Z	+	2.067
	CLK_ibuf_RNIVQ04:Y	cell	ADLIB:GB +	0.224
	CLK_ibuf_RNIVQ04/U0_RGB1:A	net CLK_ibuf_RNIVQ04/U0_1		0.662
	CLK_ibuf_RNIVQ04/U0_RGB1:Y	cell	ADLIB:RGB +	0.110
	DFN1_0:CLK	net CLK_c cell	+ ADLIB:SLE +	0.741
	DFN1_0:Q DFN1_1:D	net DEN1 0 O	ADLIB:SLE +	0.236
	V K	Driviou		>

Figure 17 · Updated Maximum Delay Analysis View

Repeat the above steps and cascade as many sets as you need using the filtering mechanism.



#### To remove a set created with filters:

- 1. Select the set that uses filters.
- 2. Right-click the set, and choose **Delete Set** from the shortcut menu.

#### To rename a set created with filters:

- 1. Select the set that uses filters.
- 2. Right-click the set, and choose **Rename Set** from the shortcut menu.
- 3. Edit the name directly in the Domain Browser.

#### To edit a specific filter in the set:

- 1. Select the filter to edit.
- 2. Right-click the filter, and choose Edit Set from the shortcut menu.

#### See Also

SmartTime Options Store Filter as Analysis Set Edit Set dialog box



# **Advanced Timing Analysis**

# **Understanding Inter-Clock Domain Analysis**

When functional paths exist across two clock domains (the register launching the data and the one capturing it are clocked by two different clock sources), you must provide accurate specification of both clocks to allow a valid inter-clock domain timing check. This is important especially when the clocks are specified with different waveforms and frequencies.

When you specify multiple clocks in your design, the first step is to consider whether the inter-clock domain paths are false or functional. If these paths are functional, then you must perform setup and hold checks between the clock domains in SmartTime. Unless specified otherwise, SmartTime considers the inter-clock domain as false, and therefore does not perform setup or hold checks between the clock domains.

If you have several clock domains that are subset of a single clock (such as if you want to measure clock tree delay from an input clock to a generated clock), you must configure Generated Clock Constraints for each of the clock domains in order for SmartTime to do execute the calculation and show timing for each of the inter-clock-domain paths.

Once you include the inter-clock domains for timing analysis, SmartTime analyzes for each inter-clock domain the relationship between all the active clock edges over a common period equal to the least common multiple of the two clock periods. The new common period represents a full repeating cycle (or pattern) of the two clock waveforms (as shown below).

For setup check, SmartTime considers the tightest relation launch-capture to ensure that the data arrives before the capture edge. The hold check verifies that a setup relationship is not overwritten by a following data launch.

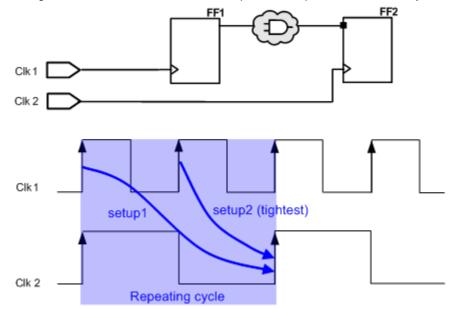


Figure 18 · Example Showing Inter-Clock Domains

#### See Also

Activating inter-clock domain analysis Deactivating a specific inter-clock domain Displaying inter-clock domain paths

# Activating Inter-Clock Domain Analysis

#### To activate the inter-clock domain checking:

- 1. In SmartTime, from the **Tools** menu choose **Options**. The <u>SmartTime Options Dialog Box</u> dialog box appears (as shown below).
- 2. In the general category, check the Include inter-clock domains in calculations for timing analysis.

SmartTime Options		? <b>×</b>
Option Categories Select a category: General Analysis Advanced	General Operating Conditions Perform maximum delay analysis based on WORST Perform minimum delay analysis based on BEST Clock Domains ✓ Include inter-clock domains in calculations for timing analysis ✓ Enable recovery and removal checks.	case  case  Restore Defaults
Help		OK Cancel

Figure 19 · SmartTime Options Dialog Box for SmartFusion2, RTG4 and IGLOO2

Option Categories	General
Select a category: General	Operating Conditions
Analysis Advanced	Perform maximum delay analysis based on slow_lv_ht case
	Perform minimum delay analysis based on fast_hv_lt case
	Clock Domains
	Include inter-clock domains in calculations for timing analysis.
	₩ Enable recovery and removal checks.
	Restore Defaults

Figure 20 · SmartTime Options Dialog Box for PolarFire

3. Click **OK** to save the dialog box settings.



#### See Also

Inter-Clock Domain Analysis Deactivating a Specific Inter-Clock Domain Displaying Inter-Clock Domain Paths

# **Displaying Inter-Clock Domain Paths**

Once you <u>activate the inter-clock domain checking</u> for a given clock domain CK1, SmartTime automatically detects all other domains CKn with paths ending at CK1. SmartTime creates inter-clock domain sets CKn to CK1 under the domain CK1. Each of these sets enables you to display the inter-clock domain paths between a given clock domain and CK1.

#### To display an inter-clock domain set:

- 1. Expand the receiving clock domain of the inter-clock domain in the Domain Browser to display its related sets. For the inter-clock domain CK1 to CK2, expand clock domain CK2.
- 2. Select the inter-clock domain that you want to see expanded from these sets. Once selected, all paths between the related two domains are displayed in Paths List in the same way as any register to register set.

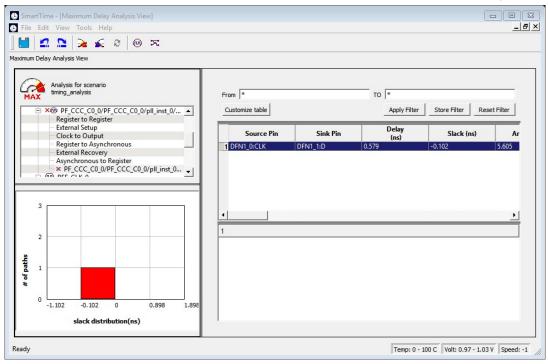


Figure 21 · Maximum Delay Analysis View

#### See Also

Understanding inter-clock domain analysis Activating inter-clock domain analysis Deactivating a specific inter-clock domain



# Deactivating a Specific Inter-Clock Domain

To deactivate the inter-clock domain checking for the specific clock domains clk2->clk1, without disabling this option for the other clock domains:

- 1. From the **Tools** menu, choose **Constraints Editor > Primary Scenario** to open the Constraints Editor View.
- In the Constraints Browser, double-click False Path under Exceptions. The "Set False Path Constraint dialog box appears.
- 3. Click the **Browse** button to the right of the **From** text box. The **Select Source Pins for False Path Constraint** dialog box appears.
- 4. For Specify pins, select by keyword and wildcard.
- 5. For Pin Type, select Registers by clock names from the Pin Type drop-down list.
- 6. Type the inter-clock domain name, for example Clk2 in the filter box and click Filter.
- 7. Click **OK** to begin filtering the pins by your criteria. In this example, [get\_clocks {Clk2}] appears in the **From** text box in the **Set False Path Constraint** dialog box.
- 8. Repeat steps 3 to 7 for the **To** option in the <u>Set False Path Constraint</u> dialog box, and type Clk2 in the filter box.
- 9. Click OK to validate the new false path and display it in the Paths List of the Constraints Editor.
- 10. Click the Recalculate All icon 🖾 in the toolbar.
- 11. Select the inter-clock domain set clk2 -> clk1 in the Domain Browser (as shown below).
- 12. Verify that the set does not contain any paths.

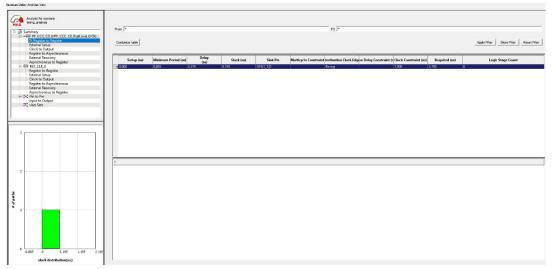


Figure 22 · Maximum Delay Analysis View

#### See Also

Understanding inter-clock domain analysis Activating inter-clock domain analysis Displaying inter-clock domain paths Select Source or Destination Pins for Constraint dialog box

Set False Path Constraint dialog box

# **Changing Output Port Capacitance**

Output propagation delay is affected by both the capacitive loading on the board and the I/O standard. The I/O Attribute Editor in ChipPlanner provides a mechanism for setting the expected capacitance to improve the propagation delay model. SmartTime automatically uses the modified delay model for delay calculations.

To change the output port capacitance and view the effect of this change in SmartTime Timing Analyzer, refer to the following example. The figure below shows the delay from DFN1 to output port Q. It shows a delay of 6.603 ns based on the default loading of 5 pF.

	x 🐵 S 🏂 🗲 🚨									
um Del	ay Analysis View	au .								
AX	Analysis for scenario timing_analysis	From *				TO *				
	External Recovery Asynchronous to Register	Customize table						Apply Filter	Store Filter	Reset Filter
~ .	FCCC_C0_0/FCCC_C0_0/CCC_INST/GL1     Register to Register     External Setup	Source Pin	Sink Pin	Delay (ns)	Slack (ns)	Arrival (ns)	Required (ns)	Clock to	Out (ns)	
	Clock to Output Register to Asynchronous	1 DFN1_1:CLK	0	5.251		10.442			10	0.442
		Name		Туре		Net			Macro	10
		✓ Summary data required time data arrival time		Туре		Net			Macro	
	This set has no path.	Summary data required time data arrival time slack V Data_arrival time_calcu FCCC_C0_0/FCCC_C0		:GL1 Clock					Macro	
	This set has no path.	<ul> <li>Summary data required time data arrival time slack</li> <li>Data_arrival_time_calcul FCCC_C0_0/FCCC_C0</li> </ul>	)_0/CCC_INST/GL1 )_0/CCC_INST/INST_CCC_IP	GL1 Clock	source generatio	on			Macro	
	This set has no path.	Summary data required time data arrival time slack V Data_arrival time_calcu FCCC_C0_0/FCCC_C0	)_0/CCC_INST/GL1 )_0/CCC_INST/INST_CCC_IP )_0/GL1_INST:An	:GL1 Clock		on	0_0/FCCC_C0_0	/GL1_net	Macro	

Figure 23 · Maximum Delay Analysis View

If your board has output capacitance of 15 pf on Q, you must perform the following steps to update the timing number:

1. Open the I/O Attribute Editor and change the output load to 15 pf.

		view/12.0_Release/94609	/ccc2 (t	op)										-		×
File E	dit View Logic 1	Tools Help Hierarchical NLV	Flat NLV	* * 🧔		ð	B () ()									
Main Obje	ect Browser	đ×	Port	: View [active] 🛛 🗗	Pin Vi	ew	🗗 Package V	liew	8 Floorplan	ner Vi	ew 8	•	Properties			80
				Port Name	1 Slew	•	Pre-Emphasis 💌	0.	utput Drive (mA)	•	Output Load (pF)	•	Port Name:	Q		
>	Ports I/O Ports	d 🕼 🥑 1	2	D	**								Macro: Type:	100	_obuf D, Single	-ended
			3	Q	SLOW				4		15		Placed: Pin: 1/0 Standa: 1/0 Bank:	B2 rd: LV Ba		ORIO

Figure 24 · I/O Attribute Editor View

- 2. Select File > Save.
- 3. Select **File > Close**.
- 4. Open the SmartTime Timing Analyzer.

You can see that the Clock to Output delay changed to 5.952 ns.



# **Generating Timing Reports**

# **Types of Reports**

Using SmartTime you can generate the following types of reports:

- **Timer report** This report displays the timing information organized by clock domain.
- **Timing Violations report** This flat slack report provides information about constraint violations.
- **Bottleneck report** This report displays the points in the design that contribute to the most timing violations.
- Datasheet report This report describes the characteristics of the pins, I/O technologies, and timing
  properties in the design.
- **Constraints Coverage report** This report displays the overall coverage of the timing constraints set on the current design.
- Combinational Loop report This report displays loops found during initialization.

#### See Also

Generating a Timing Report Generating a Timing Violation Report Generating a datasheet report Generating a bottleneck report Generating a constraints coverage report Generating a Combinational Loop Report

## Generating a Timing Report

The timing report enables you to quickly determine if any timing problems exist in your design. The Maximum Delay Analysis timing report lists the following information about your design:

- Maximum delay from input I/O to output I/O
- Maximum delay from input I/O to internal registers
- Maximum delay from internal registers to output I/O
- Maximum delays for each clock network
- · Maximum delays for interactions between clock networks

#### To generate a timing report:

- From the SmartTime Max/Min Delay Analysis View, choose Tools > Reports > Timer. The <u>Timing Report</u> <u>Options Dialog Box</u> appears.
- 2. Select the options you want to include in the report, and then click OK.

The timing report appears in a separate window.

#### See Also

<u>Understanding Timing Reports</u> <u>Timing Report Options Dialog Box</u>



# **Understanding Timing Reports**

The timing report contains the following sections:

### Header

The header lists:

- The report type
- The version of Designer used to generate the report
- The date and time the report was generated
- General design information (name, family, etc.)

### Summary

The summary section reports the timing information for each clock domain.

By default, the clock domains reported are the explicit clock domains that are shown in SmartTime. You can filter the domains and get only specific sections in the report (see <u>Timing Report Options Dialog Box</u>).

### **Path Sections**

The paths section lists the timing information for different types of paths in the design. This section is reported by default. You can deselect this option in the <u>Timing Report Options Dialog Box</u>.

By default, the number of paths displayed per set is 5.

You can filter the domains using the Timing Report Options dialog box.

You can also view the stored filter sets in the generated report using the timing report options. The filter sets are listed by name in their appropriate section, and the number of paths reported for the filter set is the same as for the main sets.

By default, the filter sets are not reported.

### **Clock domains**

The paths are organized by clock domain.

### **Register to Register set**

This set reports the paths from the registers clock pins to the registers data pins in the current clock domain.

### **External Setup set**

This set reports the paths from the top level design input ports to the registers in the current clock domain.

### **Clock to output set**

This set reports the paths from the registers clock pins to the top level design output ports in the current clock domain.

### **Register to Asynchronous set**

This set reports the paths from registers to asynchronous control signals (like asynchronous set/reset).

### **External Recovery set**

This set reports the external recovery check timing for asynchronous control signals (like asynchronous set/reset).

### Asynchronous to Register set

This set reports the paths from asynchronous control signals (like asynchronous set/reset) to registers.



### Inter-clock domain

This set reports the paths from the registers clock pins of the specified clock domain to the registers data pins in the current clock domain. Inter-domain paths are not reported by default.

### Pin to pin

This set lists input to output paths and user sets. Input to output paths are reported by default. To see the userdefined sets, use the <u>Timing Report Options Dialog Box</u>.

### Input to output set

This set reports the paths from the top level design input ports to top level design output ports.

### **Expanded Paths**

Expanded paths can be reported for each set. By default, the number of expanded paths to report is set to 1. You can select and change the number when you specify <u>Timing Report Options</u>.



🕒 Timer Report File Actions Help Timing Report Max Delay Analysis ~ SmartTime Version v12.0 Microsemi Corporation - Microsemi Libero Software Release v12.0 (Version 12.500.0.4) Date: Fri Sep 14 11:55:24 2018 Design: top Family: PolarFire Die: MPF100T Package: FCG484 Temperature Range: 0 - 100 C Voltage Range: 0.97 - 1.03 V Speed Grade: STD Design State: Post-Layout Data source: Preliminary Operating Conditions: slow lv lt Scenario for Timing Analysis: timing\_analysis \_\_\_\_\_ SUMMARY Clock Domain: CLK Period (ns): 2.000 Frequency (MHz): 500.000 Required Period (ns): 0.100 Required Frequency (MHz): 10000.000 External Setup (ns): Max Clock-To-Out (ns): 13.607 -1.983Input to Output Max Delay (ns): N/A END SUMMARY \_\_\_\_\_ Clock Domain CLK Info: The maximum frequency of this clock domain is limited by the minimum pulse widths of pin CLK ibuf/U IOPAD:PAD SET Register to Register Path 1 From: DFN1 0:CLK To: DFN1 1:D Delay (ns): 0.434 Slack (ns): -0.348

Figure 25 · Timing Report

### See Also

<u>Generating a Timing Report</u> <u>Timing Report Options Dialog Box</u>

# **Generating a Timing Violation Report**

The timing violations report provides a flat slack report centered around constraint violations.

#### To generate a timing violation report

 From the SmartTime Max/Min Delay Analysis View window, choose Tools > Reports > Timing Violations. The <u>Timing Violations Report Options Dialog Box</u> appears.



2. Select the options you want to include in the report, and then click **OK**. The timing violations report appears in a separate window.

#### See Also

Understanding Timing Violation Reports

# **Understanding Timing Violation Reports**

The timing violation report contains the following sections:

#### Header

The header lists:

- The report type
- The version of Designer used to generate the report
- The date and time the report was generated
- General design information (name, family, etc.)

#### **Paths**

The paths section lists the timing information for the violated paths in the design.

The number of paths displayed is controlled by two parameters:

- A maximum slack threshold to report
- A maximum number or path to report

By default, the slack threshold is 0 and the number of paths is limited. The default maximum number of paths reported is 100.

All clocks domains are mixed in this report. The paths are listed by decreasing slack.

You can also choose to expand one or more paths. By default, no paths are expanded. For details, see the timing violation report options.



```
_ 🗆 🗙
Timing_violations Report
  File Actions Help
 Timing Violation Report Max Delay Analysis
 SmartTime Version v11.6
 Microsemi Corporation - Microsemi Libero Software Release v11.6 (Version
 11.6.0.16
 Date: Thu Apr 30 16:18:45 2015
 Design: false path
 Family: SmartFusion2
 Die: M2S050
 Package: 484 FBGA
 Temperature Range: 0 - 85 C
 Voltage Range: 1.14 - 1.26 V
 Speed Grade: STD
 Design State: Post-Layout
 Data source: Production
 Min Operating Conditions: BEST - 1.26 V - 0 C
 Max Operating Conditions: WORST - 1.14 V - 85 C
 Scenario for Timing Analysis: Primary
 Path 1
   From:
                                D2 reg:CLK
   To:
                                Q reg:D
                                1.341
   Delay (ns):
   Slack (ns):
                                -0.373
   Arrival (ns):
                               5.333
   Required (ns):
                                4.960
```

Figure 26 · Timing Violations Report

#### See Also

<u>Generating a Timing Violation Report</u> <u>Timing Violations Report Options Dialog Box</u>

# Generating a Constraints Coverage Report

The constraints coverage report contains information about the constraints in the design.

To generate a constraints coverage report, from the SmartTime Max/Min Delay Analysis View, choose **Tools** > **Reports** > **Constraints Coverage**. Select the text format and number of unconstrained instances and click **OK**. The report appears in a separate window.

#### See Also

Understanding Constraints Coverage Reports



# **Understanding Constraints Coverage Reports**

The constraint coverage displays the overall coverage of the timing constraints set on the current design. You can generate this report either from within Designer or within SmartTime Analyzer. The report contains three sections:

- Coverage Summary
- Results by Clock Domain
- Enhancement Suggestions

Constraints_coverage Re	eport				
File Actions Help					
Design Family Die Package Temperature Range Voltage Range Speed Grade Design State Analysis Min Cas Analysis Max Cas Scenario for Tim	3e 3e	false_path SmartFusion M2S050 484 FBGA 0 - 85 C 1.14 - 1.24 STD Post-Layout BEST WORST Primary	5 V		E
Coverage Summary					
+   Type of check   +	Met I	Violated	Untested	Total	L
		10 0 0 15	40 20 10 105	50   20   10   120	
	10   0   0	0 0 0	40 20 10	50   20   10	
+	clk				
+	Met I	Violated	Untested	Total	1
Setup   Recovery   Output Setup   Total Setup		3 0 0 6	12   6   3   42	15   6   3   48	
Removal   Output Hold   Total Hold	3   0   0   6	0 0 0	12 6 3 42	15   6   3   48	
<ul> <li>Enhancement Sugge</li> <li>Max input dela D0, D0, D0, D1</li> <li>Min input dela D0, D0, D0, D1</li> </ul>	estions Ay constraint 1, D1, D1, D2, Ay constraint	missing on p D2, D2, RST, missing on p	ports: , RST, RST ports:	*	+
					•

Figure 27 · Constraints Coverage Report

### **Coverage Summary**

The coverage summary gives statistical information on the timing constraint in the design. For each type of timing checks (Setup, Recovery, Output, Hold and Removal), it specifies how many are Met (there is a constraint and it is satisfied), Violated (there is a constraint and it is not satisfied), or Untested (no constraint was found).



### **Clock Domain**

This section provides a coverage summary for each clock domain.

### **Enhancement Suggestions**

The enhancement suggestion reports, per clock domain, a list of constraints that can be added to the design to improve the coverage. It also reports if some options impacting the coverage can be changed.

### **Detailed Stats**

This section provides detailed suggestions regarding specific clocks or I/O ports that may require to be constrained for every pin/port that requires checks.

Setting SmartTime Options

# Generating a Bottleneck Report

The bottleneck report provides a list of the bottlenecks in the design.

To generate a bottleneck report, from the,SmartTime Max/Min Delay Analysis View, choose **Tools > Reports > Bottleneck**. The report appears in a separate window.

#### See Also

Understanding Bottleneck Reports Timing Bottleneck Analysis Options Dialog Box

# **Understanding Bottleneck Reports**

A bottleneck is a point in the design that contributes to multiple timing violations. The purpose of the bottleneck report is to provide a list of the bottlenecks in the design. You can generate this report either from SmartTime Analyzer. It contains two sections

- Device Description
- Bottleneck Analysis



File Actions Help			
Bottleneck Report Max Delay An-	alysis		
SmartTime Version 11.6.0.13			
	emi Libero Software Release v11.6 (Version 11.6.0.13)		
Date: Tue Apr 21 13:18:30 2015			
Design	TOP		
Family	RTG4		
Die	RT4G150		
Package	1657 CG		
Radiation Exposure	0		
Temperature	MIL		
Voltage	MIL		
Speed Grade	-1		
Design State	Post-Layout		
Data source	Advanced		
Analysis Max Case	WORST		
Set selection type	Select Entire Design		
Cost type	Path Count		
Max Paths	100		
Max Parallel Paths	1		
Bottleneck instances	10		
Slack Threshold	0		
Scenario for Timing Analysis	Primary		
Bottleneck Analysis			
+		++	
Instance Name		Path Count	
*		++	
FDDR_INIT_0/COREABC_0/IO_OUT[0];Q		1 50 1	
<pre>/ CoreAHBLite_0/matrix4x16/masterstage_0/SDATASELInt_RNIBSEF1[0]:Y</pre>		16	
CoreAHBLite_0/matrix4x16/slavestage_0/HREADYOUT_or:Y		15 1	
CoreAHBLite_0/matrix4x16/masterstage_0/HREADY_M_iv_RNIME982:Y		15 1	
CoreAHBLite_0/matrix4x16/slavestage_0/slave_arbiter/arbRegSMCurrentState_RNO[1]:Y   1		11 1	
CoreAHBLite_0/matrix4x16/slavestage_0/slave_arbiter/arbRegSMCurrentState_RN0[3]:Y   1		11 1	
CoreAHBLite_O/matrix4x16/slavestage_O/slave_arbiter/arbRegSMCurrentState_RNO[11]:Y   1			
CoreAHBLite_0/matrix4x16/slavestage_0/slave_arbiter/arbRegSMCurrentState_nss_i_0[0]:Y   1			
CoreAHBLite 0/matrix4x16/slav	vestage 0/slave arbiter/arbRegSMCurrentState RNO[7]:Y	1	

#### Figure 28 · Bottleneck Report

The bottleneck can only be computed if and only a cost type is defined. There are two options available:

- **Path count:** This cost type associates the severity of the bottleneck to the count of violating/critical paths that traverse the instance.
- **Path cost:** This cost type associates the severity of the bottleneck to the sum of the timing violations for the violating/critical paths that traverse the instance.

### **Device Description**

The device section contains general information about the design, including:

- Design name
- Family
- Die
- Package
- Software version

#### **Bottleneck Analysis**

This section lists the core of the bottleneck information. It is divided into two columns:

- Instance name: refers to the output pin name of the instance.
- Path Count: Displays the number of violating paths which include the instance pin.

#### See Also

Timing Bottleneck Analysis Options Dialog Box



# Generating a Datasheet Report

The datasheet reports information about the external characteristics of the design.

Note: Generating Datasheet Report is not supported in PolarFire.

To generate a datasheet report, from the SmartTime Max/Min Delay Analysis View, choose **Tools > Reports > Datasheet**. The report appears in a separate window.

### See Also

<u>Understanding Datasheet Reports</u> <u>Timing Datasheet Report Options Dialog Box</u>

# **Understanding Datasheet Reports**

The datasheet report displays the external characteristics of the design. . You can generate this report from SmartTime Max/Min Delay Analysis View. It contains three tables:

- Pin Description
- DC Electrical Characteristics
- AC Electrical Characteristics



	AT7	Input	1	1												
	AU7	Input		1												
	AW4	Input	- 1	1												
	AV4	Input	- 1	1												
	BA5	Input	5 I	1												
	AY5			1												
				1												
			= I	1												
				1												
				1												
	AG40	Outpu	IT   SSTL	18I (1)												
0_OUT	AC36	Outpu	IT   SSTL	181 (1)												
	AE40	Outpi	IC   SSTL	101 (1)												
				(2)												
				1												
				1												
				i												
				Outp					i							
				i i												
		Outpu	at	1												
	AV8															
	AW8		1t   													
Zacteri Zcci   (V)   	Vccr   (V)	Outpu	Output Load (pF)		Odt   Imp   (Ohm)	Input   Delay 	Resistor   Pull 	Schmitt   Trigger 	Slew   	Output	1					
/cci   (V)   	AW8 + istics Vccr   (V)   	Outpo Direction	Output Load (pF)	Odt_Static   	Odt   Imp   (Ohm)	Input   Delay 	Resistor   Pull   +	Schmitt   Trigger   +	Slew   	Output   Drive	1					
/cci   (V)   	Vccr   (V)	Outpu   Direction	Output Load (pF)	Odt_Static       	Odt   Imp   (Ohm) +	Input   Delay       Off	Resistor   Pull     None	Schmitt   Trigger   +   Off	Slew   	Output   Drive   (mA) +	1					
racteri 7cci   (V)      .8   1.8	Vccr   (V)   	Output Direction Input Output	Output Load (pF)	Odt_Static       	Odt   Imp   (Ohm) +	Input   Delay       Off 	Resistor   Pull     None   None	Schmitt   Trigger   +   Off	Slew           SLOW	Output   Drive   (mA) +	1					
racteri 7cci   (V)      .8   1.8	Vccr   (V)   	Output Direction Input Output	Output Load (pF)	Odt_Static         	Odt   Imp   (Ohm) +	Input   Delay       Off 	Resistor   Pull     None   None	Schmitt   Trigger   +   Off   	Slew           SLOW	Output   Drive   (mA) +     4	1					
	0_01I	AV4   BA5   AY5   BA7   BA7   BA9   AY9   AN35   AU35   AG36   AG36   AG36   AG36   AG36   AM36   AM36   AJ36   AJ36 	AV4   Input   BA5   Input   BA5   Input   BA7   Input   BA7   Input   BA7   Input   BA9   Input   AY9   Input   AY9   Input   AY9   Outpu   A39   Outpu   AG39   Outpu   AG39   Outpu   AG39   Outpu   AG39   Outpu   AG36   Outpu   AA39   Outpu   AA39   Outpu   AA38   Outpu   AJ39   Outpu   AJ38   Outpu   AJ3   Outpu   AJ3   Outpu   AJ3   Outpu   AJ5   Outpu   AU5   Outpu   AV6   Outpu   AV6   Outpu	AV4   Input     BA5   Input     AX5   Input     BA7   Input     BA7   Input     BA7   Input     BA9   Input     AX9   Output   STL   AX39   Output   STL   AG40   Output   AG40   Output     AG40   Output   AG40   Output     AG40   Output   AG40	AV4   Input     BA5   Input     AY5   Input     AY5   Input     BA7   Input     BA7   Input     BA9   Input     AY9   Input     AY9   Output   SSTL18I (1)     AX99   Output   SSTL18I (1)     AG40   Output   SSTL18I (2)     AG40   Output   LVCMOS18 (2)     AG4   Output   LVCMOS18 (2)     AG5   Output     LVCMOS18 (2)     AG5   Output         AU5   Output         AV6   Output	AV4   Input	AV4   Input     BA5   Input     AY5   Input     BA7   Input     BA7   Input     BA7   Input     BA9   Input     AX9   Output   SSTL181 (1)     AX99   Output   SSTL181 (1)     AG40   Output   SSTL181 (1)     AG46   Output   SSTL181 (1)     AG48   Output   SSTL181 (2)     AG48   Output   LVCMOS18 (2)     AG48   Output   LVCMOS18 (2)     AG48   Output   LVCMOS18 (2)     AG48   Output     AG48   Output     AG48   Output     AG48   Output     AG48   Output	AV4   Input	AV4   Input	AV4   Input	AV4   Input   BA5   Input   AY5   Input   BA7   Input   BA7   Input   BA7   Input   BA9   Input   AY9   Output   SSTL18   (1)   AX99   Output   SSTL18   (1)   AG40   Output   SSTL18   (1)   AG46   Output   SSTL18   (1)   AG46   Output   SSTL18   (1)   AG46   Output   SSTL18   (1)   AG46   Output   SSTL18   (2)   AG48   Output   SSTL18   (2)   AG48   Output   LVCMOS18 (2)   AG48   Output   LVCMOS18 (2)   AG48   Output   AG48					

Figure 29 · Datasheet Report

### **Pin Description**

Provides the port name in the netlist, location on the package, type of port, and I/O technology assigned to it. Types can be input, output, inout, or clock. Clock ports are ports shown as "clock" in the Clock domain browser.

### **DC Electrical Characteristics**

Provides the parameters of the different I/O technologies used in the design. The number of parameters displayed depends on the family for which you have created the design.

### **AC Electrical Characteristics**

Provides the timing properties of the ports of the design. For each clock, this section includes the maximum frequency. For each input, it includes the external setup, external hold, external recovery, and external removal for every clock where it applies. For each output, it includes the clock-to-out propagation time. This section also displays the input-to-output propagation time for combinational paths.

### See Also

<u>Generating a Datasheet Report</u> <u>Timing Datasheet Report Options Dialog Box</u>



# Generating a Combinational Loop Report

The combinational loop report displays all loops found during initialization and reports pins associated with the loop(s), and the location where the loop is broken.

To generate the combinational loop report; from the Tools menu, choose Reports > Combinational Loops ....

Select either the **Plain Text** or **Comma Separated Values** option in the Combinational\_Loops Report Options dialog box and click **OK**.

The plain text report will pop up in a new window; you will be prompted to save the CSV in a directory of your choosing.

### See Also

Understanding Combinational Loop Reports

# **Understanding Combinational Loop Reports**

The combinational loop report displays all loops found during initialization and reports pins associated with the loop(s), and the location where the loop is broken.

Combinational_loops Report		- C X
File Actions Help		
Combinational Loop Report SmartTime Version 11.6.0.15 Microsemi Corporation - Microse 11.6.0.15) Date: Fri May 01 15:50:15 2015	mi Libero Software Release v11.6 (	Version
Voltage Range Speed Grade Design State Analysis Min Case		

Figure 30 · Combinational Loop Report

### See Also

Generating a Combinational Loop Report



# **Timing Concepts**

# Static Timing Analysis Versus Dynamic Simulation

Static timing analysis (STA) offers an efficient technique for identifying timing violations in your design and ensuring that it meets all your timing requirements. You can communicate timing requirements and timing exceptions to the system by setting timing constraints. A static timing analysis tool will then check and report setup and hold violations as well as violations on specific path requirements.

STA is particularly well suited for traditional synchronous designs. The main advantage of STA is that unlike dynamic simulation, it does not require input vectors. It covers all possible paths in the design and does all the above with relatively low run-time requirements. The major disadvantage of STA is that the STA tools do not automatically detect false paths in their algorithms.

# **Delay Models**

The first step in timing analysis is the computation of single component delays. These components could be either a combinational gate or block or a single interconnect connecting two components.

Gates that are part of the library are pre-characterized with delays under different parameters, such as input-slew rates or capacitive loads. Traditional models provide delays between each pair of I/Os of the gate and between rising and falling edges.

The accuracy with which interconnect delays are computed depends on the design phase. These can be estimated using a simple Wire Load Model (WLM) at the pre-layout phase, or a more complex Resistor and Capacitor (RC) tree solver at the post-layout phase.

# **Timing Path Types**

Path delays are computed by adding delay values across a chain of gates and interconnects. SmartTime uses this information to check for timing violations. Traditionally, timing paths are presented by static timing analysis tools in four categories or "sets":

- Paths between sequential components internal to the design. SmartTime displays this category under the Register to Register set of each displayed clock domain.
- Paths that start at input ports and end at sequential components internal to the design. SmartTime displays this category under the External Setup and External Hold sets of each displayed clock domain.
- Paths that start at sequential components internal to the design and end at output ports. SmartTime displays this category under the Clock to Out set of each displayed clock domain.
- Paths that start at input ports and end at output ports. SmartTime displays this category under the Input to Output set.

# Maximum Clock Frequency

Generally, you set clock constraints on clocks for which you have a specified requirement. The absence of violations indicates that this clock will be able to run at least at the specified frequency. However, in the absence of such requirements, you may still be interested in computing the maximum frequency of a specific clock domain.

To obtain the maximum clock frequency, a static timing analysis tool computes the minimum period for each path between two sequential elements. To compute the maximum period, the tool evaluates the maximum data path delay and the minimum skew between the two elements, as well as the setup on the receiving sequential element. It also considers the polarity of each sequential element. The maximum frequency is the inverse of the largest value among the maximum period of all the paths in the clock domain. The path responsible for limiting the frequency of a given clock is called the critical path.



# **Setup Check**

The setup and hold check ensures that the design functions as specified at the required clock frequency.

Setup check specifies when data is required to be present at the input of a sequential component in order for the clock to capture this data effectively into the component. Timing analyzers evaluate the setup check as a maximum timing budget allowed between adjacent sequential elements. For more details on how setup check is processed, refer to <u>Arrival Time, Required Time, and Slack</u>.

### See Also

Static Timing Analysis Versus Dynamic Simulation Arrival Time, Required Time, and Slack

# Arrival Time, Required Time and Slack

You can use arrival time and required time to verify timing requirements in the presence of constraints. Below is a simple example applied to verifying the clock requirement for setup between sequential elements in the design.

The arrival time represents the time at which the data arrives at the input of the receiving sequential element. In this example, the arrival time is considered from the setup launch edge at CK, taken as a time reference (instant zero). It follows the clock network along the blue line until the clock pin on FF1 (delay d1). Then it continues along the data path always following the blue line until the data pin D on FF2. Therefore,

#### Arrival\_Time\_FF2:D = d1 + d2

The required time represents when the data is required to be present at the same pin FF2:D. Assume in this example that in the presence of an FF with the same polarity, the capturing edge is simply one cycle following the launch edge. Using the period T provided to the tool through the clock constraint, the event gets propagated through the clock network along the red line until the clock pin of FF2 (delay d3). Taking into account FF2 setup (delay d4), this means that the clock constraint requires the data to be present d4 time before the capturing clock edge on FF2. Therefore, the required time is:

Required\_Time\_{FF2:D} = T + d3 - d4

The slack is simply the difference between the required time and arrival time:

SlackFF2:D = Required\_TimeFF2:D - Arrival\_TimeFF2:D

If the slack is negative, the path is violating the setup relationship between the two sequential elements.

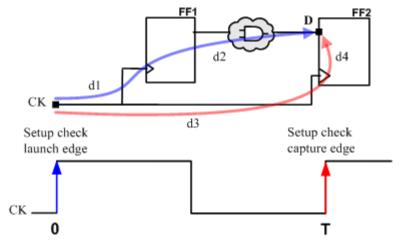


Figure 31 · Arrival Time and Required Time for Setup Check



# **Timing Exceptions Overview**

Use timing exceptions to overwrite the default behavior of the design path. Timing exceptions include:

- Setting multicycle constraint to specify paths that (by design) will take more than one cycle.
- Setting a false path constraint to identify paths that must not be included in the timing analysis or the optimization flow.
- Setting a maximum/minimum delay constraint on specific paths to relax or to tighten the original clock constraint requirement.

# **Clock Skew**

The clock skew between two different sequential components is the difference between the insertion delays from the clock source to the clock pins of these components. SmartTime calculates the arrival time at the clock pin of each sequential component. Then it subtracts the arrival time at the receiving component from the arrival time at the launching component to obtain an accurate clock skew.

Both setup and hold checks must account for clock skew. However, for setup check, SmartTime looks for the smallest skew. This skew is computed by using the maximum insertion delay to the launching sequential component and the shortest insertion delay to the receiving component.

For hold check, SmartTime looks for the largest skew. This skew is computed by using the shortest insertion delay to the launching sequential component and the largest insertion delay to the receiving component. SmartTime makes this distinction automatically.

# **Cross Probing**

Design objects displayed in SmartTime can be cross-probed into other Libero SoC tools. Libero SoC allows cross-probing from SmartTime to the Constraints Editor (but not vice versa) and from SmartTime to Chip Planner (but not vice versa). When cross-probing from SmartTime to one of the other tools, both SmartTime and the other tool must first be opened.

### From SmartTime to Constraint Editor

You can add a timing exception constraint from SmartTime and have the Constraints Editor display the Constraint. From the SmartTime Maximum or Minimum Delay Analysis View, click a timing path to add a timing exception constraint. When the Constraints Editor's Add Constraint dialog box opens, the fields for source (from) pin and destination (to) pin are populated with the correct names from the timing path you have selected.

To add a timing exception constraint from a timing path in SmartTime Max/Min Delay Analysis View:

- 1. Open SmartTime (Design Flow Window > Verify Timing > Open interactively).
- 2. Open the Constraints Editor (Constraint Manager > Timing Tab > Edit with Constraints Editor).
- 3. Select Max/Min Delay Analysis View and right-click a timing path in the table.
- 4. Select a timing exception constraint to add: False Path Constraint, Maximum Delay Constraint, Minimum Delay Constraint, or Multicycle Path Constraint.



0	ustomize table		Appl	y Filter Store F	lter Reset Filte	ar
	Source Pin	Sink Pin	Delay (ns)	Slack (ns)	Arrival (ns)	1
1	Q[6]:CLK	Q[6]	3.990		7.592	-
2	Q[4]:CLK	Q[4]	3.899		7.499	-
3	Q[3]:CLK	Q[3]	3.872		7.472	E
4	Q[2]:CLK	Q[2]	Copy Print		7.463	
5	Q[1]:CLK	Q[1]	Add False Path	Constraint	6.640	-
6	Q[0]:CLK	Q[0]	Add Max Delay	Constraint	6.633	
	`*[	, III.	Add Min Delay	Constraint		
Na	me	Туре	Add Multicycle	Path Constraint	Macro	-
4	Summary data required time		Show Path in C	hip Planner		
	data arrival time		Expand selected	d paths		
	slack Data_arrival_time_calc	ulation				
					2	

Figure 32 · Add Timing Constraint from SmartTime's Reported Timing Path

**Note**: The Add Max/Min Delay, False Path, and Multicycle Path Constraint menu items are grayed out if the Constraint Editor is not open.

Add the Constraint in the Add Constraint dialog box. Note that the source/from pin and destination/to pin field are populated with the correct pin names captured from the SmartTime reported path (Source Pin and Sink Pin) you have clicked.



🔝 Set Maximum Delay Constraint	8 2
Maximum delay : 1.0 ns	
From :	
[ get_pins { q_reg[3]/CLK } ]	·
	<b>T</b>
*	,
Through :	
	Â
	w
To :	
[ get_pins { Q[3]/D } ]	·
4	w
Comment :	
Help	OK Cancel

Figure 33 · Add Maximum Delay Constraint

- 5. Click OK to exit the Add Constraint Dialog box.
- 6. Click Save in the Constraints Editor.
- 7. Exit the Constraints Editor.
- 8. Exit SmartTime.
- 9. Rerun Place and Route if the newly-added constraint that is added to a file (the Target file) is used for Place and Route and Verify Timing.
- 10. Open SmartTime Maximum/Minimum Delay Analysis View.

### From SmartTime to Chip Planner

Cross-probing allows you to select a design object in one application and display the selected object in another application. Because Libero SoC allows you to cross-probe design objects from SmartTime to Chip Planner, you can better understand how the two applications interact with each other. With cross-probing, a timing path not meeting timing requirements can be fixed with relative ease when you see the less-than-optimal placement of the design object (in terms of timing requirements) in Chip Planner. Cross-probing from SmartTime to Chip Planner is available for the following design objects:

- Macros
- Ports
- Nets/Paths

Note: Cross-probing of design objects is available from SmartTime to Chip Planner but not vice versa.

Before you can cross-probe from SmartTime to Chip Planner, you must:

- 1. Complete the Place and Route step on the design.
- 2. Open both SmartTime and Chip Planner.



### **Cross-Probing Examples**

To cross-probe from SmartTime to Chip Planner, a design macro in SmartTime is used.

### **Design Macro Example**

- 1. Make sure that the design has successfully completed the Place and Route step.
- 2. Open SmartTime Maximum/Minimum Analysis View.
- 3. Open Chip Planner.
- 4. In the SmartTime Maximum Analysis View, right-click the instance Q[2] in the Timing Path Graph and choose **Show in Chip Planner**. Note that with cross-probing, the Q[2] macro is selected in Chip Planner's Logical View and highlighted (white) in the Chip Canvas. The Properties window in Chip Planner displays the properties of Q[2].

Note: Show in Chip Planner is grayed out if Chip Planner is not already open.

Note: You may need to zoom in to view the highlighted Q2 Macro in the Chip Canvas.

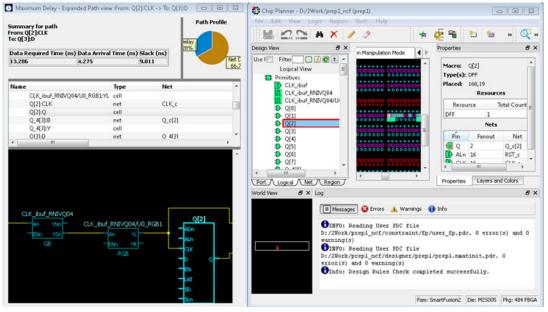


Figure 34 · Cross-Probing – Macro

### Timing Path Example

- 1. Make sure that the design has successfully completed the Place and Route step.
- 2. Open the SmartTime Maximum/Minimum Analysis View.
- 3. Open Chip Planner.
- 4. In the SmartTime Maximum/Minimum Analysis View, right-click the net CLK\_ibuf/U0/U\_IOPAD:PAD in the Table and choose **Show Path in Chip Planner**. Note that the net is selected (highlighted in red) in the Chip Canvas view and the three macros connected to the net are also highlighted (white) in the Chip Canvas view.

Note: Show Path in Chip Planner is grayed out if Chip Planner is not already open.



SmartTime - [Maximum Delay - Expanded Path view :From: Q[2]:CLK -> To: Q[3]:D]	Chip Planner - D:/2Work/prep1_ncf (prep1) File Edit View Logic Region Tools Help	
≝ Ω № ≽ € 0 ⊚ ≍	H CC AX / 2	≉ 🤹 » 🐮 » 🔍 »
Immary for path one (0/2)CLK v (0/2)D ata Required Time (ns) Data Arrival Time (ns) Slack (ns) 3.206 4.275 9.011	Logical View 000000000000000000000000000000000000	
Anne Trpe Net Mac	D         Q[4]         >+++         >++++         >++++         >++++         >++++         >++++         >+++++         >+++++         >+++++         >++++++         >++++++         >++++++         >+++++++         >++++++++         >+++++++++         >++++++++++         >+++++++++++         >+++++++++++++         >+++++++++++++++++++++++++++++++++++	
CLK_ibuf_RNIVQ04An CLK_ibuf_RNIVQ04An CLK_ibuf_RNIVQ04An criment compose_power or one analysis compose_power or one analysis c	c. 0 error(s) and 0 INFO: Reading User	<pre>c PDC file onstraint/fp/user_fp.pd warning(s) c PDC file lesigner/prepl/prepl.nma ) and 0 warning(s)</pre>

Figure 35 · Cross-Probing – Timing Path

Alternatively, right-click a path in the Max/Min Delay Analysis View and select **Show Path in Chip Planner** to cross-probe the path.

Analysis for scenario	From Custom	izo tablo								10 -
Clock to Output Register to Asynchronous External Recovery		Source Pin	Sink Pin	Delay (ns)	Slack (ns)	Arrival (ns)	Required (ns)	Setup (ns)	External Setup (ns)	
Asynchronous to Register     Generation (Inst_coc_IP-GL0     Register to Register     External Setup     Cock to Output	1 0		DFN1_0:D	0.154		0.154 Copy Print		0.262	-1.941	
Register to Asynchronous External Recovery Asynchronous to Register Proto Inn Proto Inn Studies Sets						Add Max Del Add Min Dela	ith Constraint ay Constraint ay Constraint ie Path Constra	urt.		
						Show Path in Expand selec	Chip Planner			
					_					

Figure 36 · Cross-Probing Path from Max/Min Delay Analysis View Table

### **Port Example**

- 1. Make sure that the design has successfully completed the Place and Route step.
- 2. Open the SmartTime Maximum/Minimum Analysis View.
- 3. Open Chip Planner.
- 4. In the SmartTime Maximum/Minimum Analysis View, right-click the Port "CLK" in the Path and choose **Show in Chip Planner**. Note that the Port "CLK" is selected and highlighted in the Chip Planner Port View.

Note: Show in Chip Planner is grayed out if Chip Planner is not already open.



SmartTime - [Maximum Delay - E File Edit View Tools Hel		om: Q[2]:CLK -> To: Q[3]:	0] - 0 ×		2Work/prep1_ncf (prep1) Logic Region Tools			0 8 2
<b>1 2 2 2 4 6</b> 0				100	AXIO		* 🤅 🖬	🐮 » 🔍 x
iummary for path irom: Q[2]:CLK io: Q[3]:D		Dela	Path Profile	Design View Use Filte	Øx Or	Canvas - Region P		
Data Required Time (ns) Data Ar 13.286 4.275	rival Time (ns) Slack 9.011	(ns)	Net Dr	B U/O Port     D     CLK     O				
Name	Type	Net	Mac ^	RST D S0		8.*8.*8		
<ul> <li>Data_arrival_time_calculation prep1 CLK CLK</li> </ul>	Clock source		. 5	ខ្លាំ	-			
CLK_ibuf/UI/U_JOPAD:PAD CLK_ibuf/UI/U_JOPAD:Y	net	CLK	ADL	Port A Logical A N	et Region			•
CLK_ibuf_RNIVQ84:An CLK_ibuf_RNIVQ84:YSn	net cell	CLK_ibuf	ADL *	World View	₫× Log			8 >
			,			lessages 🔞 Erro	irs 🗼 Warnings	🕕 Info
Zoom In Zoom In Zoom Out Zoom Fit Print Show in Chip Planner		2 4 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5			D:/20 0 er: 0 r: 0:/20 nit.; 0 In	FO: Reading U Work/prepl_nct pdc. 0 error(:	f/constraint/fj warning(s) ser FDC file	
Show in Chip Planner		Temp: 0 - 85 C Volt: 1.14	+			Fam: Smarth	usion2 Die: M2500	5 Diver 484 FRGA

Figure 37 · Cross-Probing – Port

From the Properties View inside Chip Planner, you will find useful information about the Port "CLK" you are crossprobing:

- Port Type
- Port Placement Location (X-Y coordinates)
- I/O Bank Number
- I/O Standard
- Pin Assignment

perties			8 :
Macro:	CLK_ibuf		
Port(s):	CLK		
Type(s):	I/O, Single-	-ended I/O, Input I/O	
Placed:	0,19		
Package Pin(s):	H1		
I/O Standard(s	): LVCMOS25		
I/O Bank:	Bank6 - MS	IO 🗌 Locked	
		Resources	
Resource		Total Count	
IO	1		
An inclusion of the second sec		Nets	
Pîn	Fanout	Net	

Figure 38 · Properties View of Port "CLK"



# **SmartTime Tutorials**

# Tutorial 1 - 32-Bit Shift Register with Clock Enable

This tutorial section describes how to enter a clock constraint for the 32-bit shift register on SmartFusion2 device. You will use the SmartTime Constraints Editor and perform post-layout timing analysis using the SmartTime Timing Analyzer.

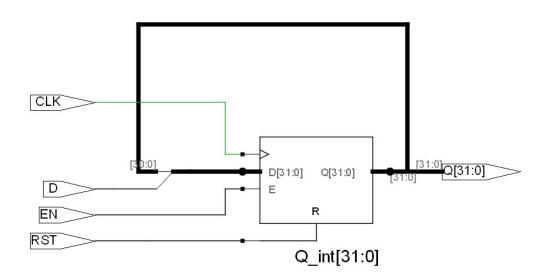


Figure 39 · 32-bit Shift Register

Use the links below to go directly to a topic:

- Add a Clock Constraint
- Run Place and Route
- Maximum Delay Analysis with Timing Analyzer
- Minimum Delay Analysis with Timing Analyzer
- <u>Changing Constraints and Observing Results</u>

#### To set up your project:

- 1. Invoke Libero SoC. From the Project menu, choose New Project.
- 2. Enter sf2\_shift32 for your new project name and browse to a folder for your project location.
- 3. Select Verilog as the Preferred HDL Type.
- 4. Leave all other settings at the default values.



ew project				
roject details Specify project details				
Project Details	Project name:	sf2_shfit32		
Device Selection	Project location:	d. (actelprj		Browse
Device Settings	Description:			
Design Template				
	Preferred HDL type	Contraction of the second seco		
Add HDL Sources				
Add Constraints				
.ibero				
Help			< Back Next >	Finish Cancel

Figure 40 · New Project Creation - 32 Bit Shift Register

- 5. Click Next to go to Device Selection page. Make the following selection from the pull-down menu:
  - Family: SmartFusion2
  - **Die**: M2S090TS
  - Package: 484FBGA
  - Speed:STD
  - Core Voltage: 1.2 V
  - Range: COM

6. Click the M2S090TS-1FG484 part number and click Next.

Project Details	Part filter									
Project Details	Family:	SmartFu			M2S090TS	•		484 FBGA	•	
	Speed:	-1	-	Core voltage:	1.2	•	Range:	COM	•	
Device Selection								Rese	et filters	
Device Settings	Search part:									
	Part Numb	er	4LUT	DFF	User I/Os	uSRAM 1K	(	LSRAM 18K	Math (18x18)	PLLs and
Design Template	M25090TS-	LFG484	86184	86184	267	112		109	84	6
Add HDL Sources Add Constraints										
bero										

- 7. Accept the default settings in the Device Settings page and click Next.
- 8. Accept the default settings in the Design Template page and click **Next**.
- 9. Click Next to go to the Add Constraints Page.



- 10. We are not adding any constraints. Click **Finish** to exit the New Project Creation wizard.
- 11. To add a new HDL file, select File> New> HDL. The Create a new HDL file dialog box opens. Name the HDL file as shift\_reg32 as shown below and click OK.

	8 23
C VHDL	
ard template	
	C VHDL

Figure 41 · Create a new HDL file Dialog Box

12. Copy and paste the code shown below into the Verilog file:

```
module shift32 ( Q,CLK,D,EN,RESET);
input D,EN,CLK,RESET;
output[31:0] Q;
reg [31:0] Q_int;
assign Q=Q_int;
always@ (posedge CLK)
begin
if(RESET)
Q_int<=0;
else begin
if(EN)
Q_int<={Q_int[30:0],D};
end
end
endmodule
```

- 13. Check the HDL file to confirm that there are no syntax errors.
- 14. Confirm that the shift\_reg32 design appears in the Design Hierarchy window, as shown in the figure below.



Design Hierarchy		8 ×
Build Hierarchy	Show: Components	
	t32 (shift_reg32.v) [work] DL Source Files	

Figure 42 · shift\_reg32 in the Design Hierarchy Window

15. In the Design Flow window, double-click **Synthesize** to run Synplify Pro with default settings. A green check mark appears next to Synthesize when Synthesis is successful (as shown in the figure below).

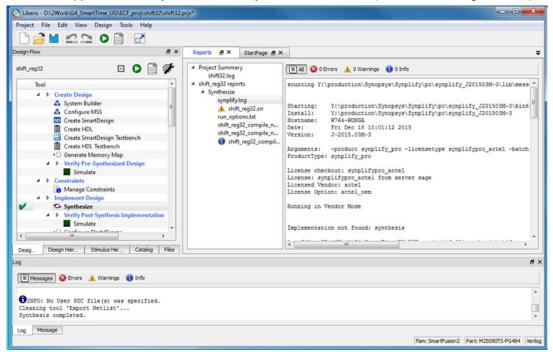


Figure 43 · Synthesis and Compile Complete - 32-Bit Shift Register with Clock Enable



# Add a Clock Constraint - 32 Bit Shift Register

### To add a clock constraint to your design:

1. In the Design Flow window, double-click **Manage Constraints**. The Constraint Manager appears (as shown in the figure below.)

Reports     ₽     StartPage     ₽     Constraint Manager     ₽     ×	Ŧ
I/O Attributes Timing Floor Planner Netlist Attributes	
New Import Link Edit with Chip Planner Check Help	<b>*</b>
Place and Route	

Figure 44 · Constraint Manager

2. Click the **Timing** tab.

File Constraints Tools Edit Help

3. Click Edit with Constraints Editor > Edit Place and Route Constraints. The Constraints Editor appears.

<ul> <li>Constraints</li> <li>Syntax</li> <li>Clock</li> <li>Clock</li></ul>	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Clock Source	(ns)	Frequency (MHz)	Dutycycle (%)	First Edge	Offset (ns)	Waveform	Add	File	
Clock 1Click with Generated Clock Input Delay									7400	FIIC	
Generated Clock	1		0.000		50%	rising	0.000	0.00 0.00		GUI	
			0.000		3078	nsing	0.000	0.00 0.00	<u> </u>	001	
- External Check											
Clock To Out											
Exceptions											
Max Delay											
Min Delay											
Multicycle											
Falce Path											
E Advanced											
Disable Timing											
Clock Source Latency											
Clock Uncertainity Clock Groups											

Figure 45 · Constraints Editor – Add clock constraint

4. In the Constraints Editor, right-click **Clock** under Requirement and select **Add Clock Constraint**. The Create Clock Constraint Dialog Box appears.



Create Clock Constraint			8 🛛
Clock Name :	Clock Source :		
Period :	ns	br Frequency:	Mhz
Offset :Duty cycle : 0.000 ns 50.0000 %	H		
Comment :		ок	Cancel

Figure 46 · Create Clock Constraint Dialog Box

- 5. From the **Clock Source** drop-down menu, choose the **CLK** pin.
- 6. Enter **my\_clk** in the Clock Name field.
- 7. Set the Frequency to 250 MHz (as shown in the figure below) and leave all other values at the default settings. Click **OK** to continue.

Create Clock Constraint				8 🕅
Clock Name : my_clk	Clock Source :	[get_ports { CLK } ]		
Period : 4	ns ——	Hr Frequency:	250	Mhz
Offset:Duty cycle:				
Add this clock to existing one with same source				_
Help		ОК	Canc	el

Figure 47 · Add a 250 MHz Clock Constraint

The clock constraint appears in the SmartTime Constraints Editor (as shown in the figure below).



- Constraints	Cumbrus	Clock Name	Clock Source	Period	Frequency	Dutycycle	First	Offset	Waveform	Т
Requirements     Clock	Syntax		CIOCK Source	(ns)	(MHz)	(%)	Edge	(ns)		_
Generated Clock	1 Click within			0.000		50%	rising	0.000	0.00 0.00	0
Input Delay	2 🚩	my_clk	[ get_ports { CL	4.000	250.000	50.000000	rising	0.000	0.00 2.00	
<ul> <li>Min Delay</li> <li>Multicycle</li> <li>False Path</li> <li>Outbound</li> <li>Disable Timing</li> <li>Clock Source Latency</li> <li>Clock Uncertainity</li> <li>Clock Groups</li> </ul>										

Figure 48 · 250 MHz Clock Constraint in the Constraint Editor

- 8. From the File menu, choose Save to save the constraints.
- 9. From the SmartTime **File** menu, choose **Exit** to exit SmartTime. Libero creates a constraint file to store the clock constraint. This file is listed and displayed in the Constraint Manager. It is named user.sdc and is designated as Target.

**Note**: A target file is used to store newly added constraints from the Constraint Editor. When the Constraint Editor is invoked and no SDC timing constraint file is present, Libero SoC creates the user.sdc file (and marks it as target) to store the timing constraints you create in the Constraint Editor.

10. In the Constraint Manager, check the checkbox under Place and Route and the checkbox under Timing Verification to associate the constraint file to the tools. The constraint file is used for both Place and Route and Timing Verification.



New Import Link	Edit with Constraint Editor	Check     Derive Constraints     Help	<b>†</b>
	Synthesis	Place and Route Timing Verification	
nstraint\user.sdc [Target]			

Figure 49 · SDC Constraint File and Tool Association

# **Run Place and Route**

- 1. Right-click Place and Route and choose Configure Options.
- 2. Click the checkbox to enable Timing-Driven layout in Layout Options and leave the other values at the default settings (as shown in the figure below). Click **OK** to continue.



Layout Options	2
Power-driven	
I/O Register Combining	
Global Pins Demotion	
High Effort Layout	
Repair Minimum Delay Violations	
Use Multiple Passes	
Help OK Car	ncel

Figure 50 · Layout Options Dialog Box

3. Double-click **Place and Route** inside the Design Flow window to start the Place and Route.

A green check mark appears next to Place and Route after successful completion of Place and Route.

# Maximum Delay Analysis with Timing Analyzer- 32-Bit Shift Register Example

The SmartTime Maximum Delay Analysis window displays the design maximum operating frequency and lists any setup violations.

### To perform Maximum Delay Analysis:

1. Right-click **Open SmartTime** in the Design Flow window and choose **Open Interactively** to open SmartTime. The Maximum Delay analysis window appears. A green check next to the clock name indicates there are no timing violations for that clock domain. The Summary page displays a summary of the clock domain timing performance.

The Maximum Delay Analysis Summary displays:

- Maximum operating frequency for the design
- External setup and hold requirements



 Maximum and minimum clock-to-out times. In this example, the maximum clock frequency for CLK is 609.75 MHz.

	Edit View Tools Help										- 6
1 4	2 🗅 🌶 🗲 0 🐵 🌫										
imum Dei	lay Analysis View										
0											
MAX	Analysis for scenario timing_analysis	Design			shift_reg32						- Â
	Summary	Family			SmartFusion2						
	v⊕ my_clk	Die			M2S090TS						
	<ul> <li>Register to Register</li> <li>External Setup</li> </ul>	Package			484 FBGA						
	Clock to Output	Temperate	ure Rang	9	0 - 85 C						
	Register to Asynchronous	Voltage R	ange		1.14 - 1.26 V						
	External Recovery Asynchronous to Register	Speed Gr	ade		STD						
-	🔀 Pin to Pin	Design State			Post-Layout						
	Input to Output St User Sets	Data source			Production						
		Min Operating Conditions		ditions	BEST - 1.26 V -	0 C					
		Max Oper	ating Co	nditions	WORST - 1.14	V - 85 C					
		Scenario	for Timin	Analysis	timing_analysis						
		Summ	Summary								
of paths	Select a set of paths to see its slack distribution.	Clock Domain			y Required Period (ns)	Required Frequency (MHz)	External Setup (ns)	External Hold (ns)	Min Clock- To-Out (ns)	Max Clock- To-Out (ns)	
		my_clk	1.640	609.756	4.000	250.000	1.297	0.510	3.781	9.880	
			M	in Delay (n	s) Max Delay	(ns)					-
	slack distribution(ns)	Incast to O			NI/A						

Figure 51 · Maximum Delay Analysis - Summary

- 2. Expand my\_clk to display the Register to Register, External Setup and Clock to Output path sets.
- 3. Select **Register to Register** to display the register-to-register paths. The window displays a list of registerto-register paths and detailed timing analysis for the selected path (as shown in the figure below). Note that all the slack values are positive, indicating that there are no setup time violations

AX Young Summary ✓ (B) my_clk ✓ Register to Register External Satup Clock to Output Register to Agnchronous External Bacovery Agnchronous to Register ✓ (P) hoto Pin Input to Output		en * ustomze table Source Pin					TO -					
										Carrier and Carl	[ and the set of the	[accent]
	1	Countra Bin								Apply Filter	Store Filter	Reset Filter
Clock to Output Register to Asynchronous External Recovery Asynchronous to Register # Input to Output Input to Output	1	Counce Bin								111		
Register to Asynchronous External Recovery Asynchronous to Register 4 🏹 Pinto Pin Input to Output	1		Sink Pin	Delay (ns)	The de Land	Arrival (ns)	Required	Setup (ns)	Minimum Period	Skew (n		
External Recovery Asynchronous to Register A XP Pin to Pin Input to Output	1	Source Pill	SILKPIN	Delay (iis)	SIACK (IIS)	Arrival (ns)	(ns)	Secup (ns)	(ns)	seew (n	•)	
Asynchronous to Register A SX Pin to Pin Input to Output	-	Q_int[18]:CLK	Q_int[19]:D	0.716	0.159	4.810	4,969	0.298	1.091	1	0.077	. (4
<ul> <li>R Pin to Pin</li> <li>Input to Output</li> </ul>		40 - 4 - 4	and the second s					arese.			10000	
Input to Output	12	Q_int[25]:CUK	Q_int[20]:0	0.704	0.164	4,809	4,973	0.298	1.050		0.054	
	3	Q_int[11]:O.K	Q_int[12]:D	0.688	0.174	4.823	4.997	0.298	1.076	5	0.090	
🖂 User Sets							2010 2010	1.00000000			100000	
	4	Q_int[5]:CLK	Q_int[6]:D	0.712	0.177	4.832	5.009	0.298	1.073	3	0.063	
		100000000						10000			10000	
	5	Q_int[7]:CLK	Q_int[8]:D	0.706	0.182	4.827	5.009	0.298	1.058	8	0.054	
	6	Q_int[19]:OUK	Q_int[20]:D	0.701	0.219	4.777	4.995	0.298	1.031	1	0.032	
30	7	Q_int[26]:CLK	Q_int[27]:D	0.673	0.245	4.753	4,998	0.299	1.005	5	0.033	
30		C.d.d.e.	C. de la									
	Na			Туре	Net			Mac	ro Op	Delay Total Fan	out Edge	
24	1	Summary										
45		data required tin								4.973		
		data arrival time								4.809		
		slack Data_arrival_time_c								0.104		
-18		Data_arrival_time_c my_clk	alculation							0.000 0.000		
		CLK		Clock source						0.000 0.000		-
		CLK_ibuf/U0/U_1	OPAD-PAD	net	CLK					0.000 0.000	1	
		CLK_ibuf/U0/U J		cell	CLA			ADU	BIOPAD IN +	2.128 2.128	21	
12		CLK_ibuf_RNIVQ		net	CLK_ibu			HOL		0.197 2.325	1	
		CLK_ibuf_RNIVQ		cell	culous			4011	B:GBM +	0.105 2.430	51	
			04/U0 RGB1 RGB1:An		CLK ibur	RNIVQ04/U0	Ville	- Corta	0.00111	0.691 3.121		
			04/U0_RGB1_RGB1:YL		Curciou.	fault dan ca		60L1	B:RGB +	0.372 3.493	6 r	
6		Q_int[25]:CLK		net	CIK dur	RNIVQ04/U0	PGR1 PGR1 m		Dinob	0.612 4.105		
		Q int[25]:Q		cell				ADU	R-SLF +	0.102 4.207	2 1	
		Q_int[26]:D		net	Q_c[25]			-00		0.602 4.809		
		data arrival time			and and					4,809		
0 0.0635 0.159 0.2545 0.35 0.4	45 4	Data required time										
slack distribution(ns)		my_clk		Clock Constra	int					1.250 1.250		

Figure 52 · SmartTime Register to Register Delay

4. Double-click a path row to open the Expanded Path window. The window shows a calculation of the data arrival and required times along with a schematic of the path (as shown in the figure below).

**Note:** The Timing Numbers in these reports may vary slightly with different versions of the Libero Software, and may not be exactly the same as what you will see when you run the tutorial.



SmartTime - [Maximum Delay - Expanded P	ath view From Q	int[25]/CLK -> To: Q_int[26]/D]									- 0 ×
File Edit View Tools Help											- 8
H 2 2 3 2 2 6 0 0	a x										
Summary for path from: Q_int[25]:CLK fo: Q_int[26]:D										Path Profile Cell Delay 0.0016	
Data Required Time (ns) Data Arrival Time											
4.973 4.809	0.164										
Name	Туре	Net	Macro	Op	Delay	lotal	Fanout Edge				
<ul> <li>Data_arrival_time_calculation</li> </ul>						0.000					
my_clk											
CLK	Clock source			+		0.000					
CLK_ibuf/U0/U_JOPAD:PAD	net	CLK		+		0.000					
CLK_ibut/U0/U_IOPAD:Y	cell		ADLIB:JOPAD_I	N +		2.128					
CLK_ibuf_RNIVQ04:An	net	CLK_ibuf		+		2.325					
CLK_ibuf_RNIVQ04:YWn	cell		ADLIB:GBM	+	0.105						
CLK ibuf RNIVQ04/U0_RGB1_RGB1:An	net	CLK_ibuf_RNIVQ04/U0_YWn		+:	0.691	3.1.21	f				
CLK_ibuf_RNIVQ04/U0_RGB1_RGB1:YL	cell		ADLIB:RGB	+	0,372	3,493	6 1				
Q_int[25]:CLK	net	CLK_ibuf_RNIVQ04/U0_RGB1_RGB1_rgbl_net_1	Contraction of the second	+	0.612	4.105					
Q_int[25]:Q	cell		ADLIB:SLE		0.102	4.207	21				
Q_int[26]:D	net	Q_c[25]	T IN BRIDE	+		4,809					
data arrival time	ince	d_dbj				4.809					
	CLK_buf/U0/	U_IOPAD CLK_buf_RNIVQ04					OLD BUE	RNIVQ04/U0_RGE	IL DODD	Q_int[26]	
							CLK_DUI	KNIVQ04/00_KG	SI_RGBZ		
	PAD	Y An YEn								ADri	
	IOPAD	151						ENn YR		11-1	
	TOPAU	IN ENn YWn								ALIN	
	200	The rest Well STRATSTORAD									
	B111	Contrast des lo justices de la participation						O Sufari		0 0	
								Q_int[25]		0 Q	
								ADO		EN	
							-				
			CLK_buf_F	RNIV	204/00	U_RGI	BI_RGB1	ALD		LAT	
				An						- 50	
				ENI	n Y	R				SEn	
								LAT			
								-sp			
								SLE			
4											741
A2.5											
										Temp: 0 - 85 C Volt: 1.14 - 1	26 V Speed: STD
				_	_	_				longer and longer and	

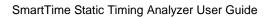
Figure 53 · Register-to-Register Expanded Path View

5. Select **External Setup** to display the Input to Register timing. Select **Path 3**. The Input Arrival time from the EN pin to Q\_int[27]:EN is 4.547 ns (as shown in the figure below).

	nalvisi Vev															
		-														_
	Analysis for scenario Primary	Pri	am •						то =							
	mmary W my_clk	0	ustomize table									Apply P	lter	Store Fil	Reset f	ilter
	<ul> <li>Register to Register</li> <li>External Setup</li> </ul>		Source Pin	Sink	Pin De	day 15)	Slack (ns)	Arrival (ns)	Required (ns)	Setup (ns)	External Setup (ns)					
	Clock to Output Register to Asynchronous External Recovery	1	EN	Q_int[31]:EN		4,547		4.547		0.399	1.258					
	Asynchronous to Register	2	ÐN	Q_int[30]:EN		4.547	_	4.547		0.399	1.248					
	Input to Output User Sets	1	Bi	Q_HII(27):EN		1.517		4.547		0.399	1.246					
		4	EN EN	Q_int[29]:EN		4.547		4.547		0.399						
		pine a	and the second se	O int[28]:EN		No Vesca		4.547		0.399	- 101054					-
			me Summary		Туре	Ne	et				Macro	Op	Delay	lotal h	anout Edge	
- 22			data required time data arrival time											N/C 4.547		
			slack									12		N/C		
			Data arrival time calco	dation										in c		
			EN										0.000	0.000	F	
			EN_ibuf/U0/U_IOPA	D-PAD	net	EN							0.000	0.000		
			EN_ibuf/U0/U_IOPA		cell						ADLIBJOPAD IN	1	2.720		11	
- 1			EN_ibuf/U0/U_IOINF		net	EN	ibuf/00/	O/TRAT			Horandoren III	1.1	0.000			
			EN_ibuf/U0/U_IOINI		cell		0000000	iner			ADUBIOINEF_BYPAS		0.106		32 f	
- 1			Q int[27]:EN		net	EN	10.				ACCESSION CONTRACT	-	1.721			
- 1	1212 122 124		data arrival time		- rest	1.14	24						arrak	4.547		
- 1	This set has no path.		Data_required_time_ca	Indation												
		1	my_clk	CUMUON									MIC	N/C		
			CLK		Clock source								0.000		1000	
- 1				0.040		CL	v					+	0.000			
- 1			CLK_ibuf/U0/U_IOP		net	cl	κ.						1.915		21	
- 1			CLK_ibuf/U0/U_IOP/		cell						ADLIB:JOPAD_IN	•	0.177		21	
- 1			CLK_ibuf_RNEVQ04:/		net	CL	K_ibuf					+			1.1	
		CLK_ibuf_RNDVQ04:YWn cell					-			ADLIB:GBM	•	0.095		5 f		
- 1			CLK_ibuf_RNIVQ04/			CL	K_ibuf_RJ	VIVQ04/U0	YWn			+	0.623	N/C	1	
- 1			CLK_ibuf_RNIVQ04/	JO_RGB1_RGB3:YL							ADLIB:RGB	+	0.335		5 e	
- L			Q_int[27]:CLK		net		K_ibuf_RI	UVQ04/U0	RGB1_RGB3_	rgbl_net_1			0.553			
	slack distribution(ns)		Q_int[27]:EN		Library setup ti	me					ADUB:SLE	12	0.399	N/C		

Figure 54 · SmartTime - Input to Register Path Analysis

6. Select **Clock to Output** to display the register to output timing. Select Path 1. The maximum clock to output time from Q\_int[16]:CLK to Q[16] is 9.486ns.





1 2	x 🐵 S 🍡 🗲 🖞 🗖													
num Dei	ay Analysis View													
~	Bootstand St.													
MAX	Analysis for scenario Primary	Fro	201 *					то •	0					
	Summary è my_clk		ustomize table								Apply P	lter 5	tore Niter	Piter
	Register to Register     External Setup		Source Pin	Sink	Pin	Delay	Slack	Arrival (ns)	Required	Clock to 0	ut (ns)			
	Clock to Output					(ns)	(ns)	, and a final first firs	(ns)					
	Register to Asynchronous	1											6	-
	External Recovery		Lease and the second											1
	Asynchronous to Register	2	Q_int[15]:CLK	Q[15]		5.354		9.461				9.46	1	
	🄀 Pin to Pin	3	Q_int[28]:CLK	Q[28]		3.946		8.054				8.05	4	
	Input to Output	1	Contention.	disol		2.340		0.034				0.02	3	
	Der Sets	4	Q_int[4]:CLK	Q[4]		3.817		7.937				7.93	7	
				2.5										
		Nat	me		Туре	Net				Macro	Op De	lay Total	Fanout Edge	
			Summary											
_		_	data required time									N/0		
			data arrival time									9,48		
			slack									N/0	0	
			Data_arrival_time_calco	lation								000 0.00		
			my_clk CLK		Clock source							000 0.00		
			CLK_ibuf/U0/U_IOP/	D-BAD		CLK						000 0.00		
			CLK_ibuf/U0/U_IOP/		cell	LLN				ADLIB:OPAD IN		128 2.12		
			CLK_ibuf_RNIVQ04:/			CLK_ibuf				Housever and		197 2.32		
			CLK_ibuf_RNEVQ04:1		cell	cen jour				ADUB:GBM		105 2.43		
			CLK_ibuf_RNIVQ04/			CLK ibuf	RNIV004	/U0_YWn				687 3.11		
	10 - 11 - 11		CLK_ibuf_RNEVQ04/							ADLIB:RGB	+ 0	372 3.48	9 8 r	
	This set has no path.		Q_int[16]:CLK			LK ibuf	RNIVQ04	/U0_RGB1_RGB0	rgbl_net_1		+ 0	618 4.10	7 1	
or parts			Q_int[16]:Q		cell					ADLIB:SLE	+ 0	127 4.23	4 2 f	
			Q_obuf[16]/U0/U_IC	OUTFF:A	net (	2_c[16]						671 5.90		
			Q_obuf[16]/U0/U_IC	OUTFF:Y	cell					ADLIB:IOOUTFF_BYPASS		403 6.30		
			Q_obuf[16]/U0/U_IC			2_obuf[10	]/U0/DO	UT				.000 6.30		
			Q_obuf[16]/U0/U_I0	PAD:PAD	cell					ADLIB-IOPAD_TRI		178 9.48		
			Q[16]		net (	2[16]					+ 0	.000 9.48		
			data arrival time									9.48	b	
			Data_required_time_ca	lculation										
	L		my_clk									N/C N/0		
			CLK		Clock source						+ 0	1000 N/0		
	slack distribution(ns)		Q(16)									r4/(	<u> </u>	

Figure 55 · SmartTime Clock to Output Path Analysis

# Minimum Delay Analysis with Timing Analyzer - 32-Bit Shift Register Example

The SmartTime Minimum Delay Analysis window identifies any hold violations that exist in the design.

To perform Minimum Delay Analysis:

1. From the SmartTime Analysis window, choose **Tools > Minimum Delay Analysis**. The Minimum Delay Analysis View appears, as shown in the figure below.



um Delay	l 🤷 達 🗲 2 🐵 🌫 / Analysis View										
0	88999 - WA										
2	Analysis for scenario timing_analysis	Design			shift_reg32						
	ummary	Family			SmartFusion2						
	@ my_clk	Die			M2S090TS						
	✓ Register to Register	Package			484 FBGA						
	External Hold Clock to Output	Temperat	ure Rang	ge	0 - 85 C						
	Register to Asynchronous	Voltage F	lange		1.14 - 1.26 V						
	External Removal Asynchronous to Register	Speed G	rade		STD						
4.3	R Pin to Pin	Design S			Post-Layout						
	Input to Output	· Data sou			Production						
		Min Oper	ating Co	oditions	BEST - 1.26 V	-0C					
		Max Ope	-		WORST - 1.14						
1			-		timing analysis						
	Select a set of paths to see	Summ	ary								
	its slack distribution.	Clock Domain		Frequency (MHz)	Required Period (ns)	Required Frequency (MHz)	External Setup (ns)	External Hold (ns)	Min Clock- To-Out (ns)	Max Clock- To-Out (ns)	1
		my_clk	1.640	609.756	4.000	250.000	1.297	0.510	3.781	9.880	]
l			A	lin Delay (n	s) Max Delay	(ns)					
		low to (	Dutput N	VA	N/A	1 - 24 - C					

Figure 56 · SmartTime Minimum Delay Analysis View- Summary

- 2. Expand **my\_clk** to display Register to Register, External Hold, Clock to Output, Register to Asynchronous, External Removal and Asynchronous to Register path sets.
- 3. Click **Register to Register** to display the reg to reg paths. The window displays a list of register to register paths and detailed timing analysis for the selected path. Note that all slack value are positive, indicating that there are no hold time violations.
- 4. Click to select the first path and observe the hold analysis calculation details, as shown in the figure below.

Analysis for scourse           Analysis for scourse           * We may ch * Register to Register External Removal Adjusticineous to Register External Removal Adjusticineous to Register * XE this Feis         Frem *         To *           * Summary Register to Asynchronous External Removal Adjusticineous to Register * XE this Feis         Source Pin         Sakk Pin         Octary (ny)         Stack Adjusticineous to Register 2 (2 prt[22] (DL         Option (12 prt[22] (DL	Delay Analysis Weir															
Number       Notice       Number       Numer       Number       Number	Analysis for commun															
Charactery       Active File       Active File       Reset File	Dimary	E.						10								
• · · · · · · · · · · · · · · ·	B Summan							10			10000		194			
Negative to Register         Source Pie         Sink Pie         Debay         Kande         Hold         Source           Lotent Hold         Clock to Cutput         Register to Register         0.200		0	ustomize table								Apply	Filter	Stor	e Filter	Reset	iter.
Clock to Culput Register to Synchronous External Removal Asynchronous to Register Input to Congut         Value (N)	🖌 Register to Register	· · · · ·														
Literard Removed Asynchronous to Register Asynchronous to Register Subsersets         C Curl(25) CuC (2 Curl(25)CuC 2 Curl(2	Clock to Output	1	Source Pin	Sink	Pin		Slack (ns)									
3         2         Q_mitta Pin         0.399         0.359         2.442         2.199         0.000         0.039           3         Q_mitta Pin         0.399         0.353         2.442         2.199         0.000         0.039           3         Q_mitta Pin         0.399         0.353         2.442         2.199         0.000         0.039           4         Q_mitta Pin         0.399         0.357         2.446         2.199         0.000         0.039           5         Q_mitta Pin         0.397         0.361         2.449         2.19         0.000         0.039           6         Q_mitta Pin         0.397         0.361         2.449         2.19         0.000         0.039           24         Q_mitta Pin         0.397         0.361         2.449         2.205         0.000         0.000           24         Q_mitta Pin         0.397         0.361         2.449         2.205         0.000         0.000           24         Q_mitta Pin         0.397         0.321         2.457         2.205         0.000         0.000           24         Q_mitta Pin         0.397         0.321         2.447         2.205         2.449	External Removal	1.	ð"hut[58] ignik	Q_int[00]10		0,286	0.250	2.439	2,189	0.000	9.036					
X         User Sets         3         Q_int[3]:Q_iX         Q_iX<	4 💢 Pin to Pin	2	Q_int[28]:XUK	Q_int[29]:D		0.289	0.253	2.442	2.189	0.000	-0.036					
30         31         2.460         2.160         0.000         4.036           24         0         0.007         0.367         0.361         2.460         0.000         4.036           24         0         0.007         0.367         0.361         2.460         0.000         4.036           24         0         0.007         0.367         0.367         0.362         2.467         2.000         0.040           24         0         0         0.007         0.367         0.367         0.362         2.467         0.000         4.045           38         0         0         0.007         0.367         0.367         0.367         0.367         0.364         0.000         4.045           38         0         0.007         0.000         0.000         1.000         0.000         1.000         0.000         1.000         0.000         1.000         0.000         1.000         0.000         1.000         0.000         1.000         0.000         1.000         0.000         1.000         0.000         1.000         0.000         1.000         0.000         1.000         0.000         1.000         0.000         1.000         1.000         0.000		3	Q_int[15]:OJK	Q_int[t6]:D		0.293	0.257	2.446	2.189	0.000	-0.036					
Marce         Type         Net         Marce         Op         Delay         Total         Fanut         Constraint         <		4	Q_int[16]:CLK	Q_int[17]:D		0.296	0,260	2.449	2, 189	0.000	-0.036					
30         Time         Type         Net         Macro         Op         Delay         Total         Fanue         E           24         4		5	Q_int[27]:OLK	Q_jnt[28]:0		0.297	0.261	2.450	2.189	0.000	-0.036					
Name         Type         Net         Marcin         Op         Delay         Total         Famou Ea           24		6	Q_int[10]:CLK	Q_W[11]:D		0.307	0.262	2.467	2.205	0.000	-0.045					
24         data annual time         2.439           18         data annual time         2.189           18         tock         0.200           19         Data annual time, calculation         0.000           10         Click induction         0.000           10         Click induction         0.000           12         Click induction         0.000           12         Click induction         0.000           14         Click induction         0.000           15         Click induction         0.000           16         Click induction         0.000           17         Click induction         0.000           18         Click induction         0.000           19         Click induction         0.000           10         Clipe         0.000           11         Click induction         0.000           12         Click induction         0.001           13         Click induction         0.001           14         Click induction         0.001           15         Click induction         0.001           16         Click induction         0.001           Click induction	30	Na	me	-	Type	Ne	e		_		Macro	Op	Delay	Total	Fanout Ex	ige
13         data required time         - 2.139           13         data required time         0.200           14         Data, arrival, time, calculation         0.200           12         CLK, but/10/U_UOPAD.PAD         Clock source         - 0.000           12         CLK, but/10/U_UOPAD.PAD         net         CLK         + 0.000         0.000           14         CLK, but/10/U_UOPAD.PAD         net         CLK         + 0.000         0.000         r           12         CLK, but/10/U_UOPAD.PAD         net         CLK, but         + 0.000         0.000         r           14         CLK, but/10/U_UOPAD.PAD         net         CLK, but         + 0.000         0.000         r           12         CLK, but/10/U_UOPAD.PAD         net         CLK, but         + 0.000         0.000         r           14         CLK, but/10/U_UOPAD.PAD         net         CLK, but         + 0.000         0.000         r           15         CLK, but/10/U_UOPAD.PAD         net         CLK, but/10/U_UOPAD.PAD         + 0.000         0.000         r           16         CLK, but/10/U_UOPAD.PAD         net         CLK, but/10/U_UOPAD.PAD         + 0.000         0.000         r           17         CLK,																-
iBc         jsck         0.200           Justa gravha time, cakutetion         0,000         c           mj_cik         Clock tource         0,000         oct           CLK_indr/MU/UJOADSPAD         net         CLK         0,000         oct           12         CLK_indr/MU/UJOADSPAD         net         CLK         0,000         oct           6         CLK_indr/MU/UJOADSPAD         net         CLK         0,000         r.           12         CLK_indr/MU/UJOADSPAD         net         CLK         0,000         1,000	24															
13 <b>J J J J J J J</b>																
13         my_c/k         0,000         0,000           CLK_bit/RNU_DVLDAPAD         Clock issure         0,000         0,000           12         CLK_bit/RNU_DVLDAPAD         Clck         0,000         0,000           12         CLK_bit/RNU_DVLDAPAD         clck         0,000         0,000           13         CLK_bit/RNU_DVLDAPAD         clck         0,000         0,000           14         ADLESIDAD_IN         1,000         1,000         0,000           15         CLK_bit/RNU_OVL/DAPAD         cell         ADLESIGEM         0,000         1,000           16         CLK_bit/RNU_OVL/DAPAD         cell         ADLESIGEM         0,000         1,000 </td <td></td> <td></td> <td></td> <td>anato o</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>0.250</td> <td></td> <td></td>				anato o										0.250		
12         Cick tource         - 0.000 0.000 r           13         Cick tource         - 0.000 0.000 r           14         Cick tource         - 0.000 0.000 r           15         Cick tource         - 0.000 0.000 r           16         Cick tource         - 0.000 0.000 r           17         Cick tource         - 0.000 0.000 r           18         Cick tource         - 0.000 0.000 r           19         Cick tource         - 0.000 0.000 r           10         Cick tource         - 0.000 0.000 r           110         Cick tource         - 0.000 0.000 r           110         Cick tource         - 0.000 0.000 r           110         Cick tource         - 0.010 1.235 1.268 5 r           110         Cick tource         - 0.010 1.001 1.000 1.	19			netion									0.000	0.000		
12         CLK_bbut/UNU/DPADDBAD         net         CLK         + 0.000         0.000         r           12         CLK_bbut/UNU/DPADDBAD         net         CLK_bbut         ADLBS/DBAD,         1.100         1.109         1.29         2           6         CLK_bbut/SRV/ORA/N         net         CLK_bbut         ADLBS/GBM         - 0.010         1.000         5.6           6         CLK_bbut/SRV/ORA/N         net         CLK_bbut/SRV/ORA/N         - 0.035         1.26         5.7           6         CLK_bbut/SRV/ORA/UN_SRGB_RGB3/n net         CLK_bbut/SRV/ORA/UN_SGB1_RGB3/n net         CLK_bbut/SRV/SRV/ORA/UN_SGB1_RGB3/n net         CLK_bbut/SRV/SRV/N net         No108/S12         0.0323         2.135         r           0_imt3010net0_imt3010.0					Clerk and							1			14	
12         CLK_bbut/DAV1_0PAR/Y         cell         ADUBRIORAD_IN +         1.109         2.7           12         CLK_bbut/PAN/QBAA.net         CLK_bbut         ADUBRIGM         0.039         1.109         2.7           6         CLK_bbut/PAN/QBAA.net         CLK_bbut/PAN/QBAV.Wn         ADUBRIGM         0.033         1.206         5.4           6         CLK_bbut/PAN/QBAV.U0_RGB1_RGB3A.net         CLK_bbut/PAN/QBAV.U0_WM         ADUBRIGM         0.033         1.206         5.7           Q_int[23PiCLK         net         CLK_bbut/PAN/QBAV.U0_WGB1_RGB3A.net         CLK_bbut/PAN/QBAV.U0_WGB1_RGB3A.net         ADUBRIGM         4.0338         5.7           Q_int[23PiCLK         net         CLK_bbut/PAN/QBAV.U0_WGB1_RGB3A.net         CLK_bbut/PAN/QBAV.U0_WGB1_RGB3A.net         ADUBRIGM         4.0338         5.7           Q_int[23PiCLK         net         CLK_bbut/PAN/QBV.U0_WGB1_RGB3A.net         CLK_bbut/PAN/QBV.U0_WGB1_RGB3A.net         ADUBRIGM         4.0327         2.233         7           Q_int[23PiCLK         net         CLK_bbut/PAN/QBV.U0_WGB1_RGB3A.net         CLK_bbut/PAN/QBV.U0_WGB1_RGB3A.net         ADUBRIGM         ADUBRIGM         4.0327         2.235         7           Q_int[23PiCLK         net         CLK_bbut/PAN/QBV.U0_WGB1_RGB3A.net         ADUBRIGM         ADUBRIGM         4.032				0.940			ĸ					-				
12         CLK_bbuf SRNOQ04Xn         net         CLK_bbuf         = 0.0141_12.03         +           6         CLK_bbuf SRNOQ04Xn         net         CLK_bbuf         ADUB/GBM         = 0.0351_12/6         5 +           6         CLK_bbuf SRNOQ04Xn0_ROBEL_ROBENA net         CLK_bbuf_RNNOQ04/L0_VWn         = 0.3681_6/31         +         0.378_21/33         r         -         0.378_21/33         r         -         0.378_21/33         1         0.328_21/33         r         -         0.328_21/33         r         -         0.328_21/33         1         -         0.328_21/33         1         -         0.328_21/33							11				ADUB:IOPAD I	N +				
6         CLK_bist/RMVQ04VV/n         cell         ADUB/GBM         - 0.0051 1.208         5 +           6         CLK_bist/RMVQ04VU0_RGBL_RGB3/nt         CLK_bist/RMVQ04VU0_YGBBL_RGB3/nt         + 0.363 1.631         + 0.363 1.631           6         CLK_bist/RMVQ04VU0_RGB1_RGB3/nt         cell         ADUB/RGB         + 0.372 1.235         r           7         Q_intt[29]CLK         net         CLK_bist_RMVQ04/U0_RGB1_RGB3_ngb1_net.1         + 0.322 1.235         r           9         Q_intt[29]CL         cell         ADUB/RGB1_RGB3_ngb1_net.2         + 0.327 2.216         2 r           9         dtts minit time         ret         Q_idtg30;D         net         Q_idtg30;D         2.439         r	12					CL	Kjbuf.					+	0.104	1.213		
6         CLK_buf_R8NQ04U0_RGBL_RGBLAA_net         CLK_buf_R8NQ04U0_RGBL_RGBLAA_net         CLK_buf_R8NQ04U0_RGBL_RGBLAA_net         - 0.361_613_1_61_1_61_1_61_1_61_1_61_1_61_1											ADLIB:GBM	+			5 f	
6         CUK_jibuf_RRMQVQUUD_RGB1_RGB3_VL_cell         ADUERGB         - 0.197 18.88         5 r           Q_int[29]/CLK         net         CUK_jibuf_RRMQV4/UD_RGB1_RGB3_rgb1_net_1         + 0.325 21.55         r           0					net	CL	Kjbuf_RN	avQ04/U0_	YWn			+	0.363	1.631		
Q_int[29]CLK net CLK[bid_F8N/Q04/U0_RGBL_RGB3_tgbL/net_1 + 0.422 2333 r Q_int[30]Q cell ADUBSLE + 0.027 2210 2 r Q_int[30]D net Q_c[29] + 0.228 2439 r ddta.minul.ime							Sector Sector	1000000			ADUB:RGB	+			5 r	
Q_int[30]:D net Q_c[29] + 0.229 2.439 / data anival time 2.439	°					CL	K_ibuf_RN	IVQ04/UD_	RGB1_RGB3_r	gbl_net_1		+				
data arrival time Z439											ADLIB:SLE	+			2 r	
					net	Q.	c[29]						0.229		1	
	0 0.2985 0.25 0.3015 0.353 0.404	1.1												2.439		
0.1985 0.25 0.3015 0.333 0.494	0.2985 0.25 0.3015 0.353 0.404		Data_required_time_ca	lculation												

Figure 57 · SmartTime Minimum Delay Analysis



# Changing Constraints and Observing Results - 32-Bit Shift Register Example

You can use the Constraints Editor to change your constraints and view the results in your design. To do so:

1. Open the Constraints Editor (Constraints Manager > Timing Tab > Edit Constraints with Constraint Editor > Edit Timing Verifications Constraints).

The Constraints Editor displays the clock constraint at 250 MHz that you entered earlier.

Constraints		Syntax	Clock Name	Clock Source	Period (ns)	Frequency	Dutycycle	First Edge	Offset (ns)
<ul> <li>Requirements</li> </ul>		Syntax	Clock Name	Clock Source	Period (ns)	(MHz)	Dutycycle (%)	rirst toge	Offset (ns)
T Clock	1	Click within this row to add			0.000		50.0%	rising +	0.000
Generated Clock									
Input Delay	2	7	my_ck	[get_ports (CLK)]	4.000	250.000	50.000000	rising +	0.000
Output Delay							2 22		
External Check									
Clock To Out									
# Exceptions E									
Exceptions     E     Max Delay									
Max Delay Min Delay									
Max Delay									
Max Delay Min Delay Multicycle False Path									
Max Delay Min Delay Multicycle False Path # Advanced									
Max Delay Min Delay Multicycle False Path Advanced Disable Timing									
Max Delay Min Delay Multicycle False Path Advanced Disable Timing Clock Source Latency—									
Max Delay Min Delay Multicycle False Path Advanced Disable Timing									

Figure 58 · Clock Constraint Set to 250 MHz

- Select the second row. Right click and choose Edit Clock Constraint. This opens the Edit Clock Constraint dialog box. Change the clock constraint from 250 MHz to 800 MHz and click the green check mark to continue.
- 3. Click Open SmartTime > Open Interactively.
- 4. Choose Maximum Delay Analysis View to view the max delay analysis.
- 5. Expand **my\_clk** in the Maximum Delay Analysis window. Click **Register to Register** to observe the timing information. Note that the slacks decrease after you increase the frequency. You may see the slacks go negative indicating Timing Violations. Negative slacks are shown in red.



Analysis for scenario											
MAX thing_analysis	Fr						10	•			
▲ ⓓ Summary ▲ 🗶 my_clk	0	unitomize table								Apply Filter	Store Filter
× Register to Register External Setup	ΙE	Source Pin	Sink Pin	Delay (ns)	Slack (es)	Arrival (ns)	Required (m)	Setup (ns)	Hinimum Period	Skew (ns)	
Clock to Output Register to Asynchronous	1	Q_M(11)-CLK	Q_H4\$12]=D	2.306	-1.574	6.533	4,959	0.299	2.824	0.139	
External Recovery Asynchronous to Register	2	Q_HERICK	Q_M(7):0	1.041	-0.175	5.184	5.009	0.298	1.425	0.086	
✓ X° Pin to Pin Input to Output	3	d"M@licrk	Q_W[1]ID	0.970	-0.102	5.117	5.015	0.298	1.352	0.084	
X User Sets	4	Q_W(20)KLK	Q_W(21).D	0.969	-0.064	5.069	5.005	0.298	1.314	0.047	
	5	Q_MEXER.	Q_W(31).0	0.885	-0.002	5.007	5.005	0.298	1.252	0.069	-
	6	Q_H4[13]:CLK	Q_H(14):D	0.732	0.141	4.845	4.986	0.298	1.109	0.079	
	7	Q_Ht[15]:CLK	Q_H(16]:D	0.731	0.142	4.831	4.973	0.298	1. 108	0.079	
30		Q_H4(22):CLK	Q_Ht[23]:0	0.721	0.148	4.857	5.005	0.298	1. 102	0.083	
	9	Q_H6[18]:CLK	Q_Ht[15]:D	0.722	0.150	4.835	4.985	0.298	L 100	0.080	
24	50	Q_INE[30]:CLK	Q_Ht[1]:D	0.730	0.155	4.865	5.020	0.298	1.095	0.067	
	11	Q_M(28):CLK	Q_M(29):D	0.713	0.170	4.834	5.004	0.298	1.080	0.069	
18	12	Q_ME12]:CLK	Q_M[13]ID	0.715	0.184	4.800	4,984	0.298	1.066	0.053	
12	Na			Type	Net			Ma	cro Op	Delay Total Fanout Edge	
		Summary data required tin data arrival time slack	ч							4.959 6.533 -1.574	1
		Data_arrival_time_c my_clk CLK		Clock source	CLK					0.000 0.000 r 0.000 0.000 r 0.000 0.000 r	
0		CLK, Bull V0/U J		cell	CLK			AD	IBJORAD IN -	0.000 0.000 r 2128 2128 2 r	

Figure 59  $\cdot$  Maximum Delay Analysis After Setting Clock Constraint to 800 MHz

Note: The actual timing numbers you see may be slightly different.

6. Close SmartTime. Click No when prompted to save changes.

### **Tutorial 2 - False Path Constraints**

This section describes how to enter false path constraints in SmartTime. You will import an RTL source file from the design shown below. After routing the design, you will analyze the timing, set false path constraints, and observe the maximum operating frequency in the SmartTime Timing Analysis window.

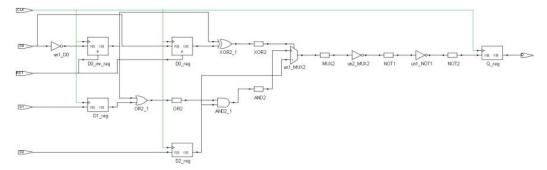


Figure 60 · Example Design with False Paths

### Set Up Your False Path Example Design Project

- 1. Open Libero and create a new project (from the Project menu, choose New Project).
- 2. Name the project **false\_path** and set the project location according to your preferences. Click **Next**. Enter the following values for your Device Selection settings:
  - Family: SmartFusion2
  - **Die**: M2S050
  - Package: 484 FBGA



- Speed: STD
- Die Voltage: 1.2 V
- Range: COM
- 3. Click **Finish** to create the new project.

### Import the false\_path Verilog File and Add Constraints

You must import the <u>false\_path.v</u> Verilog source file into your design for this tutorial. Then run Libero SoC.

#### To import the Verilog Source File:

- 1. From the File menu, choose Import > HDL Source Files.
- 2. Browse to the location of the false\_path.v you saved and select it. Click **Open** to import the file.
- 3. Verify that the file appears in Design Hierarchy
- 4. In the Design Flow window, double-click **Synthesize** to run synthesis. A green check mark appears when the Synthesis step completes successfully.
- 5. Expand Edit Constraints. Right-click Timing Constraints and choose Open Interactively.
- 6. Double-click on **Manage Constraints**. Select the Timing tab, pull down the **Edit with Constraint Editor** sub-menu, and select the "Edit Place and Route Constraints". The Constraints Editor will open.
- 7. Double-click on the Requirements: Clock and the Create Clock Constraint dialog box will open.
- 8. Double click the browse button for Clock Source, and select CLK; name it clk (or whatever you want).
- 9. Set the frequency to be 100 MHz.

Create Clock Constraint	Charle Sources a	[get_ports { CLK } ]		? X
Clock Name : clk	Clock Source :	[get_ports { CLK } ]		
Period : 10	ns	Hor Frequency:	100	Mhz
		1		
Offset : Duty cycle :				
0.000 ns 50.0000 %				
Add this clock to existing one with same source				
Comment :				
Help		ОК	Ca	Incel

Figure 61 · Clock constraint of 100MHz

• Click OK to return to the Constraints Editor and observe that the clock information has been filled in as shown in the figure below.

File Construints Restore	Help										
M SA SA SA FO PA	2.	M.	🔉 😕 🗇 🐮	0							
onstraints Editor											
Constraints     Requirements	•		Syntax	Clock Name	Clock Source	Period (ns)	Frequency (HHz)	Dutycycle (%)	First Edge	Offset (ns)	Waveform
Clock Generated Clock		1	Click within this row			0.000		\$0.0%	rising	0.000	0.00 0.00 G
Input Delay Output Delay		2	*	đ.	[get_ports {CLK }]	10.000	100.000	50.000000	rising	0.000	0.00 5.00 U
External Check Clock To Out Exceptions Max Delay											

Figure 62 · Clock Constraint of 100 MHz in false\_path design

10. Save your changes (File > Save) and close the Constraints Editor (File > Close).



11. In the Constraint Manager, check the checkbox under Place and Route and the checkbox under Timing Verification to associate the constraint file to both tools. The constraint file is used for both Place and Route and Timing Verification.

# Place and Route Your FALSE\_PATH Design

### To run Place and Route on false\_path design:

1. In Libero SoC, right-click Place and Route and choose Configure Options.

Layout Options	8 23
∏ ▼ Timing-driven	
Power-driven	
I/O Register Combining	
Global Pins Demotion	
Driver Replication	
High Effort Layout	
Repair Minimum Delay Violations	
Configure	
Help Of	Cancel

### Figure 63 · Layout Options Dialog Box

- 2. Click the checkbox to enable Timing-Driven layout in Layout Options and leave the other values unchecked. Click **OK** to close the Layout Options dialog box.
- 3. Right-click Place and Route and choose Run.

A green check mark appears next to Place and Route in the Design Flow window when Place and Route completes successfully.



Design Flow			₽×
Top Module(root): false_path	-	0	ø
Active Synthesis Implementation: synthesis			
Tool			
🖻 🕨 Create Design			- 1
- 🖧 System Builder			
- 🖧 Configure MSS			
Create SmartDesign			
Create HDL			
🔛 Create SmartDesign Testbench			
Create HDL Testbench			
Generate Memory Map			
Verify Pre-Synthesized Design			
Simulate			
Constraints			
Manage Constraints			
V 🗇 🕨 Implement Design			
- Q: Netlist Viewer			
V Synthesize			
Verify Post-Synthesized Design			
• Generate Simulation File			
🔤 🚟 Simulate			
Configure Flash*Freeze			
Configure Register Lock Bits			
V Place and Route			
Verify Post Layout Implementation			
• Generate Back Annotated Files			
- 🚆 Simulate			_
🗠 🔯 Verify Timing			
🗠 😋 Open SmartTime			
🖹 🖹 Verify Power			
IO Analyzer			
Mi CCNI Apply Tor			

Figure 64 · Synthesize and Place and Route Successful Completion

# **Timing Analysis - Maximum Clock Frequency**

The SmartTime Maximum Delay Analysis View displays the design maximum operating frequency and lists any setup violations.

### To perform Maximum Delay Analysis:

1. Expand Verify Post Layout Implementation. Right-click Open SmartTime and choose Open Interactively to open SmartTime. The Maximum Delay Analysis View appears (as shown in the figure below). The Maximum Delay Analysis View displays a summary of design performance and indicates that the design will operate at a maximum frequency of 442.48 MHz.

Note: You may see a slightly different maximum frequency with a different version of Libero SoC.



	n Delay Analysis View										0
m Delay	Analysis View										
	Analysis for scenario	<b>D</b> (4)					1				
AX	timing_enalysis	Design				_path rtFusion2	-				
Sh Su	ammary	Family									
	Register to Register	Die			M2S		-				
	External Setup	Package				FBGA					
	Clock to Output	Temperatu	and a local and a strength of the		0 - 8	5 C					
	Register to Asynchronous External Recovery	Voltage R	ange		1.14	- 1.26 V					
	Asynchronous to Register	Speed Gr	ade		STD						
4 55	E Pin to Pin	Design St	ate		Post	-Layout					
- 25	Input to Output User Sets	Data sour	ce		Prod	uction					
		Min Opera	ting Cond	tions	BES	T - 1.26 V - 0 C					
		Max Oper	ating Cond	litions	WOF	RST - 1.14 V - 85 (	2				
		Scenario	Scenario for Timing Analysis timing_analysis								
E											
		Summa	ary								
		Clock Domain	Period (ns)	Freque (MHz)	ency	Required Period (ns)	Required Frequency (MHz)	External Setup (ns)	External Hold (ns)	Min Clock-To- Out (ns)	Max Clock-To- Out (ns)
- I	Select a set of paths to see	clk	2.294	435.92	0	10.000	100.000	0.114	0.791	5.333	10.355
	its sleck distribution.		Min Delay (ns) Max Delay (ns)								
			Input to Output N/A								
		in the O				lax Delay (ns)					

Figure 65 · Maximum Delay Analysis Summary

- 2. Expand **clk** to expand the display and show the Register to Register path sets.
- 3. Select **Register to Register** to display the register-to-register paths. Notice that the slack values are positive.
- Double-click to select and expand the row in the path list with the path is from the CLK pin of flip-flop D0\_reg to the D input of flip flop Q\_reg. Note that the path goes through the S input of multiplexer un1\_MUX2.

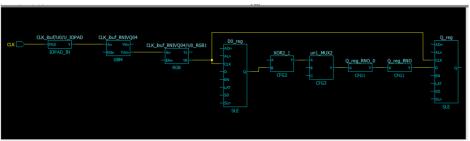


Figure 66 · Expanded Path

Looking at the code in false\_path.v, we can see on lines 51 and 52, that D0\_reg and D)\_inv\_reg are always the inverse of each other in "operational" mode (ie except for when RST is active). Line 56 says that XOR2 is the XOR of these two signals, and hence always 1 (again, except for when RST is active). And finally line 59 says that XOR2 is the select of MUX2.

We might reasonably decide that we are not interested in the reset mode delay for this design; and hence this path is a false path for our timing analysis purposes.



```
43
         if (RST)
44 🕂
         begin
45
             D0 reg
                          <= 1'b0;
46
             D0 inv reg
                          <= 1'b0;
47
         end
48
49
         else
50
         begin
51
             D0 reg
                          <= D0;
52
             D0 inv reg
                          <= ~D0;
53
         end
54
    end
55
56
    assign XOR2 = D0 reg ^ D0 inv reg;
57
    assign OR2 = D0 inv reg || D1 reg;
58
    assign AND2 = OR2 && D2 reg;
59
    assign MUX2 = (XOR2) ? (D2 reg) : (AND2);
60
61
```

Figure 67 · Analyzing the false paths

Similar analysis shows that the path from D0\_inv\_reg:CLK to Q\_reg:D shares exactly the same false-path characteristic. We should disable both paths.

- 5. Re-start the Libero Constraints Editor. The Constraints Editor must be running in order for us to use the back-annotation feature of StartTime. Go to the Constraint Manager tab, Timing sub-tab; and again pull down the "Edit with Constraint Editor", and choose "Edit Timing Verification Constraints".
- 6. Leave this running and go back to SmartTime. From the Tools menu select Max Delay Analysis.
- 7. To set the path from D0\_inv\_reg:CLK to Q\_reg :D as false, select the row containing this path in the Register to Register path set, right-click and choose Add False Path Constraint (as shown in the figure below). The Set False Path Constraint dialog box appears (it may pop-behind; check other Constraint Manager windows).

2 2 3 2 2 6 9 2											
m Delay Analysis View											
Analysis for scenario Primary	E	om =					Tr				
Summary		ustomize table								Apply Filter	Store Filter
Clock to Output Register to Asynchronous		Source Pin	Sink Pin	Delay (ns)	Slack (ns)	Arrival (ns)	Required (ns)	Setup (ns)	Minimum Period (ns)	Skew (ns)	
External Recovery Asynchronous to Register	1	D0_aw_reg:CLK	Q_reg:D	1.906	7.740	5.687	13-627	0.298	2.260	0.056	
X Pin to Pin     Input to Output     St User Sets	2	D0_reg:CLK	Copy Print		7.882	5.745	13.627	0.298	2.118	0.066	
Sc userses	3	D1_reg:OLK	Add False Path	Constraint	7.896	5.731	13.627	0.298	2.104	0.067	
	4	D2_reg:CLK	Add Max Delay Add Min Delay	Constraint 6	8.294	5.333	13.627	0.298	1.706	0.067	
			Add Multicycle	Path Constraint							
			Expand selected	i paths							

Figure 68 · Right-Click > Add False Path Constraint



Set False Path Constraint	? <mark>×</mark>
From :	
þ0_inv_reg:CLK	<b>^</b>
< · · · · · · · · · · · · · · · · · · ·	-
Through :	
	^
	-
< · · · · · · · · · · · · · · · · · · ·	
To :	
Q_reg:D	· ···
	*
<	
Comment :	
Help	Cancel

Figure 69 · Set False Path Constraint Dialog Box

- 8. **Click** OK to close the Set False Path Constraint dialog box.
- 9. Check the Constraints Editor window, there should now be an entry under Exceptions > False Path
- 10. Return to the SmartTime window and repeat for the D0\_reg:CLK -> Q\_reg:D path.
- 11. Since we are only interested in timing analysis through the MUX when select = 1, we can also ignore the MUX "0" path from D1\_reg:D through the AND2. We make this a false path, also.
- 12. At this point the Constraints Editor should now look as follows. Save the file and exit the Constraints Editor and SmartTime.



ile Constraints Tools Edit Help     🛃 🎦    ૠ 🍇 👺 ¥⊠			T\PF2.2\false_path\false_path.prj	x] - [constraints cui		_
Constraints Editor straints Editor						-
E Constraints						
Requirements		Syntax	From	Through	То	File
V Clock Generated Clock	1	Click withi				GUI
···· Input Delay ···· Output Delay	2	٣	[get_pins {D0_inv_reg/CLK }		[get_pins { Q_reg/D } ]	X:\sandhya\de
External Check	3	٣	[get_pins { D0_reg/CLK } ]		[get_pins { Q_reg/D } ]	X:\sandhya\de
Exceptions Max Delay	4	*	[get_pins { D1_reg/CLK } ]		[get_pins { Q_reg/D } ]	X:\sandhya\de
<ul> <li>Advanced</li> <li>Disable Timing</li> <li>Clock Source Latency</li> <li>Clock Uncertainity</li> <li>Clock Groups</li> </ul>		1				
4 <b>+</b>						

Figure 70 · False Path Constraints in the SmartTime Constraint Editor

- 13. Place and Route is now invalidated, and needs to be re-run before we can do timing analysis again. This is because we have changed the constraint file that we are using for both P&R and for Timing Analysis. It is possible to use different constraint files, in which case we would not need to re-run P&R.
- 14. Right-click on **Open SmartTime** and choose **Update and Open Interactively**. You will see that Place and Route is run automatically before SmartTime is re-started.
- 15. View the summary in the Maximum Delay Analysis View (**Tools > Max Delay Analysis**). Note that SmartTime now reports the maximum operating frequency as 586.17 MHz, as shown in the figure below.

Note: The maximum operating frequency may vary slightly with a different version of the Libero software.

	🞦 🕄 🏂 🗲 🕫 📨										
um Delay	r Analysis View										
-	Analysis for scenario										
TAX	Primary	Design			false_path						
	immary immy_clk	Family	Family Die		SmartFusio	on2					
4 1		Die			M2S050						
Register to Register External Setup Clock to Output		Package	Package		484 FBGA						
		Temperatur	Temperature Range		0 - 85 C						
	Register to Asynchronous	Voltage Ra	Voltage Range		1.14 - 1.26 V						
	External Recovery Asynchronous to Register	Speed Gra	Speed Grade		STD						
4 35	Pin to Pin	Design State Data source		Post-Layout							
~	Input to Output				Production						
St. User Sets		Min Operating Conditions		ons	BEST - 1.26 V - 0 C						
		Max Opera	ting Condit	ions	WORST - 1	1.14 V - 85 C					
		Scenario fo	r Timing Ar	nalysis	Primary						
•	Select a set of paths to see its slack distribution.	Summa Clock Domain	Period (ns)	Frequ (MHz)		equired eriod (ns)	Required Frequency (MHz)	External Setup (ns)	External Hold (ns)	Min Clock-To- Out (ns)	Max Clock-To- Out (ns)
		my_clk	1.706	586.1	166 10	.000	100.000	-0.025	0.753	5.117	9.781
					_				1		
10	0		0.0.00	Delay (r	ns) Max De	elay (ns)					
	slack distribution(ns)	Input to Ou	tput N/A		N/A						

Figure 71 · Maximum Delay Analysis View - Summary



16. Select the Register to Register set for my\_clk. Observe that only one path is visible, from D2\_reg: CLK to Q\_reg:D. This is the only path that propagates a signal (as shown in the figure below).

🗖 🗅 🍕 🔌 🗲 0 🐵 🌫												
Delay Analysis View												
Analysis for scenario Primary	From *				то							
SI Summary	Customize table								App	ly Filter Sto	ore Filter Reset	Filter
▲ √⊕ my_clk	[											
Register to Register External Setup	Source Pin	Sink Pin	Delay (ns)	Slack (ns)	Arrival (ns)	Required (ns)	Setup (ns	) Minis	mum Pe (ns)	riod	Skew (ns)	
Clock to Output	1 D2_reg:CLK Q_r	reg:D	1.341	8.294	5.333	13.627	0.2	2.0		L 706	0.06	5
Register to Asynchronous	a belleditori (20											1
External Recovery												
Asynchronous to Register												
🌫 Pin to Pin												
Pin to Pin Input to Output												
<ul> <li>Fin to Pin</li> </ul>												
Pin to Pin     Input to Output												
Pin to Pin Input to Output												
Pin to Pin Input to Output												
Pin to Pin Input to Output	Name	Туре		Net		Macro	Ор	Delay	Total F	Fanout Edge		
Pin to Pin Input to Output	4 Summary	Туре		Net		Macro	Op			Fanout Edge		
St Pin to Pin Input to Output ズ User Sets	Summary     data required time	Туре		Net		Macro	Op		13.627	Fanout Edge		
X Pinto Pin Input to Output ズ User Sets	4 Summary	Туре		Net		Macro	Op		13.627 5.333	Fanout Edge		
X Pinto Pin Input to Output ズ User Sets	Summary     data required time	Туре		Net		Macro			13.627	Fanout Edge		
X Pin to Pin Input to Output X User Sets	<ul> <li>Summary data required time data arrival time</li> </ul>			Net		Macro			13.627 5.333	Fanout Edge		
X Pin to Pin Input to Output X User Sets	Summary     data required time     data arrival time     slack     Data_arrival_time_calculat			Net		Macro			13.627 5.333	Fanout Edge		
X Pin to Pin Input to Output X User Sets	<ul> <li>Summary data required time data arrival time slack</li> </ul>	tion	source	Net		Macro		0.000	13.627 5.333 8.294	Fanout Edge		
X Pin to Pin Input to Output X User Sets	<ul> <li>Summary data required time data arrival time slack</li> <li>Data_arrival_time_calculat my_clk</li> </ul>	ntion Clock	source	Net		Macro		0.000	13.627 5.333 8.294 0.000 0.000			
X Pin to Pin Input to Output X User Sets	<ul> <li>Summary data required time data arrival time slack</li> <li>Data_arrival_time_calculat my_clk. CLK CLK ibut/U0/U_JOPAD:</li> </ul>	tion Clock	source				-	0.000 0.000 0.000	13.627 5.333 8.294 0.000 0.000 0.000	r		
X Pin to Pin Input to Output X User Sets	<ul> <li>Summary data required time data arrival time slack</li> <li>Data_arrival_time_calculat my_clk. CLK CLK_ibut/U0/U_JOPAD: CLK_ibut/U0/U_JOPAD:</li> </ul>	tion Clock :PAD net :Y cell	source	CLK		Macro ADLIB:JOPA	-	0.000 0.000 0.000 2.128	13.627 5.333 8.294 0.000 0.000	r		
The first bin       Imput to Output       X       User Sets	<ul> <li>Summary data required time data arrival time slack</li> <li>Data, arrival, time_calculat my.clk CLK CLK, ibut/V0/U_JOPAD: CLK, ibut/V0/U_JOPAD: CLK, ibut/V0/U_JOPAD:</li> </ul>	tion PAD net Y cell net	source			ADLIB:10PA	- + + D_IN + +	0.000 0.000 0.000 2.128 0.352	13.627 5.333 8.294 0.000 0.000 0.000 2.128 2.480	r r 2 r f		
<sup>3</sup> ∑ lin to lin Input to Output User Sets	<ul> <li>Summary data required time data arrival time data, arrival time, calculat my_clk CLK</li> <li>Data_arrival, time, calculat my_clk CLK, ibut/100/U_JOPAD: CLK, ibut/100/U_JOPAD: CLK, ibut/RNIVQ04/MA</li> </ul>	tion Clock PAD net Y cell net (n cell	source	CLK CLK_ibuf	004/10 19/0		- - D_IN + + +	0.000 0.000 0.000 2.128 0.352 0.105	13.627 5.333 8.294 0.000 0.000 2.128 2.480 2.585	r r 2 r		
XPinto Pin Input to Output     XUser Sets	<ul> <li>Summary data required time data arrival time slack</li> <li>Data, arrival, time_calculat my.clk CLK CLK, ibut/V0/U_JOPAD: CLK, ibut/V0/U_JOPAD: CLK, ibut/V0/U_JOPAD:</li> </ul>	tion Clock PAD net Y cell net (n cell _RGB1:An net	source	CLK	Q04/U0_YWn	ADLIB:10PA	- + + D_IN + +	0.000 0.000 0.000 2.128 0.352	13.627 5.333 8.294 0.000 0.000 0.000 2.128 2.480 2.585 3.051	r r 2 r f 1 f		

Figure 72 · Maximum Delay Analysis View - Register to Register

- 17. Close SmartTime.
- 18. Close Libero SoC.

### false\_path.v

```
// Company: Microsemi Corp
11
// File history:
11
      0.1 Initial Version
11
// Description:
// Simple example design to demonstrate use of timing
    constraints.
11
11
// Targeted device: Family::SmartFusion2; Die::M2S050;
   Package::484 FBGA;
11
11
// Author: Joe X
11
module false_path (D0, D1, D2, RST, CLK, Q);
input
      D0;
input
      D1;
input
      D2;
input
      RST;
input
      CLK;
output Q;
       D0_reg;
reg
```



```
reg
        D0_inv_reg;
reg
       D1_reg;
reg
       D2_reg;
reg
       Q_reg;
wire XOR2 /*synthesis syn_keep=1*/;
wire AND2 /*synthesis syn_keep=1*/;
      OR2 /*synthesis syn_keep=1*/;
wire
wire
      MUX2 /*synthesis syn_keep=1*/;
wire NOT1 /*synthesis syn_keep=1*/;
wire NOT2 /*synthesis syn_keep=1*/;
assign Q = Q_reg /*synthesis syn_keep=1*/;
always @(posedge CLK or posedge RST)
begin
    if (RST)
   begin
                  <= 1'b0;
       D0_reg
        D0_inv_reg <= 1'b0;</pre>
    end
    else
    begin
                  <= D0;
        D0_reg
        D0_inv_reg <= ~D0;</pre>
    end
end
assign XOR2 = D0_reg ^ D0_inv_reg;
assign OR2 = D0_inv_reg || D1_reg;
assign AND2 = OR2 && D2_reg;
assign MUX2 = (XOR2) ? (D2_reg) : (AND2);
always @(posedge CLK)
begin
              <= D1;
   D1_reg
   D2_reg
               <= D2;
    Q_reg <= NOT2;
end
not u1 (NOT1, MUX2);
not u2 (NOT2, NOT1);
```

```
endmodule
```



# **Dialog Boxes**

# Add Path Analysis Set Dialog Box

Use this dialog box to specify a custom path analysis set.

Note: The Analysis menu is available only in Maximum or Minimum Delay Analysis view.

To open the Add Path Analysis Set dialog box (shown below) from the SmartTime Timing Analyzer, choose any path and right click to select Add Set

Add Path Analysis Set	8 23
Name :- Source pins:	Trace from :- $\ensuremath{ \ensuremath{ \bullet \ }}$ Source to sink $\ensuremath{ \ensuremath{ \ensuremath{ \circ \ }}}$ Sink to source Sink Pins:
DFN1_0:CLK DFN1_1:CLK PF_CCC_C0_0/PF_CCC_C0_0/pll_inst_0:REF_CLK_0	
Select All Filter source pins: Pin Type: Registers by pin names * Filter	Select All Filter sink pins: Pin Type: Registers by pin names * Filter
Help	OK Cancel

Figure 73 · Add Path Analysis Set Dialog Box

### Name

Enter the name of your path set.

### **Trace from**

Select whether you want to trace connected pins from **Source to sink** or from **Sink to source**. By default, the pins are traced Source to sink.



## **Source Pins**

Displays a list of available and valid source pins. You can select multiple pins. To select all source pins, click the **Select All** button beneath the Source Pins list.

## **Select All**

Selects all the pins in the Source Pins list to include in the path analysis set.

## **Filter Source Pins**

Enables you to specify thesource **Pin Type** and the **Filter**. The default pin type is Registers by pin name. You can specify any string value for the **Filter**. If you change the pin type, the **Source Pins** shows the updated list of available source pins.

## **Sink Pins**

Displays list of available and valid pins. You can select multiple pins. To select all source pins, click the **Select All** button beneath the **Sink Pins list**.

## Select All

Selects all the pins in the Sink Pins list to include in the path analysis set.

## **Filter Sink Pins**

Enables you to specify thesink **Pin Type** and the **Filter**. The default pin type is Registers (by pin). You can specify any string value for the **Filter**. If you change the pin type, the **Sink Pins** shows the updated list of available sink pins.

# Analysis Set Properties Dialog Box

Use this dialog box to view information about the user created set.

To open the **Analysis Set Properties** dialog box (shown below) from the Timing Analysis View, right-click any user-created set in the Domain Browser, and choose **Properties** from the shortcut menu.

Analysis Set I	Properties		8 23
Name :	SS		
Parent set :	<u> </u>		
From :	FN1_1:CLK PF_CCC	_CO_0/PF_CCC_	C0_0/pll_inst_0:REF_CLK_0
To :	_0/PF_CCC_C0_0/p	oll_inst_0:REF_CL	K_0 DFN1_1:CLK DFN1_1:D
Help		ОК	Cancel

Figure 74 · Analysis Set Properties Dialog Box

### Name

Specifies the name of the user-created path set.

## **Parent Set**

Specifies the name of the parent path set to which the user-created path set belongs.

# 

# **Creation filter**

## From

Specifies a list of source pins in the user-created path set.

# То

Specifies a list of sink pins in the user-created path set.

# Edit Filter Set Dialog Box

Use this dialog box to specify a filter.

To open the **Edit Filter Set** dialog box (shown below) from the SmartTime Max/Min Delay Analysis view, rightclick an existing filter set in the clock domain browser, and then choose **Edit Set** from the shortcut menu.

Edit Path Analysis Set	? ×
Name :- my_set1	Trace from :- 🔘 Source to sink 💿 Sink to source
Source pins:	Sink Pins:
Source pins: CFG0_GND_INST:Y CoreAHBLite_0/matrix4x16/masterstage_0/DEFSLAVEDATAS CoreAHBLite_0/mat	Sink Pins: SerDes_AHBBUS_0/PCIE_SERDES_IF_0/SERDESIF_INST_RNO_ SerDes_
* Filter	* Filter
Help	OK Cancel

Figure 75 · Edit Path Analysis Set Dialog Box

## Name

Specifies the name of the path you want to edit.

## **Creation filter**

Source Pins - Displays a list of source pins in the user-created path set.



Sink Pins - Displays a list of sink pins in the user-created path set.

#### See Also

Using filters

# Customize Analysis View Dialog Box

Use this dialog box to customize the timing analysis grid.

To open the **Customize Analysis View** dialog box (shown below) from the SmartTime Max/Min Delay Analysis View, click the **Customize table** button (circled in red in the figure below) in the Max/Min Delay Analysis View.

Z 🖸 🔰 🎽 🗲 0 🐵 🖂									
n Delay Analysis View									
Analysis for scenario Primary		ion •			то	-			
Register to Asynchronous		Customize table					Apply F	Filter Store Filter	Reset Filter
External Removal Asynchronous to Register a X (20) GLO		Source Pin	Sink Pin	Delay (ns)	Slack (ns)	Arrival (ns)	Required (ns)	Hold (ns)	Skew (ns
× Register to Register	1	POOR_INIT_0/COREADC_0/	RTG-FODRIC_0/U0/INST_	0.764	-0.930	3.010	3,990	1.749	-
Clock to Output Register to Asynchronous	2	FDOR_INIT_0/COREABC_0/	RTG4FDDRC_0/U0/3NST	0.681	-0.914	2.927	3.841	1.595	
External Removal Asynchronous to Register	3	FOOR_INIT_0/COREABC_0/	RTG4FODRC_0/U0/INST_	0.766	-0.892	3.012	3.904	1.658	
୬ ଏଲ୍ଡି GLI *	•	FOOR_INIT_0/COREABC_0/	RTG4FODRC_0/U0/INST_	0.626	-0.762	2.872	3.634	1.388	
80	5	FDOR_INIT_0/COREABC_0/	RTG4FDDRC_0/U0/0NST	0.717	-0.749	2.963	3.712	1.466	
64	6	POOR_INIT_0/COREABC_0/	RTG4PODRC_0/U0/INST_	0,648	-0.727	2.894	3.621	1.375	
45		1	1				· · · · ·		•
32	1.5	ime			Туре	Net			Macro
16 0 -0.98 -0.465 0 0.05 0.59		Summary data arrival time data required time slack Data_arrival_time_calcular	tion						
slack distribution(ns)	4		2010						

Figure 76 · Customize Table Button

The Customize Paths List Table Dialog Box appears.

Customize Paths List Table	? ×
Available fields: Clock Source Clock Edge Destination Clock Edge Logic Stage Count Clock Constraint (ns) Multicycle Constraint	Add       Source Pin         Sink Pin       Delay         Remove       Slack (ns)         Move Up       Arrival (ns)         Move Down       Skew (ns)
Help Restore Default	OK Cancel

Figure 77 · Customize Paths List Dialog Box

# **Available Fields**

Displays a list of all the available fields in the timing analysis grid.



## Show These Fields in This Order

Shows the list of fields you want to see in the timing analysis grid. Use **Add** or **Remove** to move selected items from **Available fields** to **Show these fields in this order** or vice versa. You can change the order in which these fields are displayed by using **Move Up** or **Move Down**.

## **Restore Defaults**

Resets all the options in the General panel to their default values.

# Manage Clock Domains Dialog Box

Use this dialog box to specify the clock pins you want to see in the Expanded Path view.

To open the Manage Clock Domain dialog box (shown below) from the SmartTime Max/Min Delay Analysis view,

ailable clock domains:			Show the clock do	mains in this order:
QS[2]	^	Add	DQS[0]	
LL_REF_CLK			DQS[1]	
dr_x32_0/CCC_0/pll_inst_0/OUT1	1.000		DQS[3]	
dr_x32_0/CCC_0/pll_inst_0/OUT2		Move Down	ddr_x32_0/DDR	PHY_BLK_0/IOD_TRAINING_0/CC
dr_x32_0/CCC_0/pll_inst_0/OUT3				
dr_x32_0/DDRPHY_BLK_0/IOD_TRAININ	IG_0/			
dr_x32_0/DDRPHY_BLK_0/IOD_TRAININ	IG_0/	Move Up		
dr_x32_0/DDRPHY_BLK_0/IOD_TRAININ	IG_0/			
dr_x32_0/DDRPHY_BLK_0/IOD_TRAININ	IG_0/			
dr_x32_0/DDRPHY_BLK_0/IOD_TRAININ	IG_0/ 🗸	Remove		
	~		<	>

Figure 78 · Manage Clock Domains Dialog Box

## **Available Clock Domains**

Displays alphanumerically sorted list of available clock pins. The first clock pin is selected by default.

## Show the Clock Domains in this Order

Shows the clock pins you want to see in the Expanded Path view. Use **Add** or **Remove** to move selected items from **Available clock domains** to **Show the clock domains in this order** or vice versa. You can change the order in which these clock pins are displayed by using **Move Up** or **Move Down**.

## **New Clock**

See Also

Managing Clock Domains



# Set False Path Constraint Dialog Box

Use this dialog box to define specific timing paths as being false.

This constraint removes timing requirements on these false paths so that they are not considered during the timing analysis. The path starting points are the input ports or register clock pins and path ending points are the register data pins or output ports. This constraint disables setup and hold checking for the specified paths.

Note: The false path information always takes precedence over multiple cycle path information and overrides maximum delay constraints.

To open the Set False Path Constraint dialog box (shown below) from the SmartTime Constraints Editor, choose **Constraints > Exceptions False Path > Add False Path Constraint**.

Trough:          Image: Control of the second seco	Set False Path Constraint	8 8
Image: Sector	om :	
Trough:		~
Through:		
<		
<		
Through : <		
To:		>
Control (1)	rougn :	A
<		
To:		
To:		
	k.	× .
<	1	
<		~
<		
< > >		
<		
		>
Comment : OK Cancel		

Figure 79 · Set False Path Constraint Dialog Box

#### From

Specifies the starting points for false path. A valid timing starting point is a clock, a primary input, an inout port, or a clock pin of a sequential cell.

## Through

Specifies a list of pins, ports, cells, or nets through which the disabled paths must pass.



## То

Specifies the ending points for false path. A valid timing ending point is a clock, a primary output, an inout port, or a data pin of a sequential cell.

## Comment

Enables you to provide comments for this constraint.

# SmartTime Options Dialog Box

Use this dialog box to specify the SmartTime options to perform timing analysis.

This interface includes the following categories:

- General
- Analysis
- Advanced

To open the SmartTime Options dialog box (shown below) from the SmartTime tool, choose **Tools > Options**.

## General

Option Categories	General	
Select a category: General	Operating Conditions	
Analysis Advanced	Perform maximum delay analysis based on WORST	▼ case
	Perform minimum delay analysis based on BEST	▼ case
	Clock Domains	lysis.
		Restore Defaults

Figure 80 · SmartTime Options- General Dialog Box for SmartFusion2, IGLOO2 and RTG4



Option Categories	General	
Select a category: General Analysis Advanced	Operating Conditions         Perform maximum delay analysis based on slow_lv_ht case         Perform minimum delay analysis based on fast_hv_lt case         Clock Domains         Include inter-clock domains in calculations for timing analysis.         Image: Enable recovery and removal checks.	
Help	Restore D OK	efaults

Figure 81 · SmartTime Options - General Dialog Box for PolarFire

## **Operating Conditions**

Allows you to perform maximum or minimum delay analysis based on the Best, Typical, or Worst case. By default, maximum delay analysis is based on WORST case and minimum delay analysis is based on BEST case.

## **Clock Domains**

- Include inter-clock domains in calculations for timing analysis: Enables you to specify if SmartTime must use inter-clock domains in calculations for timing analysis. By default, this option is unchecked.
- Enable recovery and removal checks: Enables SmartTime to check removal and recovery time on asynchronous signals. Additional sets are created in each clock domain in Analysis View to report the corresponding paths.

## **Restore Defaults**

Resets all the options in the General panel to their default values.



# Analysis

Option Categories	Analysis View	
Select a category: General Analysis Advanced	Display of Paths Limit the number of paths shown in a path set to: Filter the paths by slack value Slack range from: Slack range from: Slack network details in expanded path Limit the number of parallel paths in expanded path to:	100 ns
Help		Restore Defaults

Figure 82 · SmartTime Options - Analysis View Dialog Box

# **Display of Paths**

Limits the number of paths shown in a path set for timing analysis. The default value is 100. You must specify a number greater than 1.

# Filter the paths by slack value

Specifies the slack range between minimum slack and maximum slack. This option is unchecked by default.

## Show clock network details in expanded path

Displays the clock network details as well as the data path details in the Expanded Path views.

Limit the number of parallel paths in expanded path to: For each expanded path, specify the maximum number of parallel paths that SmartTime displays. The default number of parallel paths is 1.

## **Restore Defaults**

Resets all the options in the Analysis View panel to their default values.



## Advanced

Option Categories	Advanced	
<ul> <li>Select a category:</li> <li>General</li> <li>Analysis</li> <li>Advanced</li> </ul>	Special Situtations  Use loopback in bi-directional buffers(bibufs)  For Break paths at asynchronous pins  For Disable non-unate arcs in clock network	

Figure 83 · SmartTime Options - Advanced Dialog Box

# **Special Situations**

Enables you to specify if you need to use loopback in bi-directional buffers (bibufs) and/or break paths at asynchronous pins.

## **Scenarios**

Enables you to select the scenario to use for timing analysis and for timing-driven place-and-route.

## **Restore Defaults**

.

Resets all the options in the Analysis View panel to their default values.

# Store Filter as Analysis Set Dialog Box

Use this dialog box to specify a filter.

To open the **Store Filter as Analysis Set** dialog box (shown below) from the SmartTime Timing Analyzer, select a path and click the **Store Filter** button in the Analysis View Filter.

Create Filter Set	5	8 23
Name :	945	
Help	ОК	Cancel

Figure 84 · Store Filter as Analysis Set Dialog Box



## Name

Specifies the name of the filtered set.

#### See Also

Using filters

# **Timing Bottleneck Analysis Options Dialog Box**

Use this dialog box to customize the timing bottleneck report.

You can set report bottleneck options for the following categories:

- General pane
- Bottleneck pane
- Sets pane

To open the Timing Bottleneck Analysis Options dialog box (shown below) from the SmartTime tool, choose **Tools > Bottleneck Analysis**.

## **General Pane**

Option Categories	General		
<ul> <li>Select a category: General Bottleneck Sets</li> </ul>	Slack Maximum slack to include	D	ns
Help			Restore Defaults

Figure 85 · Timing Bottleneck Report - General Pane Dialog Box

## Slack

Lets you specify whether the reported paths will be filtered by threshold, and if so what will be the maximum slack to report. By default the paths are filtered by slack, and the slack threshold is 0.

## **Restore Defaults**

Resets all the options in the General pane to their default values.



# **Bottleneck Pane**

Option Categories	Bottleneck options	
<ul> <li>Select a category: General</li> <li>Bottleneck</li> <li>Sets</li> </ul>	Cost Type:	Path Count 🔹
JEIS	Limit the number of paths per section to:	100
	Limit the number of parallel paths per section to:	1
	Limit the number of reported instances to:	10
		Restore Defaults

Figure 86 · Timing Bottleneck Report - Bottleneck Pane Dialog Box

## **Bottleneck Options**

**Cost Type**: Select the cost type that SmartTime will include in the bottleneck report. By default, path count is selected. You may select one of the following two items from the drop-down list:

- **Path count**: This cost type associates the severity of the bottleneck to the count of violating/critical paths that traverse the instance. This is the default.
- **Path cost:** This cost type associates the severity of the bottleneck to the sum of the timing violations for the violating/critical paths that traverse the instance.

Limit the number of paths per section to: Specify the maximum number of paths per set type that SmartTime will include per section in the report. The default maximum number of paths reported is 100.

Limit the number of parallel paths per section to: For each expanded path, specify the maximum number of parallel paths that SmartTime will include in the report. Only cells that lie on these violating paths are reported. The default number of parallel paths is 1.

Limit the number of reported instances: Specify the maximum number of cells that SmartTime will include per section in the report. The default number of cells is 10.

## **Restore Defaults**

Resets all the options in the Bottleneck panel to their default values.



## **Sets Pane**

Option Categories	Bottleneck options Set Selection	
<ul> <li>Select a category: General Bottleneck</li> <li>Sets</li> </ul>	Set Selection	•
	Filter From: To:	
Help	R	estore Defaults

Figure 87 · Timing Bottleneck Report - Sets Pane Dialog Box

This pane has four mutually exclusive options:

- Entire Design
- Clock Domain
- Use existing user set
- Use Input to Output Set

Entire Design: Select this option to display the bottleneck information for the entire design.

**Clock Domain**: Select this option to display the bottleneck information for the selected clock domain. You can specify the following options:

- Clock: Allows pruning based on a given clock domains. Only cells that lie on these violating paths are reported.
- Type: This option can only be used in conjunction with -clock. The acceptable values are:

Value	Description
Register to Register	Paths between registers in the design
Asynchronous to Register	Paths from asynchronous pins to registers
Register to Asynchronous	Paths from registers to asynchronous pins
External Recovery	The set of paths from inputs to asynchronous pins
External Setup	Paths from input ports to register
Clock to Output	Paths from registers to output ports

**Use existing user set**: Displays the bottleneck information for the existing user set selected. Only paths that lie within the name set are will be considered towards the bottleneck report.



Filter: Allows you to filter the bottleneck report by the following options:

- From: Reports only cells that lie on violating paths that start at locations specified by this option.
- To: Reports only cells that lie on violating paths that end at locations specified by this option.

Filter defaults to all outputs.

### **Restore Defaults**

Resets all the options in the Paths panel to their default values.

#### See Also

**Bottleneck Analysis** 

# Timing Datasheet Report Options Dialog Box

Use this dialog box to select the output format for your timing datasheet report.

To open the **Timing Datasheet Report Options** dialog box (shown below) from the SmartTime Max/Min Delay Analysis view, choose **Tools > Reports > Datasheet**.

You can generate your report in one of two formats:

## **Plain Text**

Select this option to save your report to disk in plain ASCII text format.

#### **Comma Separated Values**

Select this option to save your report to disk in comma-separated value format (.CSV) format, which you can import into a spreadsheet.

<b>Option Categories</b> ✓ Select a category: General	Format	
	Plain Text	Comma Separated Values

Figure 88 · Report Options Dialog Box

Note: This Datasheet Report feature is not supported for PolarFire.



# **Timing Report Options Dialog Box**

Use this dialog box to customize the timing report.

You can set report options for the following categories:

- General
- Paths
- Sets
- Clock Domains

To open the Timing Report Options dialog box (shown below) from the SmartTime Max/Min Delay Analysis View, choose **Tools > Reports> Timer**.

## General

Timing Report Options		?	$\times$
Option Categories ☐ Select a category: — General — Paths — Sets — Clock Domains	Format         Indude a summary         Indude a summary of timing results in this report         Slack         Filter paths by slack threshold         Maximum slack to include         OK		
Help			

Figure 89 · Timing Report Options - General Dialog Box

## Format

Specifies whether or not the report will be exported as a Comma Separated Value (CSV) file or a plain text file. By default, the **Plain Text** option is selected.

## Summary

Specifies whether or not the summary section will be included in the report. By default, this option is selected.

## Analysis

Specifies the type of analysis to be included in the timing report. It can be either a Maximum Delay Analysis report or Minimum Delay Analysis report. By default, the Maximum Delay Analysis report is included in the timing report.

## Slack

Specifies whether the reported paths will be filtered by threshold, and if so what will be the maximum slack to report. By default, the paths are not filtered by slack.



# Paths

Option Categories			
Select a category: General Paths Sets Clock Domains	Display of paths Image: Include detailed path information in this report Limit the number of paths per section to: Limit the number of expanded paths per section to: Limit the number of parallel paths in expanded path to:	5 1 1	
Help			

Figure 90 · Timing Report Options - Paths Dialog Box

# **Display of Paths**

**Include detailed path information in this report**: Check this box to include the detailed path information in the timing report.

Limit the number of reported paths per section to: Specify the maximum number of paths that SmartTime will include per section in the report.

Limit the number of expanded paths per section to: Specify the maximum number of expanded paths that SmartTime will include per section in the report.

Limit the number of parallel paths in expanded path to: For each expanded path, specify the maximum number of parallel paths that SmartTime will include in the report. The default number of parallel paths is 1.



## Sets

Option Categories		
<ul> <li>Select a category:</li> <li>General</li> <li>Paths</li> <li>Sets</li> <li>Clock Domains</li> </ul>	Display of Sets	
	✓ Include Input to Output sets in this report	

Figure 91 · Timing Report Options - Sets Dialog Box

# **Display of Sets**

Specifies whether or not the user sets will be included in the timing report.

User sets are either filters that you have created and stored on the default paths sets (Register to Register, Inputs to Register, etc.) or Pin to Pin user sets. By default, the paths for these sets are not reported.

In addition, specify whether the Inputs to Output sets will be included in the report. By default, the Input to Output sets are reported.



# **Clock Domains**

Option Categories			
<ul> <li>Select a category:</li> <li>General</li> <li>Paths</li> <li>Sets</li> <li>Clock Domains</li> </ul>	Display of Clock Domains Include clock domains Limit reporting on clock domains to specified	domains	
	CLK CLK_RNIQO92/U0:Y.5 BLOCK_INTERFACE_I_CLK:A CLK_RNIQO92/U0.Y.5 CLK_RNIQO92/U0_RGB1:Y.1 CLK_RNIQO92/U0_RGB1:Y.4 CLK_RNIQO92/U0_RGB1:Y.6 CLK_RNIQO92:A CLK_RNIQO92:Y	Select Domains	
Help			

Figure 92 · Timing Report Options - Clock Domains Dialog Box

## **Display of Clock Domains**

Lets you specify what clock domains will be included in the report. By default, the current clock domains used by the timing engine will be reported.

## **Include Clock Domains**

Enables you to include or exclude clock domains in the report. Click the checkbox to include clock domains.

## Limit reporting on clock domains to specified domains

Lets you include one or more of the clock domain names in the box, or include additional clock domain names using **Select Domains**.

#### See Also

<u>Generating a datasheet report</u> <u>Understanding datasheet reports</u>

# **Timing Violations Report Options Dialog Box**

Use this dialog box to customize the timing violation report.

You can set report violation options for the following categories:

- General
- Paths

To open the Timing Report Options dialog box (shown below) from the SmartTime tool, choose **Tools > Reports > Timing Violations**.



# General

Option Categories	General	
⊡ Select a category: General Paths	Format	 ns
		Restore Defaults

Figure 93 · Timing Violations Report - General Dialog Box

## Format

Specifies whether or not the report will be exported as a Comma Separated Value (CSV) file or a plain text file. By default, the **Plain Text** option is selected.

## **Analysis**

Lets you specify what type of analysis will be reported in the report. By default, the report includes Maximum Delay Analysis.

## Slack

Lets you specify whether the reported paths will be filtered by threshold, and if so what will be the maximum slack to report. By default the paths are filtered by slack, and the slack threshold is 0.

## **Restore Defaults**

Resets all the options in the General panel to their default values.



# Paths

Timing Violations Report Options		? ×
Option Categories  Select a category:	Display of paths	
General Paths	$\boxed{\ensuremath{\mathcal{V}}}$ Limit the number of reported paths	
	Limit the number of paths per section to:	100
	Limit the number of expanded paths per section to:	0
	Limit the number of parallel paths in expanded path to:	1
		Restore Defaults
Help		OK Cancel

Figure 94 · Timing Violations Report - Paths Dialog Box

# **Display of paths**

Limit the number of reported paths: Check this box to limit the number of paths in the report. By default, the number of paths is limited.

Limit the number of paths per section to: Specify the maximum number of paths that SmartTime will include per section in the report. The default maximum number of paths reported is 100.

**Limit the number of expanded paths per section to**: Specify the maximum number of expanded paths that SmartTime will include per section in the report. The default number of expanded paths is 0.

Limit the number of parallel paths in expanded path to: For each expanded path, specify the maximum number of parallel paths that SmartTime will include in the report. The default number of parallel paths is 1.

## **Restore Defaults**

Resets all the options in the Paths panel to their default values.

#### See Also

<u>Generating timing violation report</u> <u>Understanding timing violation report</u>

# Data Change History - SmartTime

The data change history lists features, enhancements and bug fixes for the current software release that may impact timing data of the current design.

To generate a data change history, from the **Help** menu, choose **Data Change History**. This opens a data change history in text format.



```
Data Change History Report

File Actions Help

SmartTime Data Change History

Family: SmartFusion2/IGL002

Die: M2S090T/M2S090/M2GL090T/M2GL090/M2S090TV

Data source: Production

Libero 11.6

67526 - Update CCC arc delays

66997 - Update clock net delays

6727 - Update MSS/FDDR setup time in AXI mode

54350 - Update IO enable HZ/LZ arc delay

Libero 11.5 SP2A

59225 - Timing data (IND/COM) updated from advanced to production

59228 - Support 1.0V timing (for M2S090TV, -1, IND)
```

Figure 95 · SmartTime Data Change History Report



# **Tcl Commands**

For details about the Tcl commands supported by SmartTime, refer to the SmartFusion2, IGLOO2, RTG4 Tcl Commands Reference Guide or the PolarFire FPGA Tcl Commands Reference Guide.



# Glossary

### arrival time

Actual time in nanoseconds at which the data arrives at a sink pin when considering the propagation delays across the path.

#### asynchronous

Two signals that are not related to each other. Signals not related to the clock are usually asynchronous.

### capture edge

The clock edge that triggers the capture of data at the end point of a path.

#### clock

A periodic signal that captures data into sequential elements.

#### critical path

A path with the maximum delay between a starting point and an end point. In the presence of a clock constraint, the worst critical path between registers in this clock domain is the path with the worst slack.

## dynamic timing analysis

The standard method for verifying design functionality and performance. Both pre-layout and post-layout timing analysis can be performed via the SDF interface.

#### exception

See timing exception.

#### explicit clock

Clock sources that can be traced back unambiguously from the clock pin of the registers they deserve, including the output of a DLL or PLL.

#### filter

A set of limitations applied to object names in timing analysis to generate target specific sets.

#### launch edge

The clock edge that triggers the release of data from a starting point to be captured by another clock edge at an end point.

### minimum period

Timing characteristic of a path between two registers. It indicates how fast the clock will run when this path is the most critical one. The minimum period value takes into consideration both the skew and the setup on the receiving register.

#### parallel paths

Paths that run in parallel between a given source and sink pair.



## path

A sequence of elements in the design that identifies a logical flow starting at a source pin and ending at a sink pin.

### path details

An expansion of the path that shows all the nets and cells between the source pin and the sink pin.

#### path set

A collection of paths.

## paths list

Same as path set.

### post-layout

The state of the design after you run Layout. In post-layout, the placement and routing information are available for the whole design.

### potential clock

Pins or ports connected to the clock pins of sequential elements that the Static Timing Analysis (STA) tool cannot determine whether they are is enabled sources or clock sources. This type of clock is generally associated with the use of gated clocks.

### pre-layout

The state of the design before you run Layout. In pre-layout, the placement and routing information are not available.

#### recovery time

The amount of time before the active clock edge when the de-activation of asynchronous signals is not allowed.

### removal time

The amount of time after the active clock edge when the de-activation of asynchronous signals is not allowed.

### required time

The time at which the data must be at a sink pin to avoid being in violation.

#### requirement

See timing requirement.

### scenario (timing constraints scenario)

Set of timing constraints defined by the user.

#### setup time

The time in nanoseconds relative to a clock edge during which the data at the input to a sequential element must remain stable.

#### sink pin

The pin located at the end of the timing path. This pin is usually the one where arrival time and required time are evaluated for path violation.



#### skew

The difference between the clock insertion delay to the clock pin of a sink register and the insertion delay to the clock pin of a source register.

#### slack

The difference between the arrival time and the required time at a specific pin, generally at the data pin of a sequential component.

#### slew rate

The time needed for a signal to transition from one logic level to another.

#### source pin

The pin located at the beginning of a timing path.

#### STA

See static timing analysis.

## standard delay format (SDF)

Standard Delay Format, a standard file format used to store design data suited for back-annotation.

#### static timing analysis

An efficient technique to identify timing violations in a design and to ensure that all timing requirements are met. It is well suited for traditional synchronous designs. The main advantages are that it does not require input vectors, and it exclusively covers all possible paths in the design in a relatively short run-time.

### synopsys design constraint (SDC)

A standard file format for timing constraints. Synopsys Design Constraints (SDC) is a Tcl-based format used by Synopsys tools to specify the design intent, including the timing and area constraints for a design. Microsemi SoC tools use a subset of the SDC format to capture supported timing constraints. You can import or export an SDC file from the Designer software. Any timing constraint that you can enter using Designer tools, can also be specified in an SDC file.

### timing constraint

A requirement or limitation on the design to be satisfied during the design implementation.

#### timing exception

An exception to a general requirement usually applied on a subset of the objects on which the requirement is applied.

### timing requirement

A constraint on the design usually determined by the specifications at the system level.

## virtual clock

A virtual clock is a clock with no source associated to it. It is used to describe clocks outside the FPGA that have an impact on the timing analysis inside the FPGA. For example, if the I/Os are synchronous to an external clock.

#### WLM

Wire Load Model. A timing model used in pre-layout to estimate a net delay based on the fan-out.