UG0811
User Guide
SmartTime Static Timing Analyzer
Libero SoC v12.1 and later

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About SmartTime

SmartTime is the Libero SoC gate-level static timing analysis tool. With SmartTime, you can perform complete timing analysis of your design to ensure that you meet all timing constraints and that your design operates at the desired speed with the right amount of margin across all operating conditions.

Note: Creation and Editing of timing constraints are done in a separate Timing Constraints Editor. See the Timing Constraints Editor User Guide for help with creating and editing timing constraints.

Static Timing Analysis (STA)

Static timing analysis (STA) offers an efficient technique for identifying timing violations in your design and ensuring that it meets all your timing requirements. You can communicate timing requirements and timing exceptions to the system by setting timing constraints. A static timing analysis tool will then check and report setup and hold violations as well as violations on specific path requirements.

STA is particularly well suited for traditional synchronous designs. The main advantage of STA is that unlike dynamic simulation, it does not require input vectors. It covers all possible paths in the design and does all the above with relatively low run-time requirements.

The major disadvantage of STA is that the STA tools do not automatically detect false paths in their algorithms as it reports all possible paths, including false paths, in the design. False paths are timing paths in the design that do not propagate a signal. To get a true and useful timing analysis, you need to identify those false paths, if any, as false path constraints to the STA tool and exclude them from timing considerations.

The SmartTime user interface provides efficient, user-friendly ways to define these critical false paths.

Timing Constraints

SmartTime supports a range of timing constraints to provide useful analysis and efficient timing-driven layout.

Timing Analysis

SmartTime provides a selection of analysis types that enable you to:

- Find the minimum clock period/highest frequency that does not result in timing violations
- Identify paths with timing violations
- Analyze delays of paths that have no timing constraints
- Perform inter-clock domain timing verification
- Perform maximum and minimum delay analysis for setup and hold checks

To improve the accuracy of the results, SmartTime evaluates clock skew during timing analysis by individually computing clock insertion delays for each register.

SmartTime checks the timing requirements for violations while evaluating timing exceptions (such as multicycle or false paths).

SmartTime and Place and Route

Because Libero SoC Place and Route uses SmartTime STA during timing-driven place-and-route in the background; your analysis and place and route constraints are always consistent.

SmartTime and Timing Reports

From **SmartTime > Tools > Reports**, the following report files can be generated:

- Timing Report (for both Max and Min Delay Analysis)
- Timing Violations Report (for both Max and Min Delay Analysis)
- Bottleneck Report
- Constraints Coverage Report

- Combinational Loop Report

SmartTime and Cross-Probing into Chip Planner

From SmartTime, you can select a design object and cross-probe the same design object in Chip Planner. Design objects that can be cross-probed from SmartTime to Chip Planner include:

- Ports
- Macros
- Timing Paths

SmartTime and Cross-Probing into Constraints Editor

From SmartTime, you can cross-probe into the Constraints Editor. Select a Timing Path in SmartTime's Analysis View and add a Timing Exception Constraint (False Path, Multicycle Path, Max Delay, Min Delay) . The Constraint Editor reflects the newly added timing exception constraint.

The Constraints Editor must be running for Cross-Probing to work.

See Also

Starting and Closing SmartTime

Components of SmartTime Timing Analyzer

Changing SmartTime Preferences

Design Flows with SmartTime

You can access SmartTime in Libero SoC either implicitly or explicitly during the following phases of design implementation:

- During Place and Route – When you select timing-driven place-and-route, SmartTime runs in the background to provide accurate timing information.
- After Place and Route – Run SmartTime to perform post-layout timing analysis and adjust timing constraints. In the Libero SoC Design Flow window, expand **Implement Design > Verify Post-Layout Implementation**. You can:
    - Double-click **Verify Timing** to generate Timing Reports.
    - Right-click **Open SmartTime** > **Open Interactively** to run SmartTime.
- During Back-Annotation – SmartTime runs in the background to generate the SDF file for timing simulation.

You can also run SmartTime whenever you need to generate timing reports, regardless of which design implementation phase you are in.

See Libero SoC User Guide for more information about Place and Route and Back-Annotation.

Starting and Closing SmartTime

You must have completed Place and Route for your design before using SmartTime interactively. If your design has not yet been placed-and-routed, Libero SoC will complete that phase prior to starting SmartTime.

To open SmartTime interactively, in **Implement Design > Verify Post Layout Implementation** right-click **Open SmartTime** > **Open Interactively**.

SmartTime reads your design and displays post- or pre-layout timing information.

To close SmartTime, from the **File** menu, choose **Exit**.

SmartTime Components

- The Maximum Delay Analysis View  and the Minimum Delay Analysis View  enable you to analyze your design

With SmartTime, you can:

- Browse through your design's various clock domains to examine the timing paths and identify those that violate your timing requirements
- Create customizable timing reports
- Navigate directly to the paths responsible for violating your timing requirements

Setting SmartTime Options

You can modify SmartTime options for timing analysis by using the SmartTime Options dialog box.

To set SmartTime options:

From the SmartTime Maximum/Minimum Delay Analysis View window, choose **Tools> Options**.

The SmartTime Options dialog box has three categories: **General**, **Analysis**, and **Advanced**.

General

1. In the **General** category, select the settings for the operating conditions. SmartTime performs maximum or minimum delay analysis based on the Best, Typical, or Worst case.
2. Check or uncheck whether you want SmartTime to use inter-clock domains in calculations for timing analysis.
3. Click **Restore Defaults** only if you want the settings in the General pane to revert to their default settings.

Analysis

1. Click **Analysis** to display the options you can modify in the Analysis view.
2. Enter a number greater than 1 to specify the maximum number of paths to include in a path set during timing analysis.
3. Check or uncheck whether to filter the paths by slack value. If you check this box, you must then specify the slack range between minimum slack and maximum slack.
4. Check or uncheck whether to include clock network details.
5. Enter a number greater than 1 to specify the number of parallel paths in the expanded path.
6. Click **Restore Defaults** only if you want the settings in the Analysis View pane to revert to their default settings.

Advanced

1. Click **Advanced** to display advanced options.
2. Check or uncheck whether to use loopback in bidirectional buffers (bibufs) and/or break paths at asynchronous pins. Check or uncheck whether to disable non-unate arcs in the clock path.
3. Click **Restore Defaults** only if you want the settings in the Advanced pane to revert to their default settings.
4. Click **OK.**

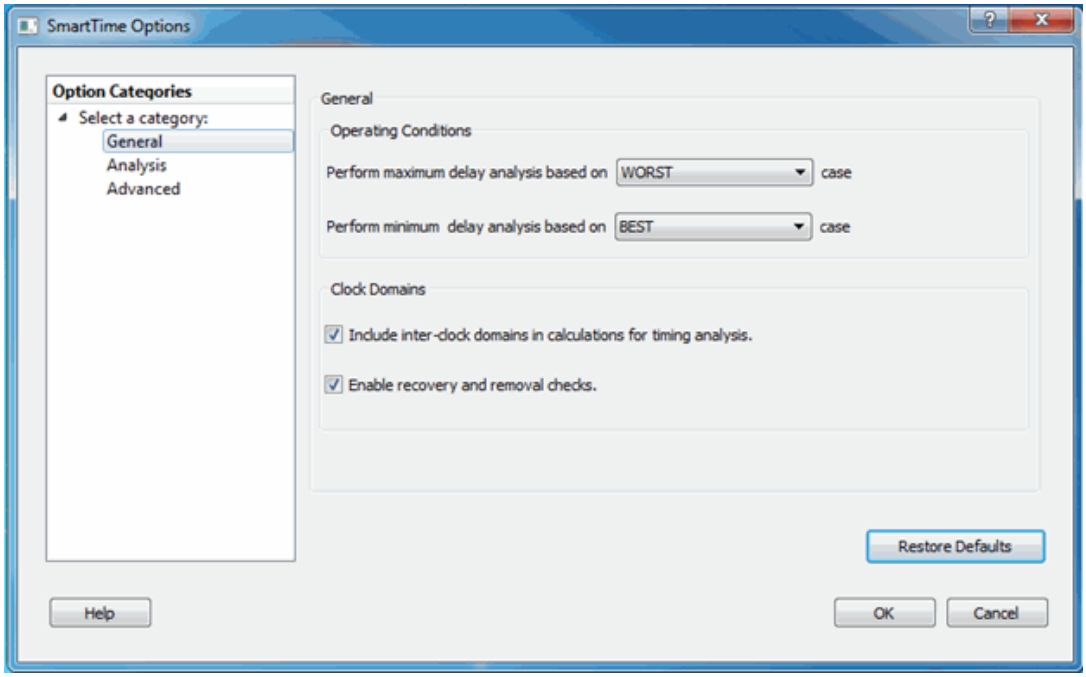


Figure 1 · SmartTime Options Dialog Box – General Options for SmartFusion2, IGLOO2 and RTG4

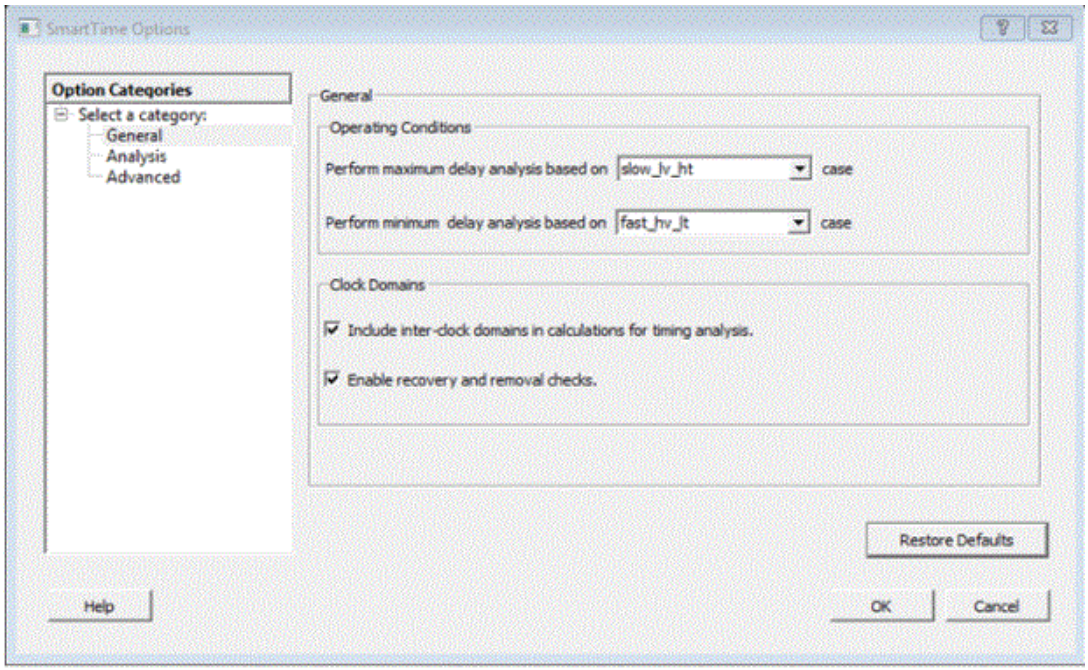


Figure 2 · SmartTime Options Dialog Box – General Options for PolarFire

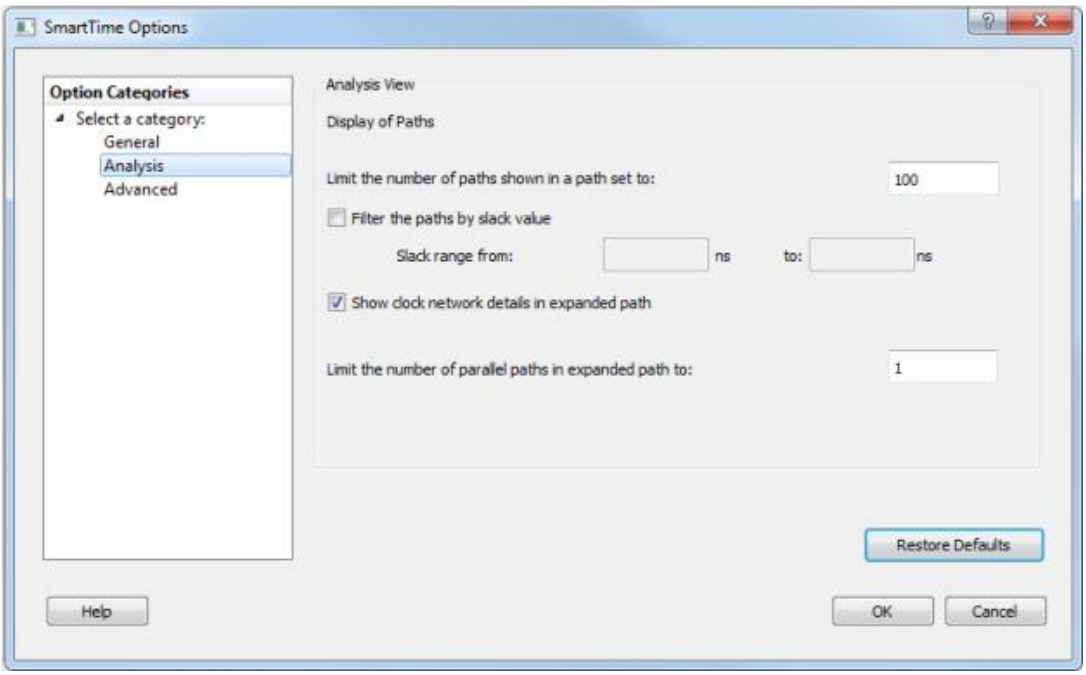


Figure 3 · SmartTime Options Dialog Box – Analysis Options

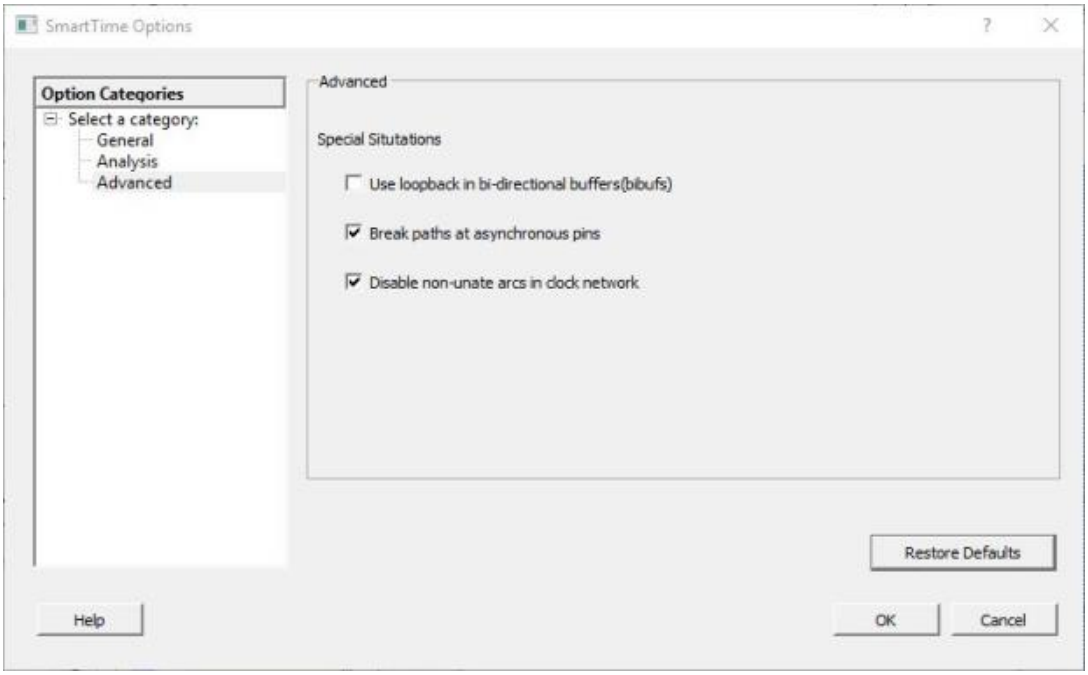


Figure 4 · SmartTime Options Dialog Box – Advanced Options

See Also

SmartTime Options Dialog Box

SmartTime Toolbar

The SmartTime toolbar contains commands for constraining or analyzing designs. Tool tips are available for each button.

Table 1 · SmartTime Toolbar

Icon	Description
	Saves the changes
	Undoes previous changes
	Redoes previous changes
	Opens the maximum delay analysis view
	Opens the minimum delay analysis view
	Opens the manage clock domains manager
	Opens the path set manager
	Recalculates all

SmartTime Timing Analyzer

SmartTime Timing Analyzer

The SmartTime Timing Analyzer is an interactive Static Timing Analysis tool. Click Open SmartTime in the Design Flow Window to invoke the SmartTime Timing Analyzer (**Design Flow Window** > **Open SmartTime > Open Interactively**).

Components of the SmartTime Timing Analyzer

Use the SmartTime Timing Analyzer to visualize and identify timing issues in your design for the selected scenario. In this view, you can evaluate how far you are from meeting your timing requirements, create custom sets to track, set timing exceptions to obtain timing closure, and cross-probe paths with other tools.

The timing analysis view includes:

- Domain Browser: Enables you to perform your timing analysis on a per domain basis.
- Path List: Displays paths in a specific set in a given domain sorted by slack.
- Path Details: Displays detailed timing analysis of a selected path in the paths list.
- Analysis View Filter: Enables you to filter the content of the paths list.
- Path Slack Histogram: When a set is selected in the Domain Browser, the Path Slack Histogram displays a distribution of the path slacks for that set. Selecting one or multiple bars in the Path Slack Histogram filters the paths displayed in the Path List.
  You can copy, change the resolution and the number of bars of the chart from the right-click menu.

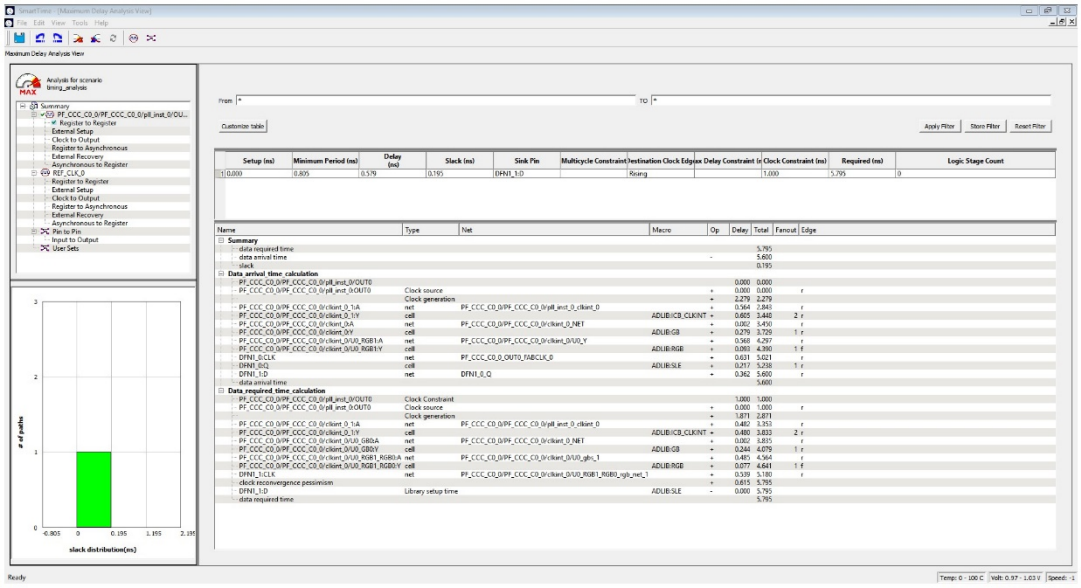


Figure 5 · SmartTime Timing Analyzer Components

Analyzing Your Design

The timing engine uses the following priorities when analyzing paths and calculating slack:

1. False path
2. Max/Min delay
3. Multi-cycle path

4. Clock

If multiple constraints of the same priority apply to a path, the timing engine uses the tightest constraint.

You can perform two types of timing analysis: Maximum Delay Analysis and Minimum Delay Analysis.

To perform the basic timing analysis:

1. Open the Timing Analysis View using one of the following methods:
    - From the SmartTime **Tools** menu, choose **Timing Maximum Delay Analysis** or **Minimum Delay Analysis.**
    - Click the  icon for Maximum Delay Analysis or the  icon for Minimum Delay Analysis from the SmartTime window.

Note: When you open the Timing Analyzer from Designer, the Maximum Delay Analysis window is displayed by default.

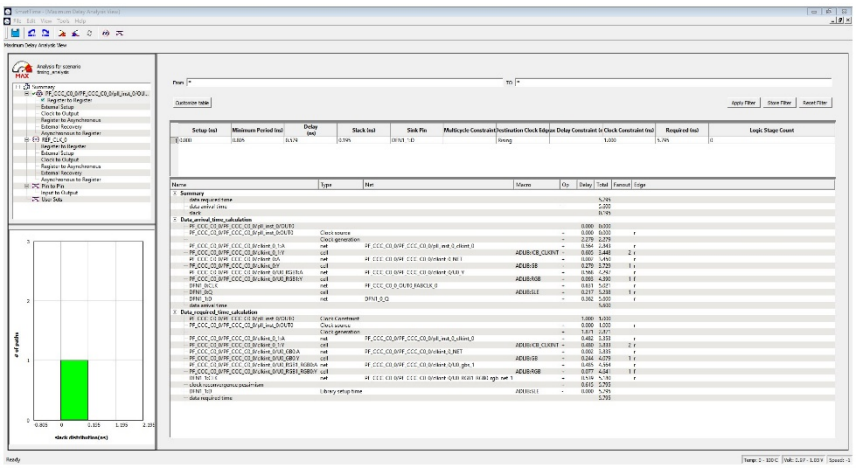


Figure 6 · Maximum Delay Analysis View

2. In the Domain Browser, select the clock domain. Clock domains with a ✔ indicate that the timing requirements in these domains were met. Clock domains with an x indicate that there are violations within these domains. The Paths List displays the timing paths sorted by slack. The path with the lowest slack (biggest violation) is at the top of the list.
3. Select the path to view. The Path Details below the Paths List displays detailed information on how the slack was computed by detailing the arrival time and required time calculation. When a path is violated, the slack is negative and is displayed in red color.
4. Double-click the path to display a separate view that includes the path details and schematic.

Note: In cases where the minimum pulse width of one element on the critical path limits the maximum frequency for the clock, SmartTime displays an icon for the clock name in the Summary List. Click on the icon to display the name of the pin that limits the clock frequency.

5. Repeat the above steps as required.

Managing Clock Domains

In SmartTime, timing paths are organized by clock domains. By default, SmartTime displays domains with explicit clocks. Each clock domain includes at least three path sets:

- Register to Register
- External Setup (in the Maximum Analysis View) or External Hold (in the Minimum Analysis View)
- Clock to Out

You must select a path set to display a list of paths in that specific set.

To manage the clock domains:

1. Right-click anywhere in the Domain Browser, and choose **Manage Clock Domains**. The Manage Clock Domains dialog box appears (as shown below).

Tip: You can click the  icon in the SmartTime window bar to display the **Manage Clock Domains** dialog box.

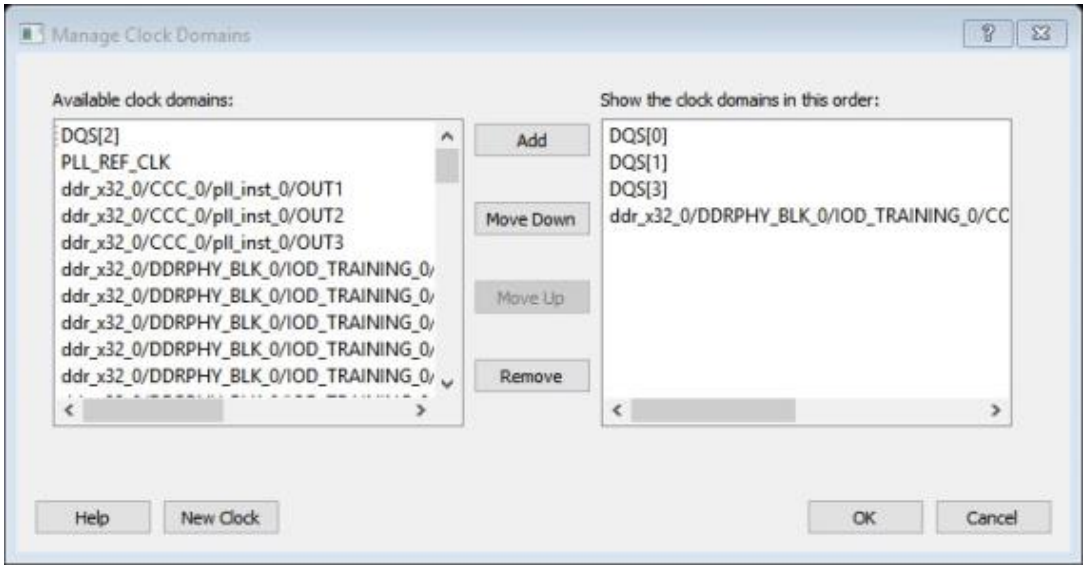


Figure 7 · Manage Clock Domains Dialog Box

2. To add a new domain, select a clock domain from the **Available clock domains** list, and click **Add**. To add a non-explicit clock domain, click **New Clock**.
   The Choose the Clock Source Pin dialog box opens, and you can select the clock source pin. You can choose to filter the available pins and search.

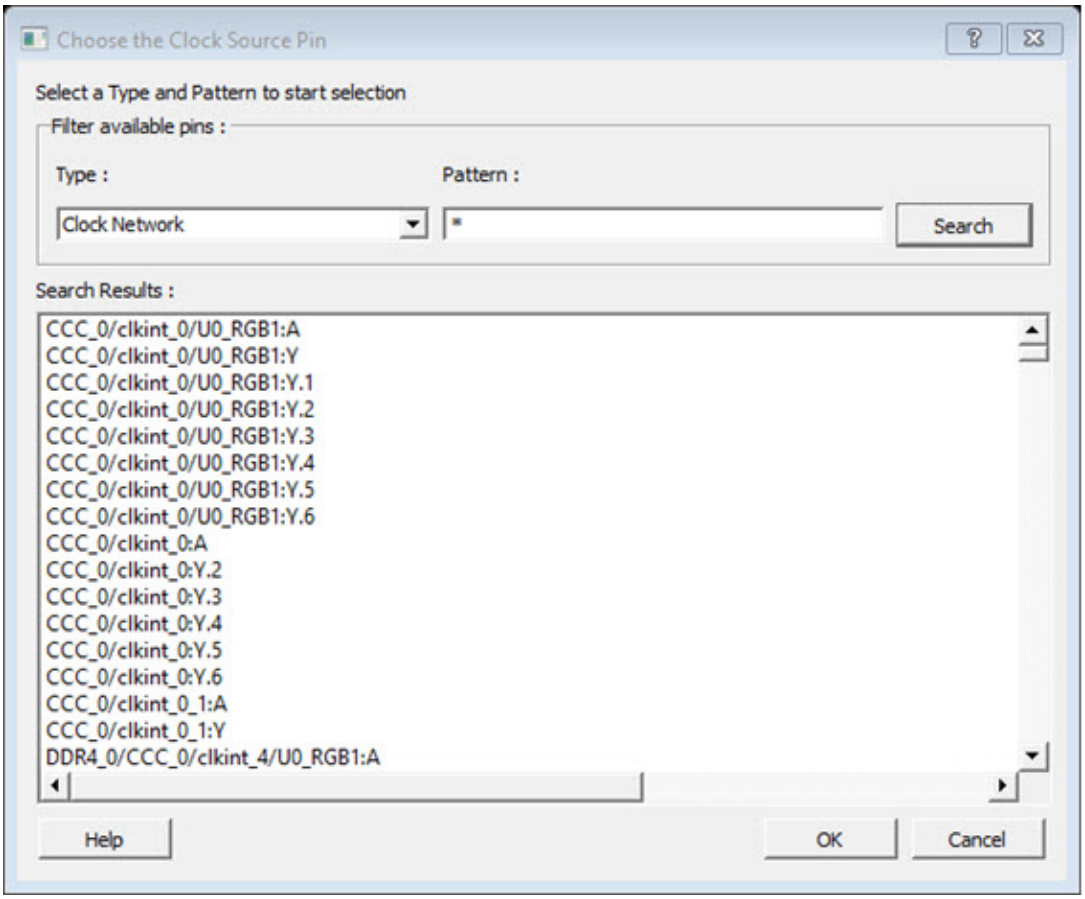


Figure 8 · Choose Clock Source Pin Dialog Box

4. To remove a displayed domain, select a clock domain from the **Show the clock domains in this order** list, and click **Remove**.
5. To change the display order in the Domain Browser, select a clock domain from the **Show the clock domains in this order** list, and then use the **Move Up** or **Move Down** to change the order in the list.
6. Click **OK**. SmartTime updates the Domain Browser based on your specifications. If you have added a new clock domain, then it will include at least the three path sets as mentioned above.

See Also

Manage Clock Domains Dialog Box

Managing Path Sets

You can create and manage custom path sets for timing analysis and tracking purposes. Path sets are displayed under the **Custom Path Sets** at the bottom of the Domain Browser.

To add a new path set:

1. Right-click anywhere in the Domain Browser, and choose **Add Set**. The Add Path Analysis Set Dialog Box appears (as shown below).

   Tip: You can click the  icon in the SmartTime window bar to display the **Add Path Analysis Set** dialog box.

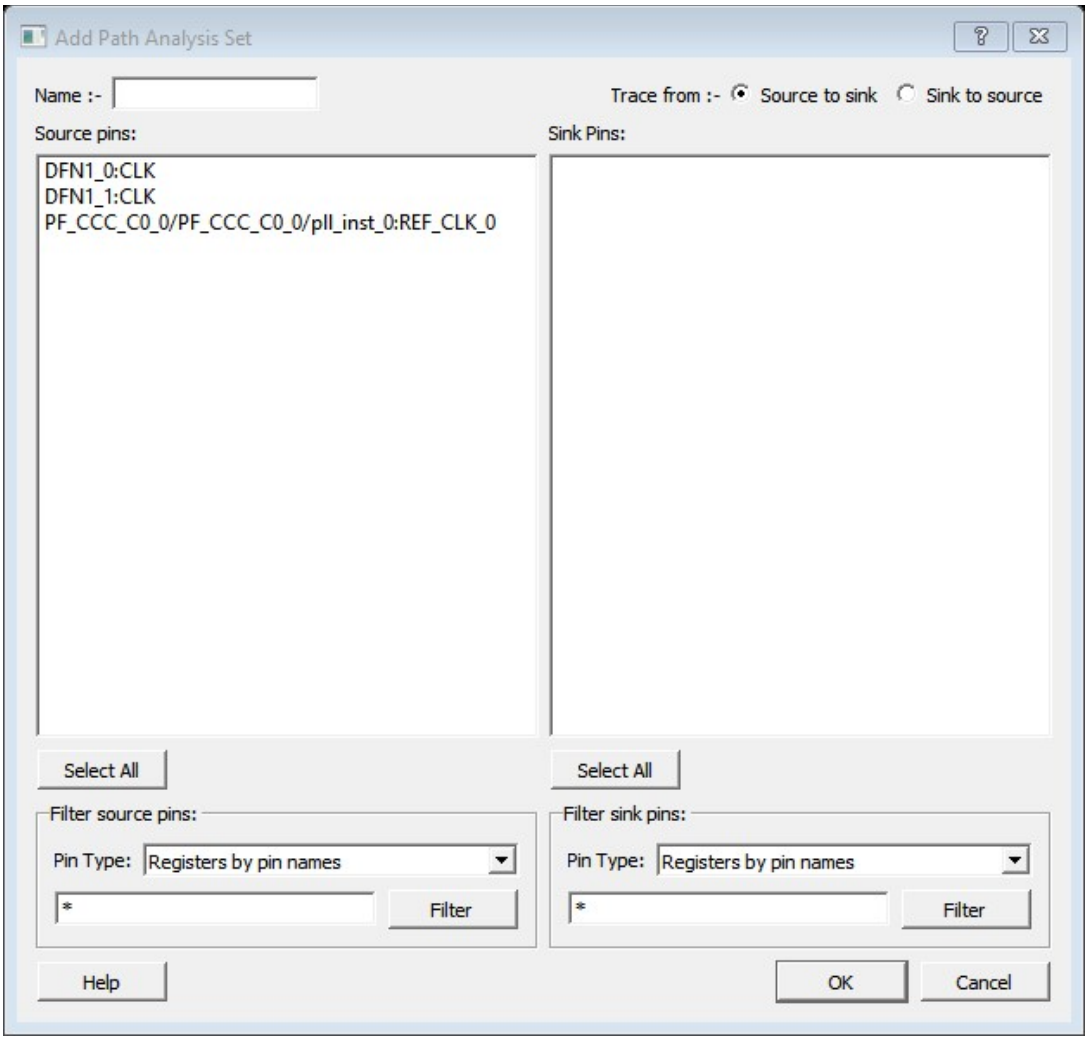


Figure 9 · Add Path Analysis Set Dialog Box

2. Enter a name for the path set.
3. Select the source and sink pins. You can use the filters to control the type of pins displayed.
4. Click **OK**. The new path set appears under **User Sets** in the Domain Browser (as shown below).

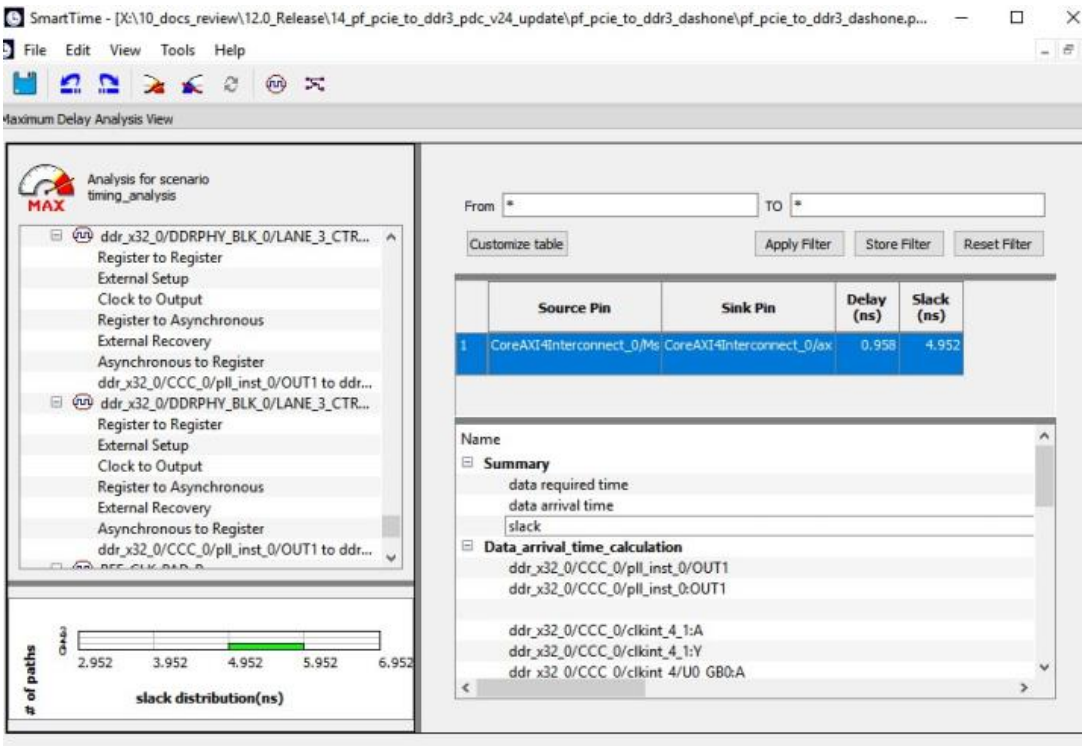


Figure 10 · Updated Domain Browser with User Sets

To remove an existing path set:

1. Select the path set from the **User Sets** in the Domain Browser.
2. Right-click the set to delete, and then choose **Delete Set** from the right-click menu.

To rename an existing path set:

1. Select the path set from **User Set** in the Domain Browser.
2. Right-click the set to rename, and then choose **Rename Set** from the right-click menu.
3. Edit the name directly in the Domain Browser.

See Also

Add Path Analysis Set Dialog Box

Using Filters

Displaying Path List Timing Information

The Path List in the Timing Analysis View displays the timing information required to verify the timing requirements and identify violating paths. The Path List is organized in a grid where each row represents a timing path with the corresponding timing information displayed in columns. Timing information is customizable; you can add or remove columns for each type of set.

By default, each type of set displays a subset of columns as follows:

- Register to Register: Source Pin, Sink Pin, Delay, Slack, Arrival, Required, Setup, Minimum Period, and Skew.
- External Setup: Source Pin, Sink Pin, Delay, Slack, Arrival, Required, Setup, and External Setup.
- Clock to Out: Source Pin, Sink Pin, Delay, Slack, Arrival, Required, and Clock to Out.
- Input to Output: Source Pin, Sink Pin, Delay, and Slack.
- Custom Path Sets: Source Pin, Sink Pin, Delay, and Slack.

You can add the following columns for each type of set:

- Register to Register: Clock, Source Clock Edge, Destination Clock Edge, Logic Stage Count, Max Fanout, Clock Constraint, Maximum Delay Constraint, and Multicycle Constraint.
- External Setup: Clock, Destination Clock Edge, Logic Stage Count, Max Fanout, Clock Constraint, Input Delay Constraint, Required External Setup, Maximum Delay Constraint, and Multicycle Constraint.
- Clock to Out: Clock, Source Clock Edge, Logic Stage Count, Max Fanout, Clock Constraint, Output Delay Constraint, Required Maximum Clock to Out, Maximum Delay Constraint, and Multicycle Constraint.
- Input to Output: Arrival, Required, Setup, Hold, Logic Stage Count, and Max Fanout.
- Custom Path Sets.

To customize the set of timing information in the Path List:

1. Select the set to customize.
2. Choose **Customize table** on the top left corner of path list to open the Customize Paths List Table dialog box.
3. To add one or more columns, select the fields to add from the **Available fields** list, and click **Add**.

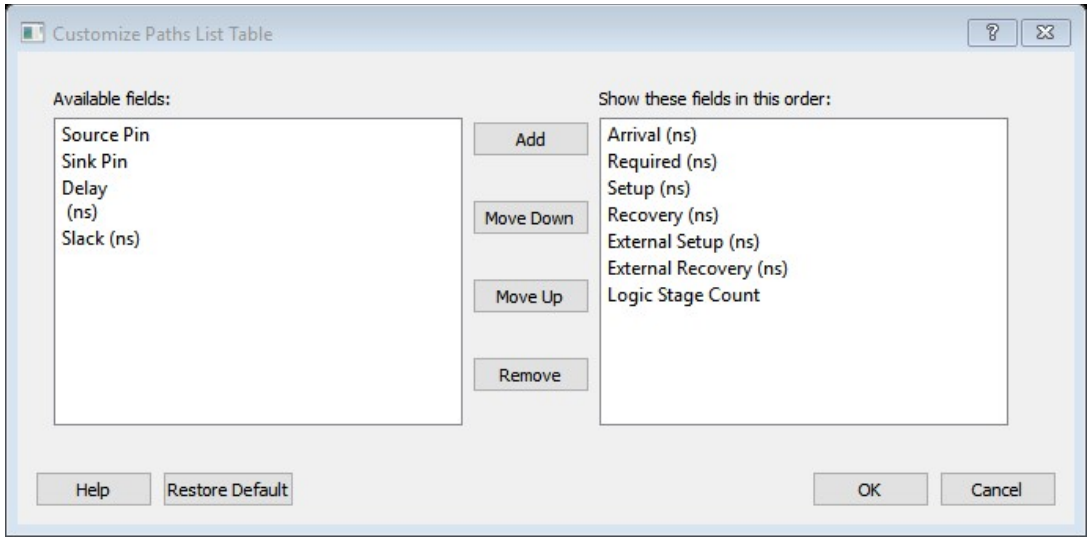


Figure 11 · Customize Paths List Table Dialog Box

4. To remove one or more columns, select the fields to remove from the **Show these fields in this order** list, and click **Remove**.
5. To change the order in which the fields appear, select fields in the **Show these fields in this order** list and click **Move Up** or **Move Down**.
6. Click **OK** to add or remove the selected columns. SmartTime updates the Timing Analysis View.

See Also

Customize Analysis View

Displaying Expanded Path Timing Information

SmartTime displays the list of paths and the path details for all parallel paths.

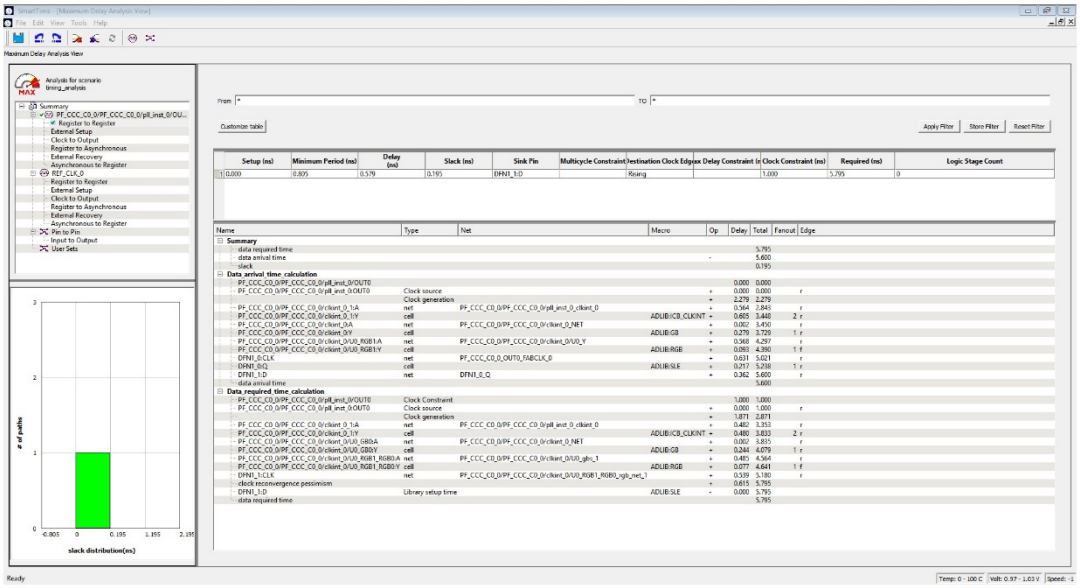


Figure 12 · Path List View

The Path List displays all parallel paths in your design. The Path Details grid displays the path details for all parallel paths.

To display the Expanded Path View:

From the Path List: double-click the path, or right-click a path and select **expand selected paths**.

From the Expanded Path View: double-click the path, or right-click the path and select **expand path**.

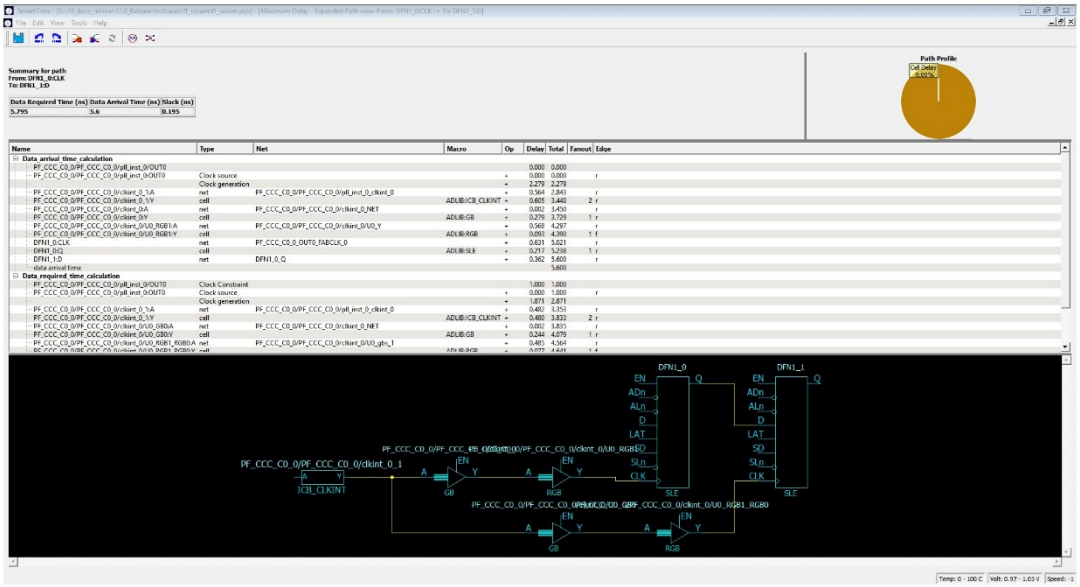


Figure 13 · Expanded Path View

The Expanded Path Summary provides a summary of all parallel paths for the selected path. The Path Profile chart displays the percentage of time taken by cells and nets for the selected path. If no parallel path is selected in this view, the Path Profile shows the percentage for all paths. By default, SmartTime only shows one path for each Expanded Path. You can change this default in the SmartTime Options dialog box.

The Expanded Path View also includes a schematic of the path and a path profile chart for the paths selected in the Expanded Path Summary.

Using Filters

You can use filters in SmartTime to limit the Path List content (that is, create a filtered list on the source and sink pin names). The filtering options appear on the top of the Timing Analysis View. You can save these filters one level below the set under which it has been created.

To use the filter:

1. Select a set in the Domain Browser to display a given number of paths, depending on your SmartTime Options settings (100 paths by default).
2. Enter the filter criteria in both the **From** and **To** fields and click **Apply Filter**. This limits the display to the paths that match your filter criteria.

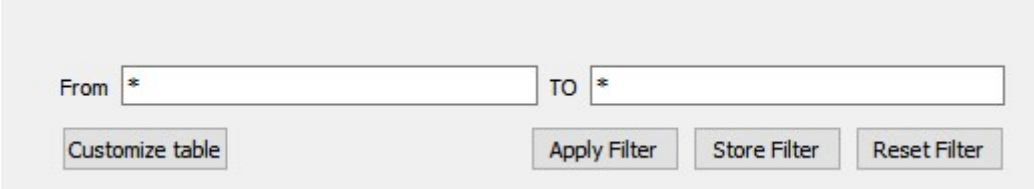


Figure 14 · Maximum Delay Analysis View

3. Click **Store Filter** to save your filter criteria with a special name. The **Create Filter Set** dialog box appears (as shown below).

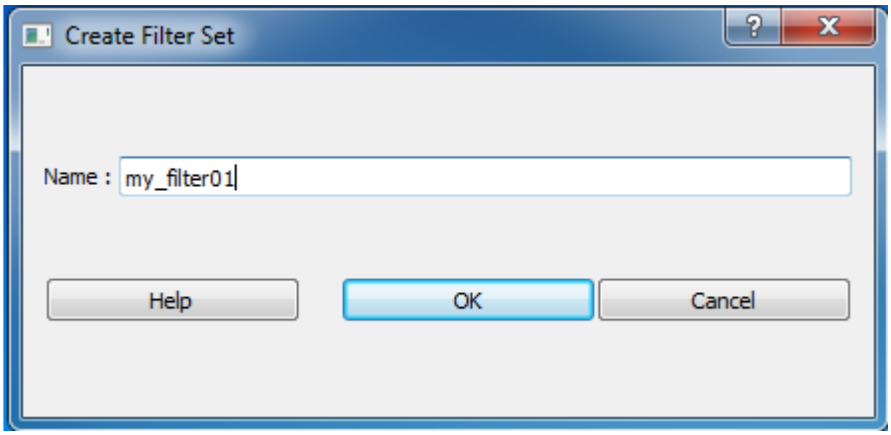


Figure 15 · Create Filter Set Dialog Box

4. Enter a name for the filter, such as myfilter01, and click **OK**. Your new filter name appears below the set under which it was created.

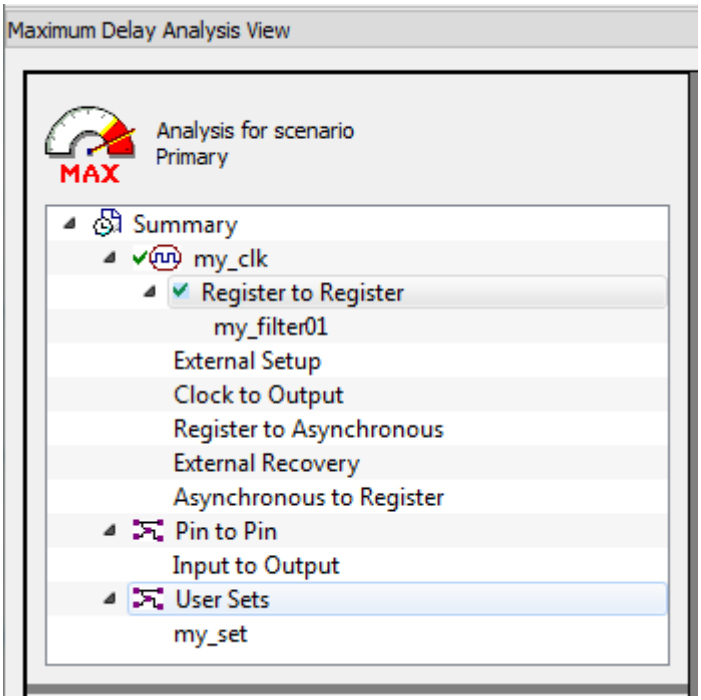


Figure 16 · my_filter01

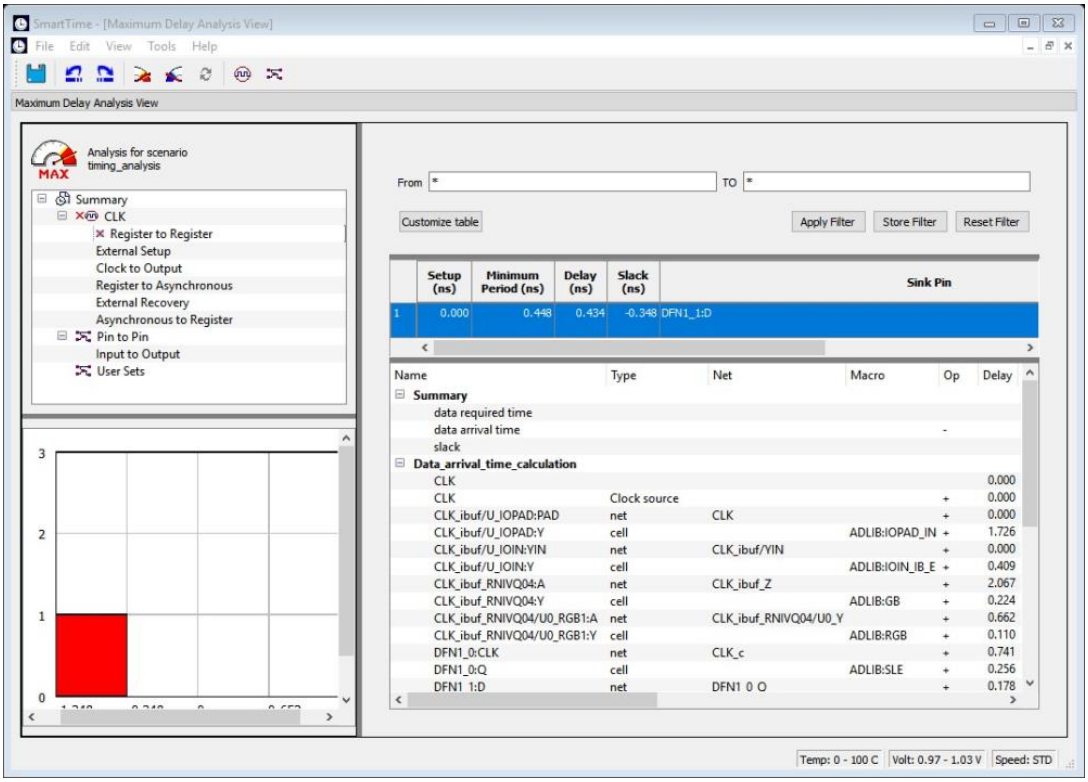


Figure 17 · Updated Maximum Delay Analysis View

Repeat the above steps and cascade as many sets as you need using the filtering mechanism.

To remove a set created with filters:

1. Select the set that uses filters.
2. Right-click the set, and choose **Delete Set** from the shortcut menu.

To rename a set created with filters:

1. Select the set that uses filters.
2. Right-click the set, and choose **Rename Set** from the shortcut menu.
3. Edit the name directly in the Domain Browser.

To edit a specific filter in the set:

1. Select the filter to edit.
2. Right-click the filter, and choose **Edit Set** from the shortcut menu.

See Also

SmartTime Options

Store Filter as Analysis Set

Edit Set dialog box

Advanced Timing Analysis

Understanding Inter-Clock Domain Analysis

When functional paths exist across two clock domains (the register launching the data and the one capturing it are clocked by two different clock sources), you must provide accurate specification of both clocks to allow a valid inter-clock domain timing check. This is important especially when the clocks are specified with different waveforms and frequencies.

When you specify multiple clocks in your design, the first step is to consider whether the inter-clock domain paths are false or functional. If these paths are functional, then you must perform setup and hold checks between the clock domains in SmartTime. Unless specified otherwise, SmartTime considers the inter-clock domain as false, and therefore does not perform setup or hold checks between the clock domains.

If you have several clock domains that are subset of a single clock (such as if you want to measure clock tree delay from an input clock to a generated clock), you must configure Generated Clock Constraints for each of the clock domains in order for SmartTime to do execute the calculation and show timing for each of the inter-clock-domain paths.

Once you include the inter-clock domains for timing analysis, SmartTime analyzes for each inter-clock domain the relationship between all the active clock edges over a common period equal to the least common multiple of the two clock periods. The new common period represents a full repeating cycle (or pattern) of the two clock waveforms (as shown below).

For setup check, SmartTime considers the tightest relation launch-capture to ensure that the data arrives before the capture edge. The hold check verifies that a setup relationship is not overwritten by a following data launch.

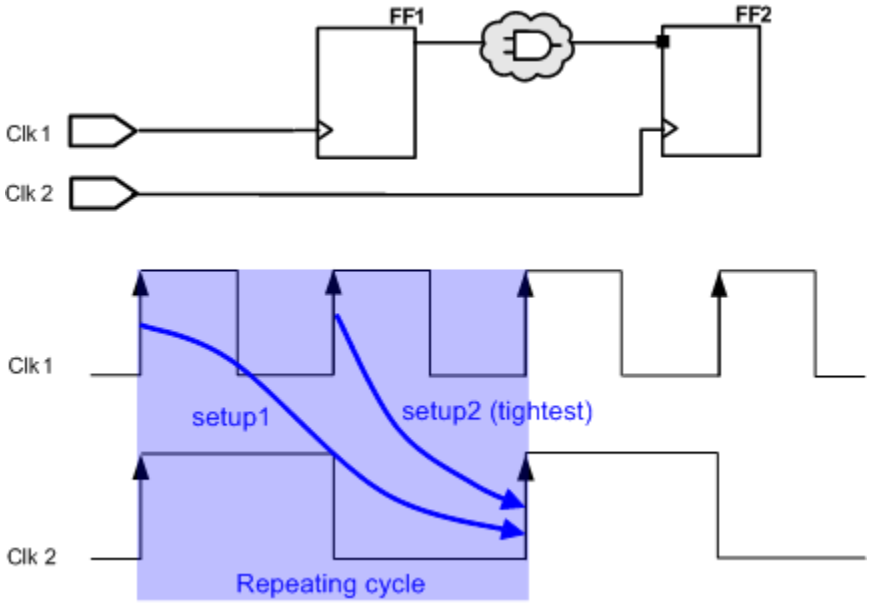


Figure 18 · Example Showing Inter-Clock Domains

See Also

Activating inter-clock domain analysis

Deactivating a specific inter-clock domain

Displaying inter-clock domain paths

Activating Inter-Clock Domain Analysis

To activate the inter-clock domain checking:

1. In SmartTime, from the **Tools** menu choose **Options**. The SmartTime Options Dialog Box dialog box appears (as shown below).
2. In the general category, check the **Include inter-clock domains in calculations for timing analysis**.

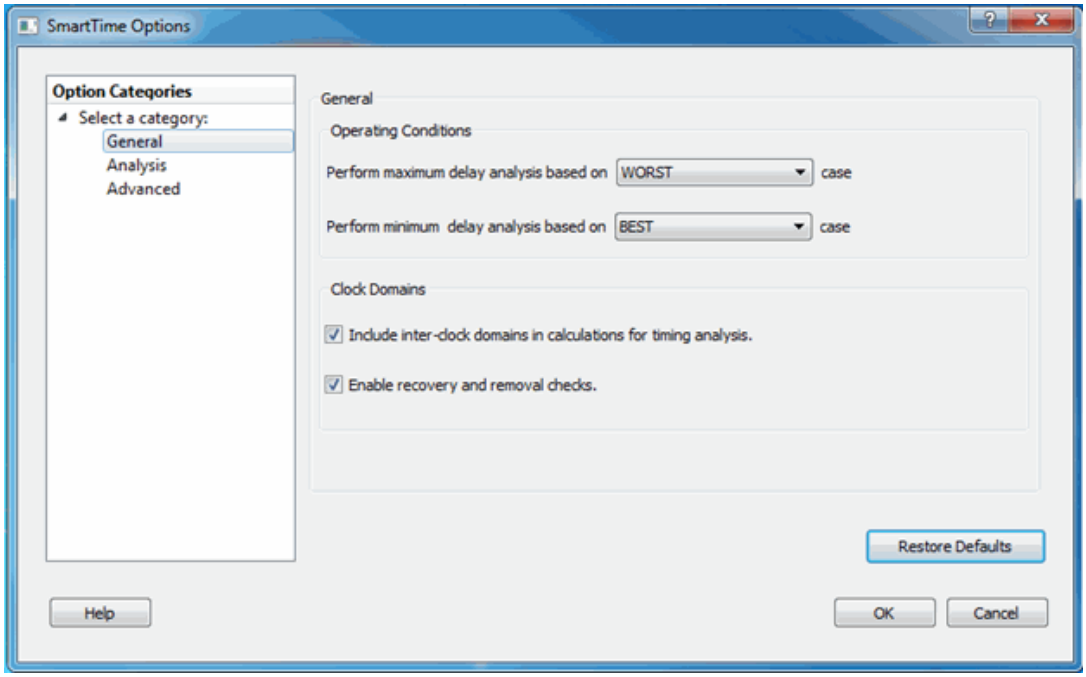


Figure 19 · SmartTime Options Dialog Box for SmartFusion2, RTG4 and IGLOO2

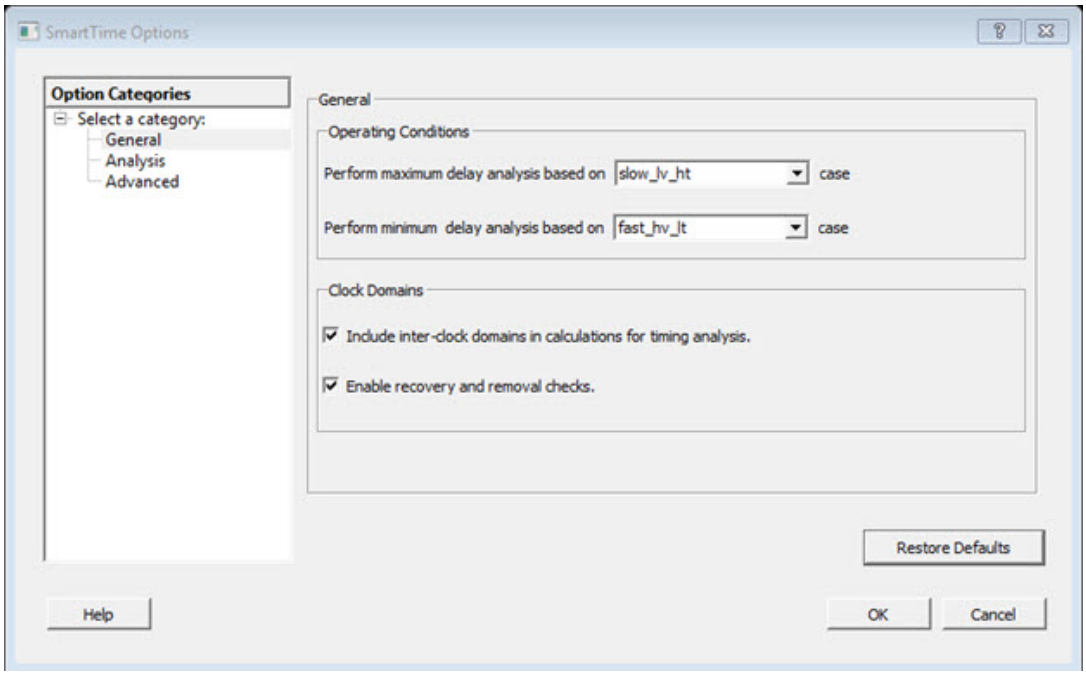


Figure 20 · SmartTime Options Dialog Box for PolarFire

3. Click **OK** to save the dialog box settings.

See Also

Inter-Clock Domain Analysis

Deactivating a Specific Inter-Clock Domain

Displaying Inter-Clock Domain Paths

Displaying Inter-Clock Domain Paths

Once you activate the inter-clock domain checking for a given clock domain CK1, SmartTime automatically detects all other domains CKn with paths ending at CK1. SmartTime creates inter-clock domain sets CKn to CK1 under the domain CK1. Each of these sets enables you to display the inter-clock domain paths between a given clock domain and CK1.

To display an inter-clock domain set:

1. Expand the receiving clock domain of the inter-clock domain in the Domain Browser to display its related sets. For the inter-clock domain CK1 to CK2, expand clock domain CK2.
2. Select the inter-clock domain that you want to see expanded from these sets. Once selected, all paths between the related two domains are displayed in Paths List in the same way as any register to register set.

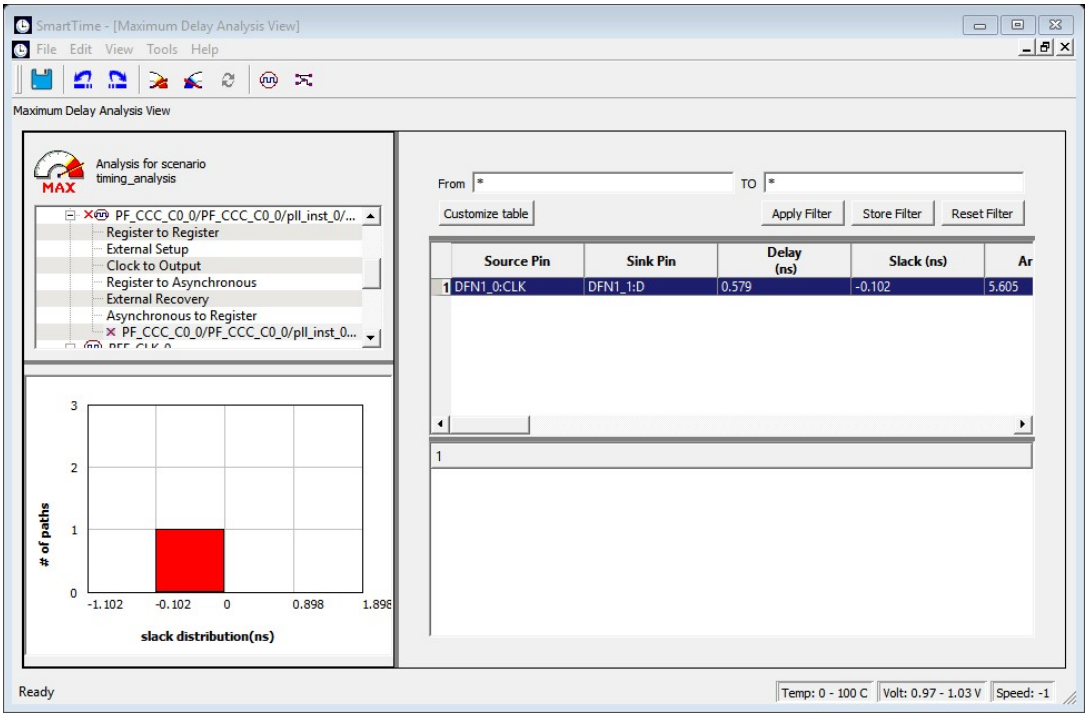


Figure 21 · Maximum Delay Analysis View

See Also

Understanding inter-clock domain analysis

Activating inter-clock domain analysis

Deactivating a specific inter-clock domain

Deactivating a Specific Inter-Clock Domain

To deactivate the inter-clock domain checking for the specific clock domains clk2->clk1, without disabling this option for the other clock domains:

1. From the **Tools** menu, choose **Constraints Editor > Primary Scenario** to open the Constraints Editor View.
2. In the Constraints Browser, double-click **False Path** under **Exceptions**. The **"Set False Path Constraint** dialog box appears.
3. Click the **Browse** button to the right of the **From** text box. The **Select Source Pins for False Path Constraint** dialog box appears.
4. For **Specify pins**, select **by keyword and wildcard**.
5. For **Pin Type**, select **Registers by clock names** from the **Pin Type** drop-down list.
6. Type the inter-clock domain name, for example **Clk2** in the filter box and click **Filter**.
7. Click **OK** to begin filtering the pins by your criteria. In this example, [get_clocks {Clk2}] appears in the **From** text box in the **Set False Path Constraint** dialog box.
8. Repeat steps 3 to 7 for the **To** option in the Set False Path Constraint dialog box, and type Clk2 in the filter box.
9. Click **OK** to validate the new false path and display it in the Paths List of the Constraints Editor.
10. Click the Recalculate All icon  in the toolbar.
11. Select the inter-clock domain set clk2 -> clk1 in the Domain Browser (as shown below).
12. Verify that the set does not contain any paths.

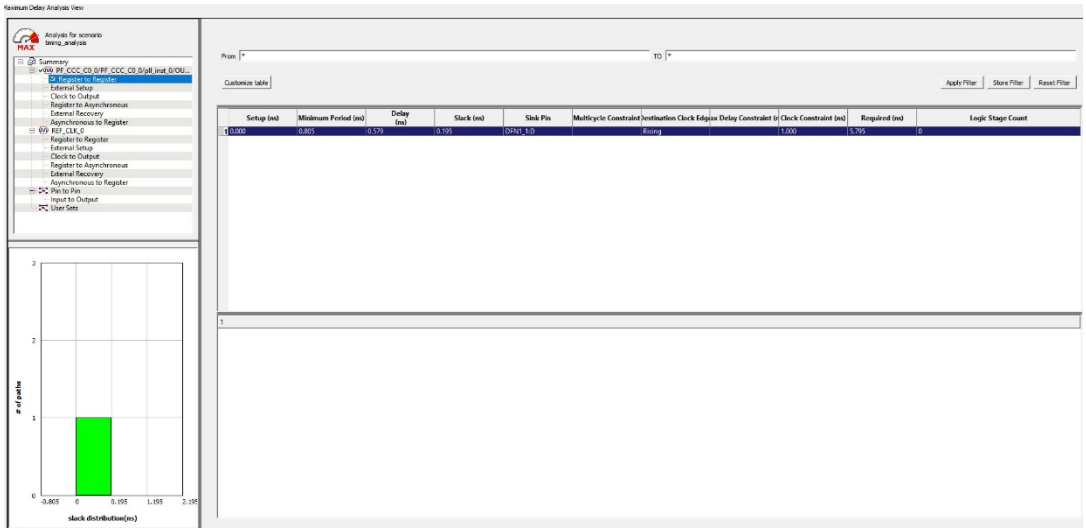


Figure 22 · Maximum Delay Analysis View

See Also

Understanding inter-clock domain analysis

Activating inter-clock domain analysis

Displaying inter-clock domain paths

Select Source or Destination Pins for Constraint dialog box

Set False Path Constraint dialog box

Changing Output Port Capacitance

Output propagation delay is affected by both the capacitive loading on the board and the I/O standard. The I/O Attribute Editor in ChipPlanner provides a mechanism for setting the expected capacitance to improve the propagation delay model. SmartTime automatically uses the modified delay model for delay calculations.

To change the output port capacitance and view the effect of this change in SmartTime Timing Analyzer, refer to the following example. The figure below shows the delay from DFN1 to output port Q. It shows a delay of 6.603 ns based on the default loading of 5 pF.

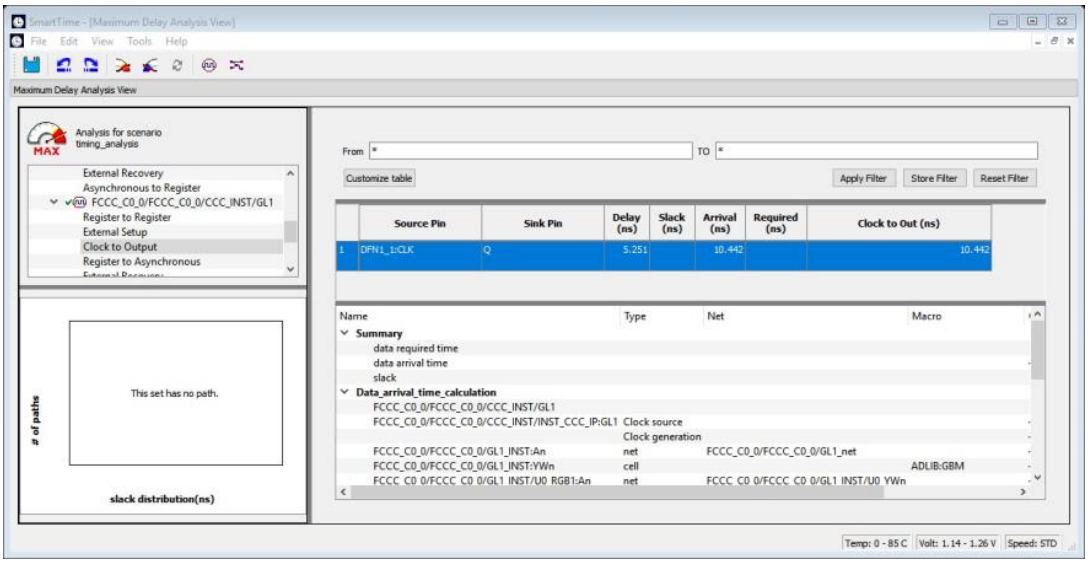


Figure 23 · Maximum Delay Analysis View

If your board has output capacitance of 15 pf on Q, you must perform the following steps to update the timing number:

1. Open the I/O Attribute Editor and change the output load to 15 pf.

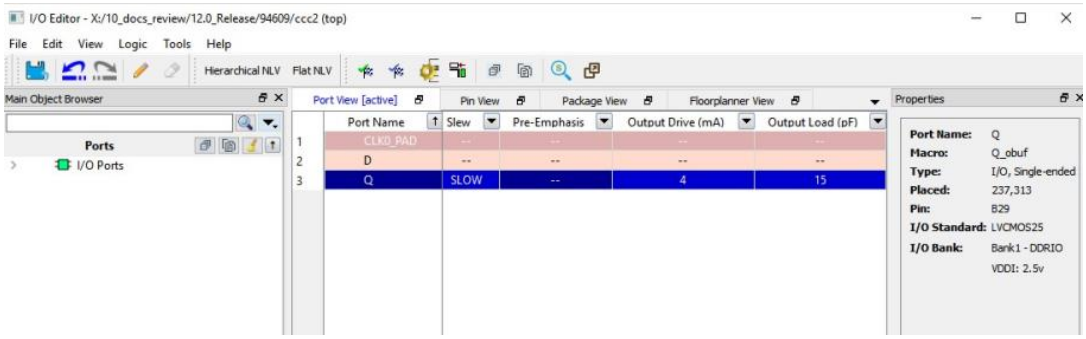


Figure 24 · I/O Attribute Editor View

2. Select **File > Save**.
3. Select **File > Close**.
4. Open the SmartTime Timing Analyzer.

You can see that the Clock to Output delay changed to 5.952 ns.

Generating Timing Reports

Types of Reports

Using SmartTime you can generate the following types of reports:

- **Timer report** – This report displays the timing information organized by clock domain.
- **Timing Violations report** – This flat slack report provides information about constraint violations.
- **Bottleneck report** – This report displays the points in the design that contribute to the most timing violations.
- **Datasheet report** – This report describes the characteristics of the pins, I/O technologies, and timing properties in the design.
- **Constraints Coverage report** – This report displays the overall coverage of the timing constraints set on the current design.
- **Combinational Loop report** – This report displays loops found during initialization.

See Also

Generating a Timing Report

Generating a Timing Violation Report

Generating a datasheet report

Generating a bottleneck report

Generating a constraints coverage report

Generating a Combinational Loop Report

Generating a Timing Report

The timing report enables you to quickly determine if any timing problems exist in your design. The Maximum Delay Analysis timing report lists the following information about your design:

- Maximum delay from input I/O to output I/O
- Maximum delay from input I/O to internal registers
- Maximum delay from internal registers to output I/O
- Maximum delays for each clock network
- Maximum delays for interactions between clock networks

To generate a timing report:

1. From the SmartTime Max/Min Delay Analysis View, choose **Tools > Reports > Timer**. The Timing Report Options Dialog Box appears.
2. Select the options you want to include in the report, and then click **OK**.

The timing report appears in a separate window.

See Also

Understanding Timing Reports

Timing Report Options Dialog Box

Understanding Timing Reports

The timing report contains the following sections:

Header

The header lists:

- The report type
- The version of Designer used to generate the report
- The date and time the report was generated
- General design information (name, family, etc.)

Summary

The summary section reports the timing information for each clock domain.

By default, the clock domains reported are the explicit clock domains that are shown in SmartTime. You can filter the domains and get only specific sections in the report (see Timing Report Options Dialog Box).

Path Sections

The paths section lists the timing information for different types of paths in the design. This section is reported by default. You can deselect this option in the Timing Report Options Dialog Box.

By default, the number of paths displayed per set is 5.

You can filter the domains using the Timing Report Options dialog box.

You can also view the stored filter sets in the generated report using the timing report options. The filter sets are listed by name in their appropriate section, and the number of paths reported for the filter set is the same as for the main sets.

By default, the filter sets are not reported.

Clock domains

The paths are organized by clock domain.

Register to Register set

This set reports the paths from the registers clock pins to the registers data pins in the current clock domain.

External Setup set

This set reports the paths from the top level design input ports to the registers in the current clock domain.

Clock to output set

This set reports the paths from the registers clock pins to the top level design output ports in the current clock domain.

Register to Asynchronous set

This set reports the paths from registers to asynchronous control signals (like asynchronous set/reset).

External Recovery set

This set reports the external recovery check timing for asynchronous control signals (like asynchronous set/reset).

Asynchronous to Register set

This set reports the paths from asynchronous control signals (like asynchronous set/reset) to registers.

Inter-clock domain

This set reports the paths from the registers clock pins of the specified clock domain to the registers data pins in the current clock domain. Inter-domain paths are not reported by default.

Pin to pin

This set lists input to output paths and user sets. Input to output paths are reported by default. To see the user-defined sets, use the Timing Report Options Dialog Box.

Input to output set

This set reports the paths from the top level design input ports to top level design output ports.

Expanded Paths

Expanded paths can be reported for each set. By default, the number of expanded paths to report is set to 1. You can select and change the number when you specify Timing Report Options.

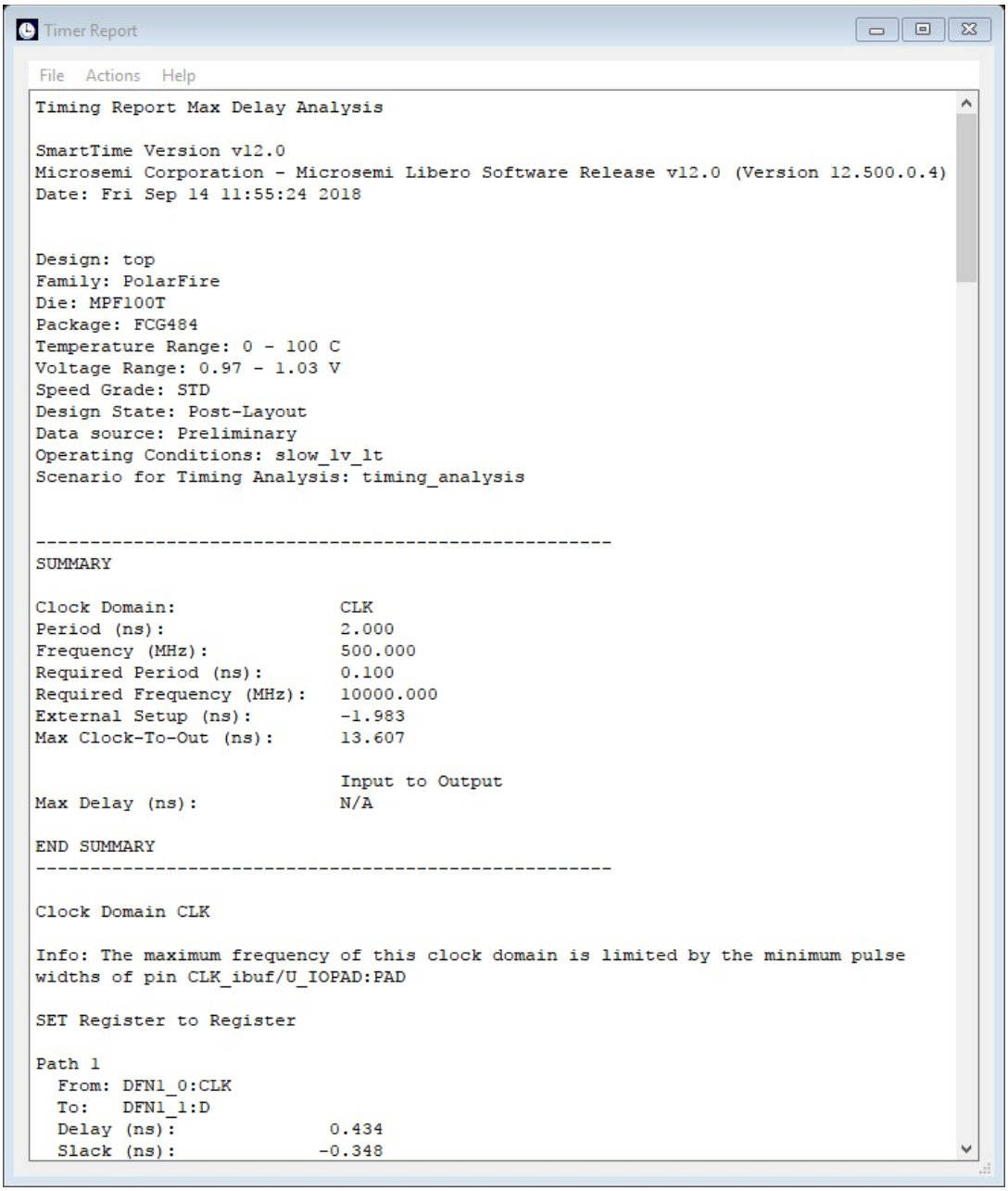


Figure 25 · Timing Report

See Also

Generating a Timing Report

Timing Report Options Dialog Box

Generating a Timing Violation Report

The timing violations report provides a flat slack report centered around constraint violations.

To generate a timing violation report

1. From the SmartTime Max/Min Delay Analysis View window, choose **Tools > Reports > Timing Violations**. The Timing Violations Report Options Dialog Box appears.

2. Select the options you want to include in the report, and then click **OK**. The timing violations report appears in a separate window.

See Also

Understanding Timing Violation Reports

Understanding Timing Violation Reports

The timing violation report contains the following sections:

Header

The header lists:

- The report type
- The version of Designer used to generate the report
- The date and time the report was generated
- General design information (name, family, etc.)

Paths

The paths section lists the timing information for the violated paths in the design.

The number of paths displayed is controlled by two parameters:

- A maximum slack threshold to report
- A maximum number or path to report

By default, the slack threshold is 0 and the number of paths is limited. The default maximum number of paths reported is 100.

All clocks domains are mixed in this report. The paths are listed by decreasing slack.

You can also choose to expand one or more paths. By default, no paths are expanded. For details, see the timing violation report options.

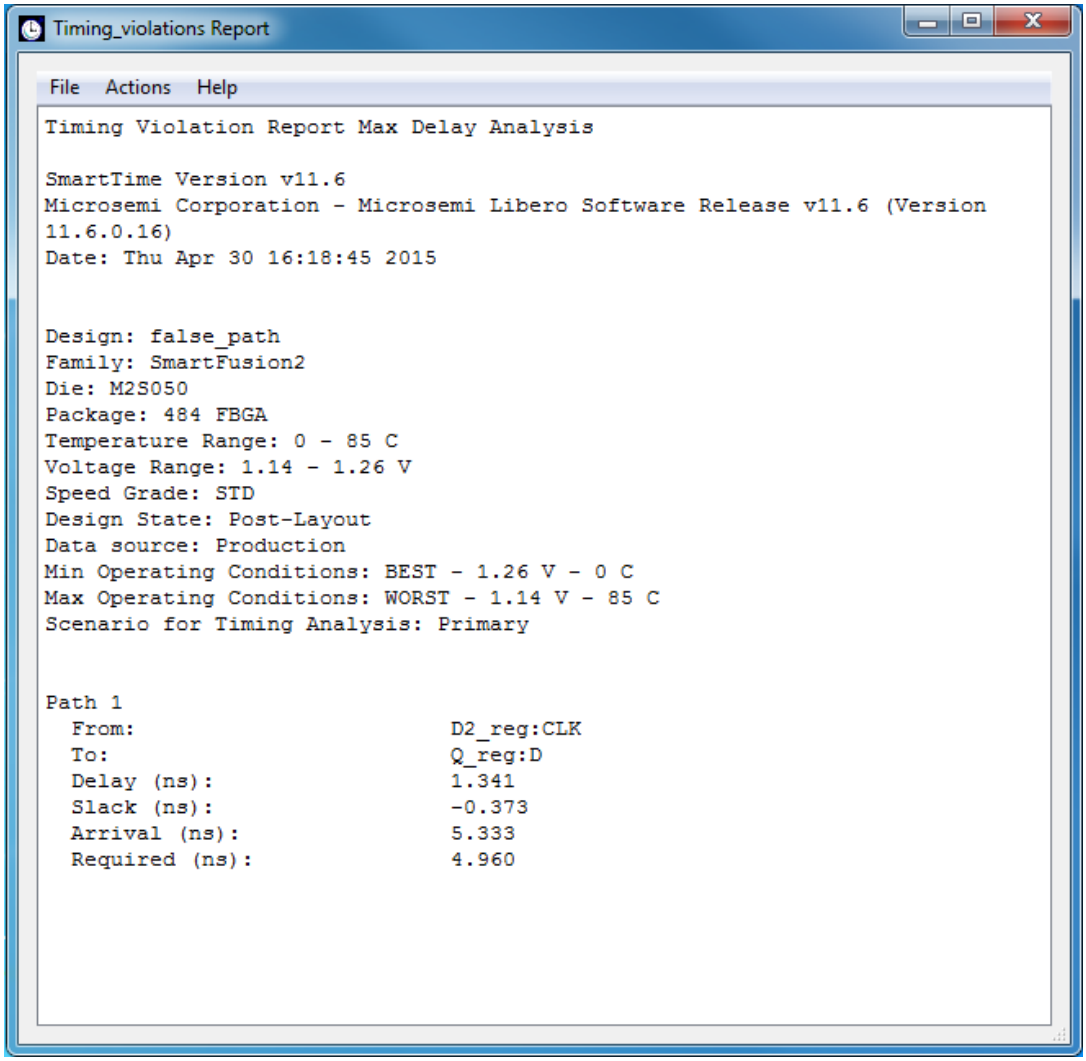


Figure 26 · Timing Violations Report

See Also

Generating a Timing Violation Report

Timing Violations Report Options Dialog Box

Generating a Constraints Coverage Report

The constraints coverage report contains information about the constraints in the design.

To generate a constraints coverage report, from the SmartTime Max/Min Delay Analysis View, choose **Tools > Reports > Constraints Coverage**. Select the text format and number of unconstrained instances and click **OK**. The report appears in a separate window.

See Also

Understanding Constraints Coverage Reports

Understanding Constraints Coverage Reports

The constraint coverage displays the overall coverage of the timing constraints set on the current design. You can generate this report either from within Designer or within SmartTime Analyzer. The report contains three sections:

- Coverage Summary
- Results by Clock Domain
- Enhancement Suggestions

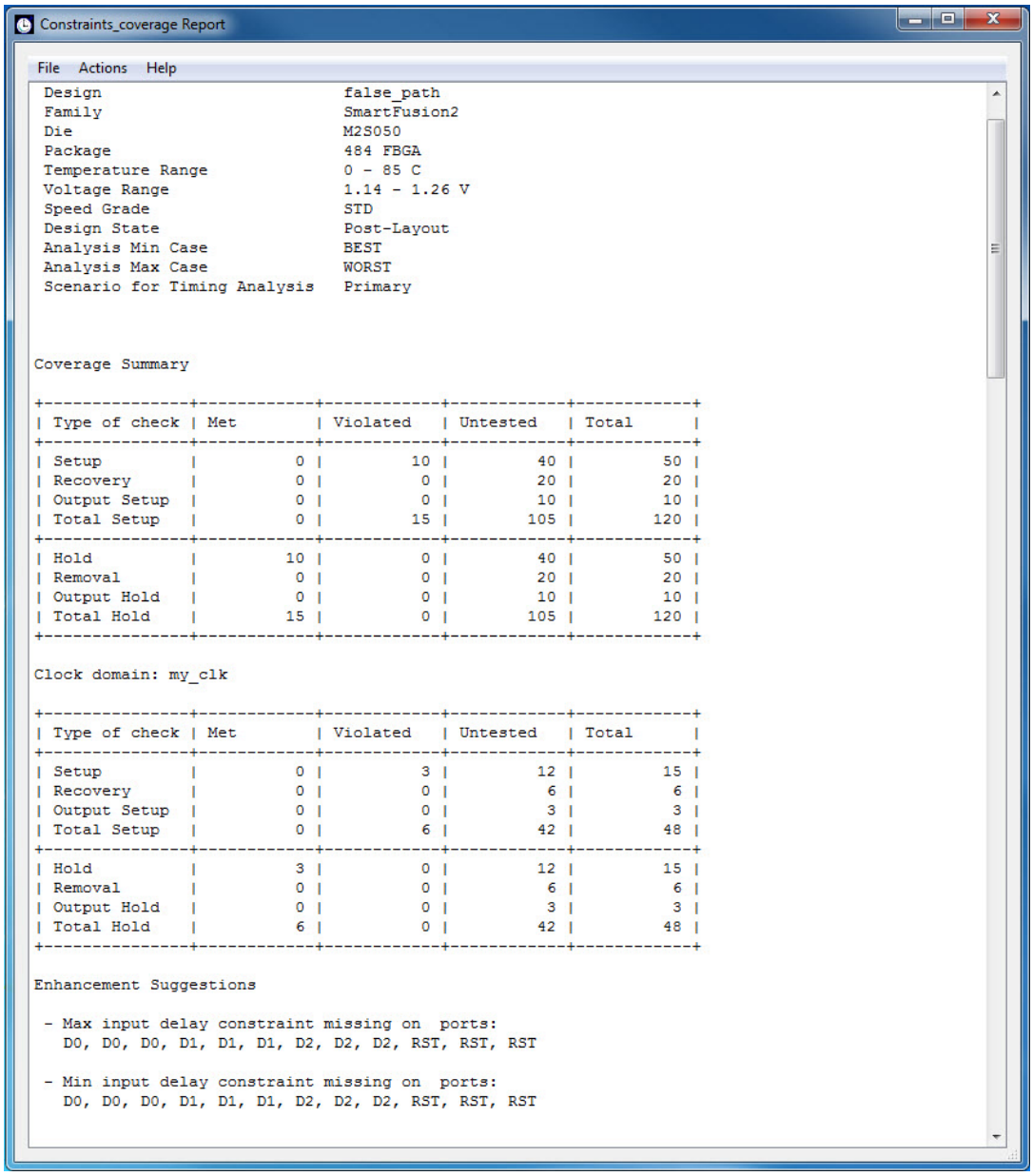


Figure 27 · Constraints Coverage Report

Coverage Summary

The coverage summary gives statistical information on the timing constraint in the design. For each type of timing checks (Setup, Recovery, Output, Hold and Removal), it specifies how many are Met (there is a constraint and it is satisfied), Violated (there is a constraint and it is not satisfied), or Untested (no constraint was found).

Clock Domain

This section provides a coverage summary for each clock domain.

Enhancement Suggestions

The enhancement suggestion reports, per clock domain, a list of constraints that can be added to the design to improve the coverage. It also reports if some options impacting the coverage can be changed.

Detailed Stats

This section provides detailed suggestions regarding specific clocks or I/O ports that may require to be constrained for every pin/port that requires checks.

Setting SmartTime Options

Generating a Bottleneck Report

The bottleneck report provides a list of the bottlenecks in the design.

To generate a bottleneck report, from the,SmartTime Max/Min Delay Analysis View, choose **Tools > Reports > Bottleneck**. The report appears in a separate window.

See Also

Understanding Bottleneck Reports

Timing Bottleneck Analysis Options Dialog Box

Understanding Bottleneck Reports

A bottleneck is a point in the design that contributes to multiple timing violations. The purpose of the bottleneck report is to provide a list of the bottlenecks in the design. You can generate this report either from SmartTime Analyzer. It contains two sections

- Device Description
- Bottleneck Analysis

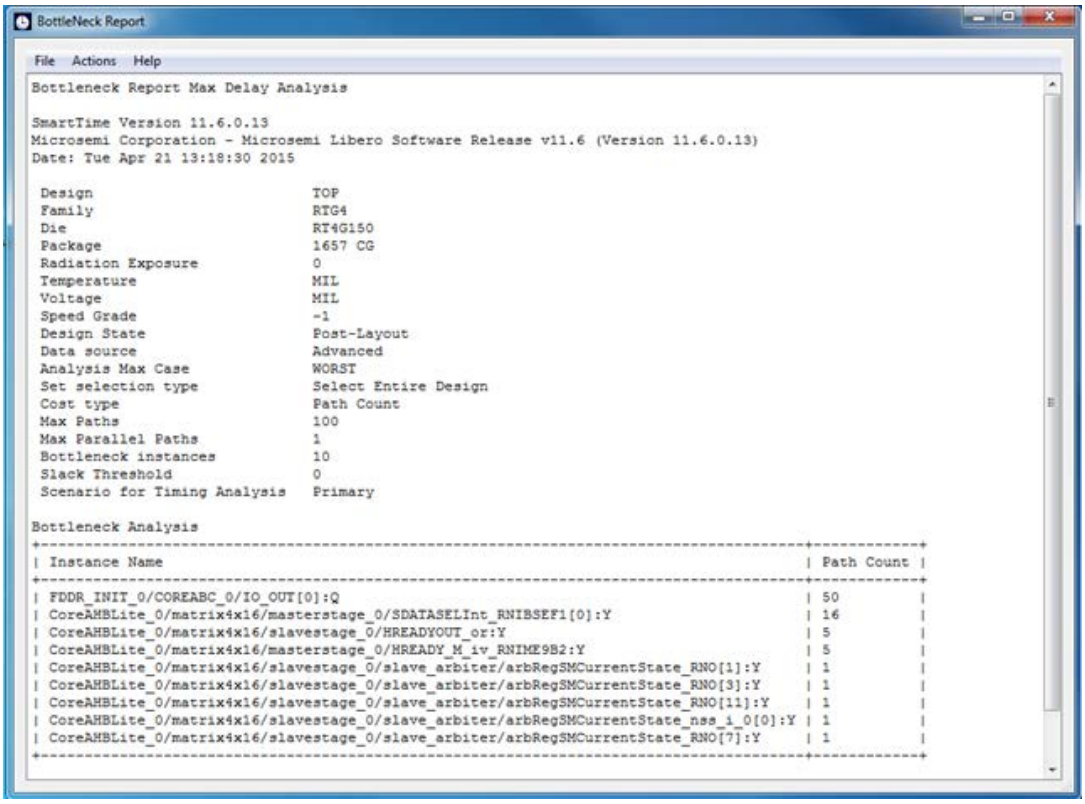


Figure 28 · Bottleneck Report

The bottleneck can only be computed if and only a cost type is defined. There are two options available:

- **Path count:** This cost type associates the severity of the bottleneck to the count of violating/critical paths that traverse the instance.
- **Path cost:** This cost type associates the severity of the bottleneck to the sum of the timing violations for the violating/critical paths that traverse the instance.

Device Description

The device section contains general information about the design, including:

- Design name
- Family
- Die
- Package
- Software version

Bottleneck Analysis

This section lists the core of the bottleneck information. It is divided into two columns:

- Instance name: refers to the output pin name of the instance.
- Path Count: Displays the number of violating paths which include the instance pin.

See Also

Timing Bottleneck Analysis Options Dialog Box

Generating a Datasheet Report

The datasheet reports information about the external characteristics of the design.

Note: Generating Datasheet Report is not supported in PolarFire.

To generate a datasheet report, from the SmartTime Max/Min Delay Analysis View, choose **Tools > Reports > Datasheet**. The report appears in a separate window.

See Also

Understanding Datasheet Reports

Timing Datasheet Report Options Dialog Box

Understanding Datasheet Reports

The datasheet report displays the external characteristics of the design. . You can generate this report from SmartTime Max/Min Delay Analysis View. It contains three tables:

- Pin Description
- DC Electrical Characteristics
- AC Electrical Characteristics

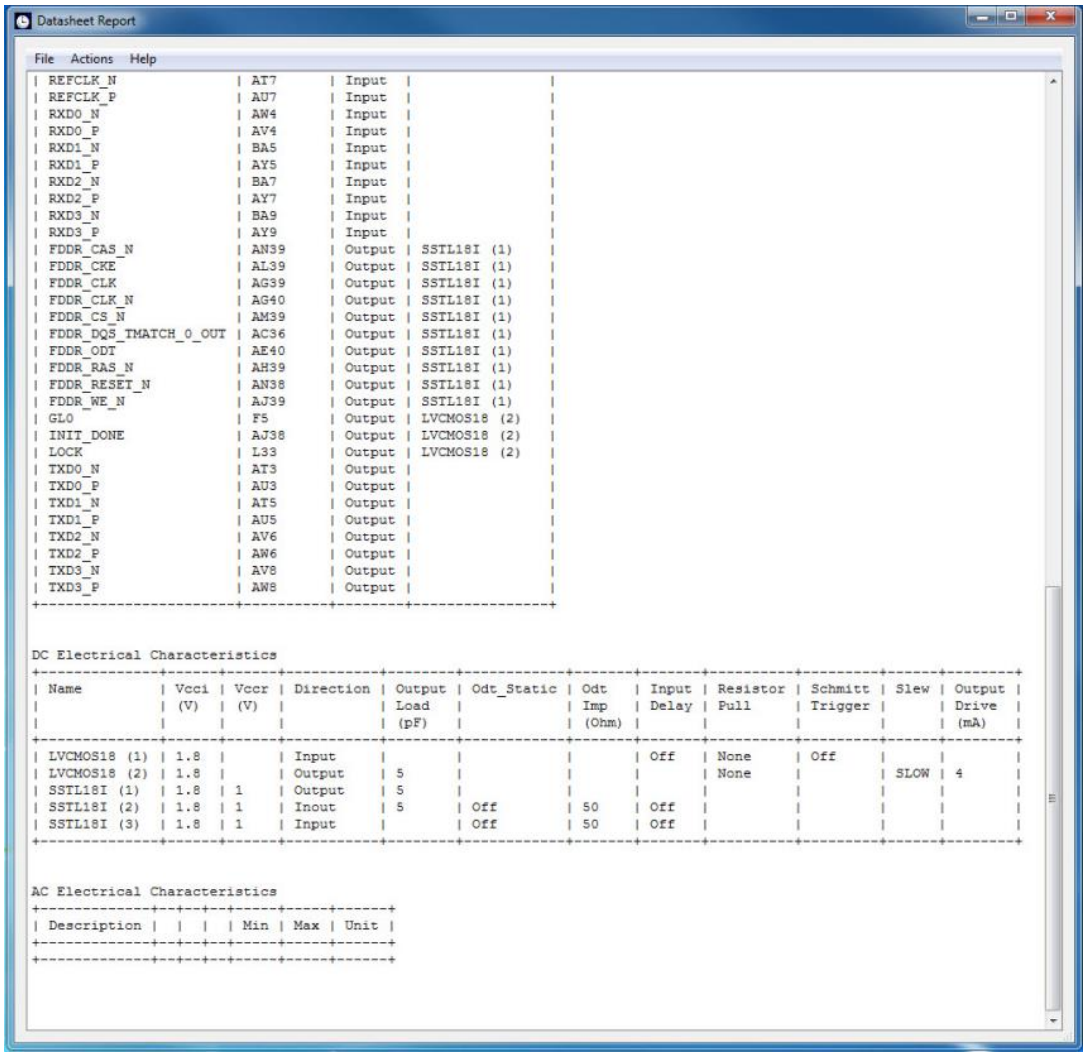


Figure 29 · Datasheet Report

Pin Description

Provides the port name in the netlist, location on the package, type of port, and I/O technology assigned to it. Types can be input, output, inout, or clock. Clock ports are ports shown as "clock" in the Clock domain browser.

DC Electrical Characteristics

Provides the parameters of the different I/O technologies used in the design. The number of parameters displayed depends on the family for which you have created the design.

AC Electrical Characteristics

Provides the timing properties of the ports of the design. For each clock, this section includes the maximum frequency. For each input, it includes the external setup, external hold, external recovery, and external removal for every clock where it applies. For each output, it includes the clock-to-out propagation time. This section also displays the input-to-output propagation time for combinational paths.

See Also

Generating a Datasheet Report

Timing Datasheet Report Options Dialog Box

Generating a Combinational Loop Report

The combinational loop report displays all loops found during initialization and reports pins associated with the loop(s), and the location where the loop is broken.

To generate the combinational loop report; from the **Tools** menu, choose **Reports > Combinational Loops ...**.

Select either the **Plain Text** or **Comma Separated Values** option in the Combinational_Loops Report Options dialog box and click **OK**.

The plain text report will pop up in a new window; you will be prompted to save the CSV in a directory of your choosing.

See Also

Understanding Combinational Loop Reports

Understanding Combinational Loop Reports

The combinational loop report displays all loops found during initialization and reports pins associated with the loop(s), and the location where the loop is broken.

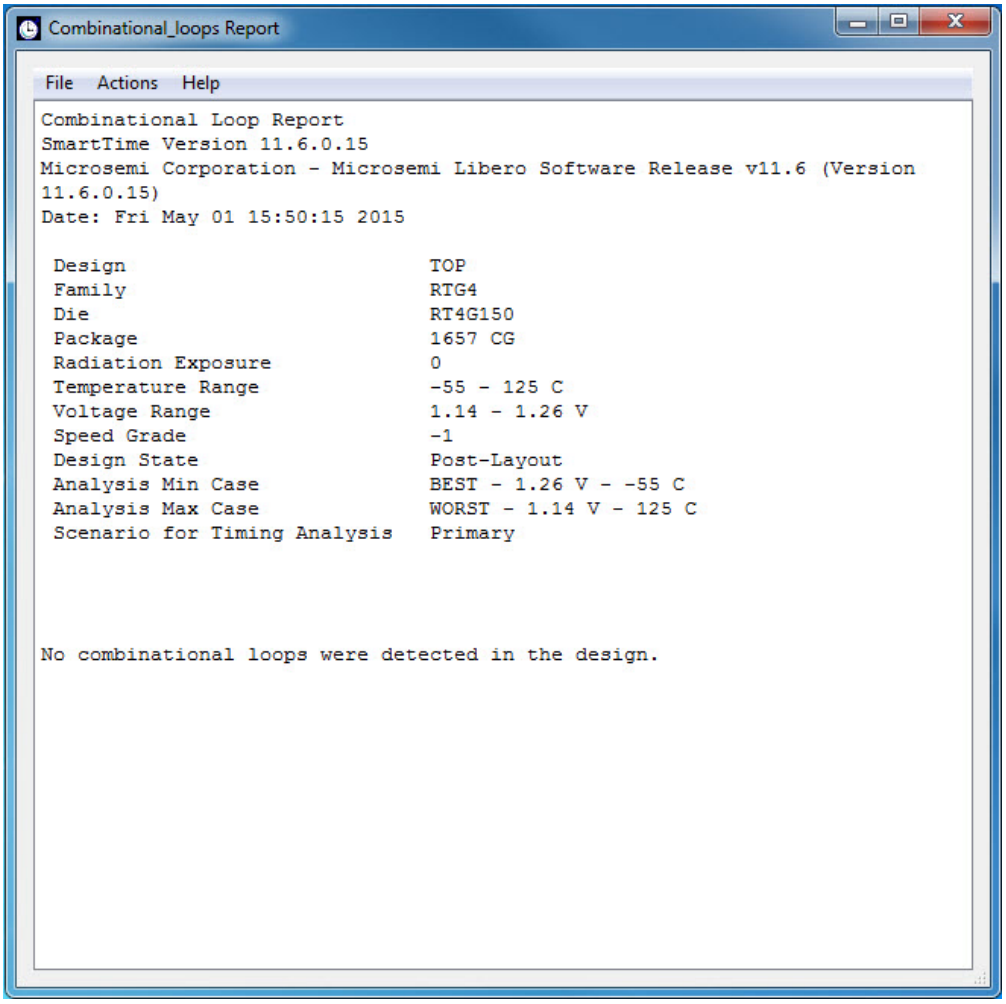


Figure 30 · Combinational Loop Report

See Also

Generating a Combinational Loop Report

Timing Concepts

Static Timing Analysis Versus Dynamic Simulation

Static timing analysis (STA) offers an efficient technique for identifying timing violations in your design and ensuring that it meets all your timing requirements. You can communicate timing requirements and timing exceptions to the system by setting timing constraints. A static timing analysis tool will then check and report setup and hold violations as well as violations on specific path requirements.

STA is particularly well suited for traditional synchronous designs. The main advantage of STA is that unlike dynamic simulation, it does not require input vectors. It covers all possible paths in the design and does all the above with relatively low run-time requirements. The major disadvantage of STA is that the STA tools do not automatically detect false paths in their algorithms.

Delay Models

The first step in timing analysis is the computation of single component delays. These components could be either a combinational gate or block or a single interconnect connecting two components.

Gates that are part of the library are pre-characterized with delays under different parameters, such as input-slew rates or capacitive loads. Traditional models provide delays between each pair of I/Os of the gate and between rising and falling edges.

The accuracy with which interconnect delays are computed depends on the design phase. These can be estimated using a simple Wire Load Model (WLM) at the pre-layout phase, or a more complex Resistor and Capacitor (RC) tree solver at the post-layout phase.

Timing Path Types

Path delays are computed by adding delay values across a chain of gates and interconnects. SmartTime uses this information to check for timing violations. Traditionally, timing paths are presented by static timing analysis tools in four categories or "sets":

- Paths between sequential components internal to the design. SmartTime displays this category under the Register to Register set of each displayed clock domain.
- Paths that start at input ports and end at sequential components internal to the design. SmartTime displays this category under the External Setup and External Hold sets of each displayed clock domain.
- Paths that start at sequential components internal to the design and end at output ports. SmartTime displays this category under the Clock to Out set of each displayed clock domain.
- Paths that start at input ports and end at output ports. SmartTime displays this category under the Input to Output set.

Maximum Clock Frequency

Generally, you set clock constraints on clocks for which you have a specified requirement. The absence of violations indicates that this clock will be able to run at least at the specified frequency. However, in the absence of such requirements, you may still be interested in computing the maximum frequency of a specific clock domain.

To obtain the maximum clock frequency, a static timing analysis tool computes the minimum period for each path between two sequential elements. To compute the maximum period, the tool evaluates the maximum data path delay and the minimum skew between the two elements, as well as the setup on the receiving sequential element. It also considers the polarity of each sequential element. The maximum frequency is the inverse of the largest value among the maximum period of all the paths in the clock domain. The path responsible for limiting the frequency of a given clock is called the critical path.

Setup Check

The setup and hold check ensures that the design functions as specified at the required clock frequency.

Setup check specifies when data is required to be present at the input of a sequential component in order for the clock to capture this data effectively into the component. Timing analyzers evaluate the setup check as a maximum timing budget allowed between adjacent sequential elements. For more details on how setup check is processed, refer to Arrival Time, Required Time, and Slack.

See Also

Static Timing Analysis Versus Dynamic Simulation

Arrival Time, Required Time, and Slack

Arrival Time, Required Time and Slack

You can use arrival time and required time to verify timing requirements in the presence of constraints. Below is a simple example applied to verifying the clock requirement for setup between sequential elements in the design.

The arrival time represents the time at which the data arrives at the input of the receiving sequential element. In this example, the arrival time is considered from the setup launch edge at CK, taken as a time reference (instant zero). It follows the clock network along the blue line until the clock pin on FF1 (delay d1). Then it continues along the data path always following the blue line until the data pin D on FF2. Therefore,

$Arrival\_Time_{FF2:D} = d1 + d2$

The required time represents when the data is required to be present at the same pin FF2:D. Assume in this example that in the presence of an FF with the same polarity, the capturing edge is simply one cycle following the launch edge. Using the period T provided to the tool through the clock constraint, the event gets propagated through the clock network along the red line until the clock pin of FF2 (delay d3). Taking into account FF2 setup (delay d4), this means that the clock constraint requires the data to be present d4 time before the capturing clock edge on FF2. Therefore, the required time is:

$Required\_Time_{FF2:D} = T + d3 - d4$

The slack is simply the difference between the required time and arrival time:

$Slack_{FF2:D} = Required\_Time_{FF2:D} - Arrival\_TimeFF2:D$

If the slack is negative, the path is violating the setup relationship between the two sequential elements.

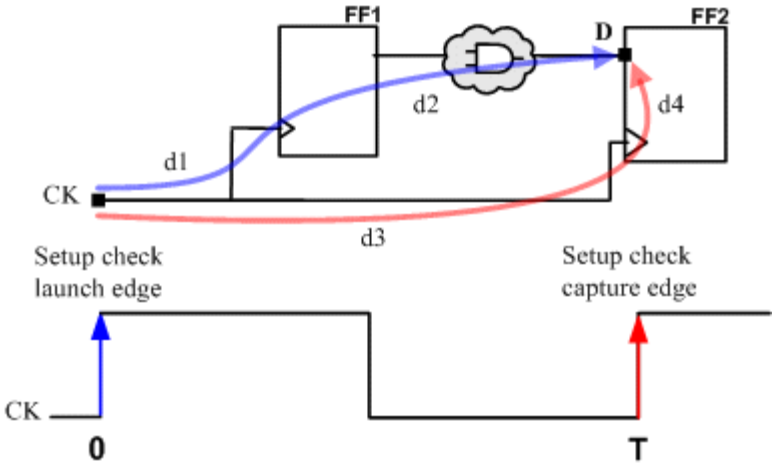


Figure 31 · Arrival Time and Required Time for Setup Check

Timing Exceptions Overview

Use timing exceptions to overwrite the default behavior of the design path. Timing exceptions include:

- Setting multicycle constraint to specify paths that (by design) will take more than one cycle.
- Setting a false path constraint to identify paths that must not be included in the timing analysis or the optimization flow.
- Setting a maximum/minimum delay constraint on specific paths to relax or to tighten the original clock constraint requirement.

Clock Skew

The clock skew between two different sequential components is the difference between the insertion delays from the clock source to the clock pins of these components. SmartTime calculates the arrival time at the clock pin of each sequential component. Then it subtracts the arrival time at the receiving component from the arrival time at the launching component to obtain an accurate clock skew.

Both setup and hold checks must account for clock skew. However, for setup check, SmartTime looks for the smallest skew. This skew is computed by using the maximum insertion delay to the launching sequential component and the shortest insertion delay to the receiving component.

For hold check, SmartTime looks for the largest skew. This skew is computed by using the shortest insertion delay to the launching sequential component and the largest insertion delay to the receiving component. SmartTime makes this distinction automatically.

Cross Probing

Design objects displayed in SmartTime can be cross-probed into other Libero SoC tools. Libero SoC allows cross-probing from SmartTime to the Constraints Editor (but not vice versa) and from SmartTime to Chip Planner (but not vice versa). When cross-probing from SmartTime to one of the other tools, both SmartTime and the other tool must first be opened.

From SmartTime to Constraint Editor

You can add a timing exception constraint from SmartTime and have the Constraints Editor display the Constraint. From the SmartTime Maximum or Minimum Delay Analysis View, click a timing path to add a timing exception constraint. When the Constraints Editor's Add Constraint dialog box opens, the fields for source (from) pin and destination (to) pin are populated with the correct names from the timing path you have selected.

To add a timing exception constraint from a timing path in SmartTime Max/Min Delay Analysis View:

1. Open SmartTime (**Design Flow Window > Verify Timing > Open interactively**).
2. Open the Constraints Editor (**Constraint Manager > Timing Tab > Edit with Constraints Editor**).
3. Select Max/Min Delay Analysis View and right-click a timing path in the table.
4. Select a timing exception constraint to add: False Path Constraint, Maximum Delay Constraint, Minimum Delay Constraint, or Multicycle Path Constraint.

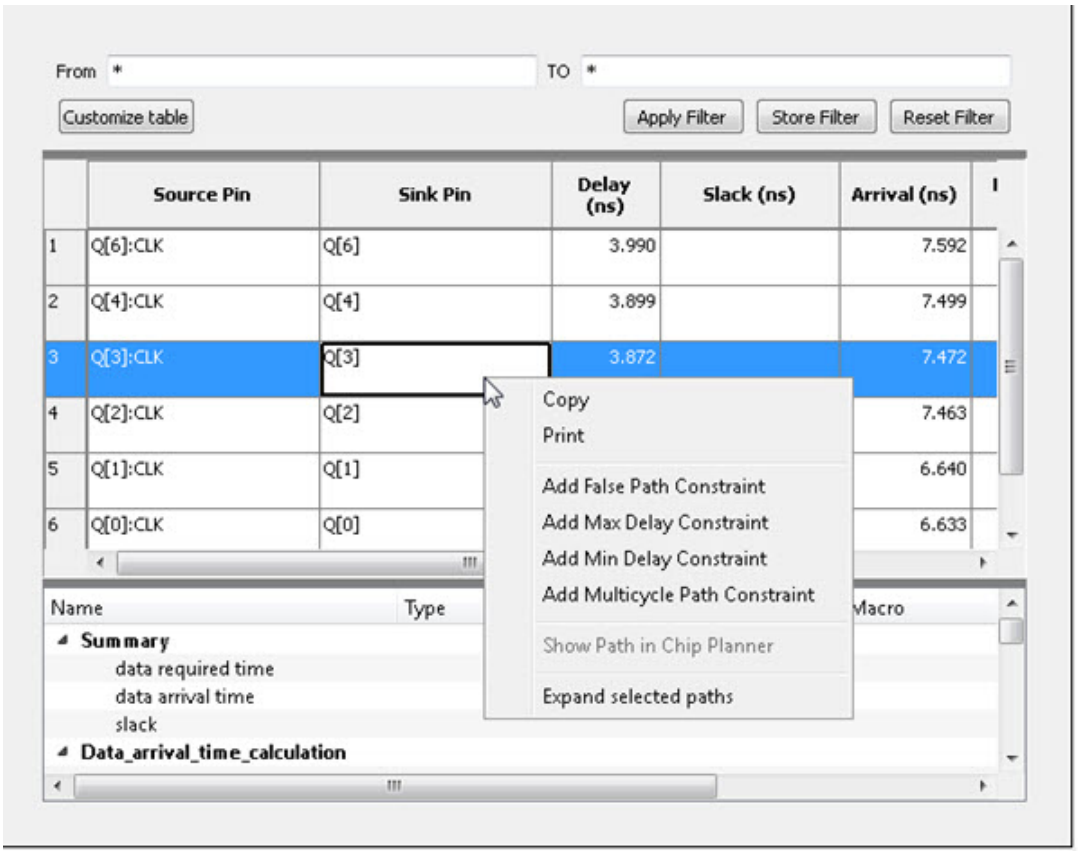


Figure 32 · Add Timing Constraint from SmartTime's Reported Timing Path

Note: The Add Max/Min Delay, False Path, and Multicycle Path Constraint menu items are grayed out if the Constraint Editor is not open.

Add the Constraint in the Add Constraint dialog box. Note that the source/from pin and destination/to pin field are populated with the correct pin names captured from the SmartTime reported path (Source Pin and Sink Pin) you have clicked.

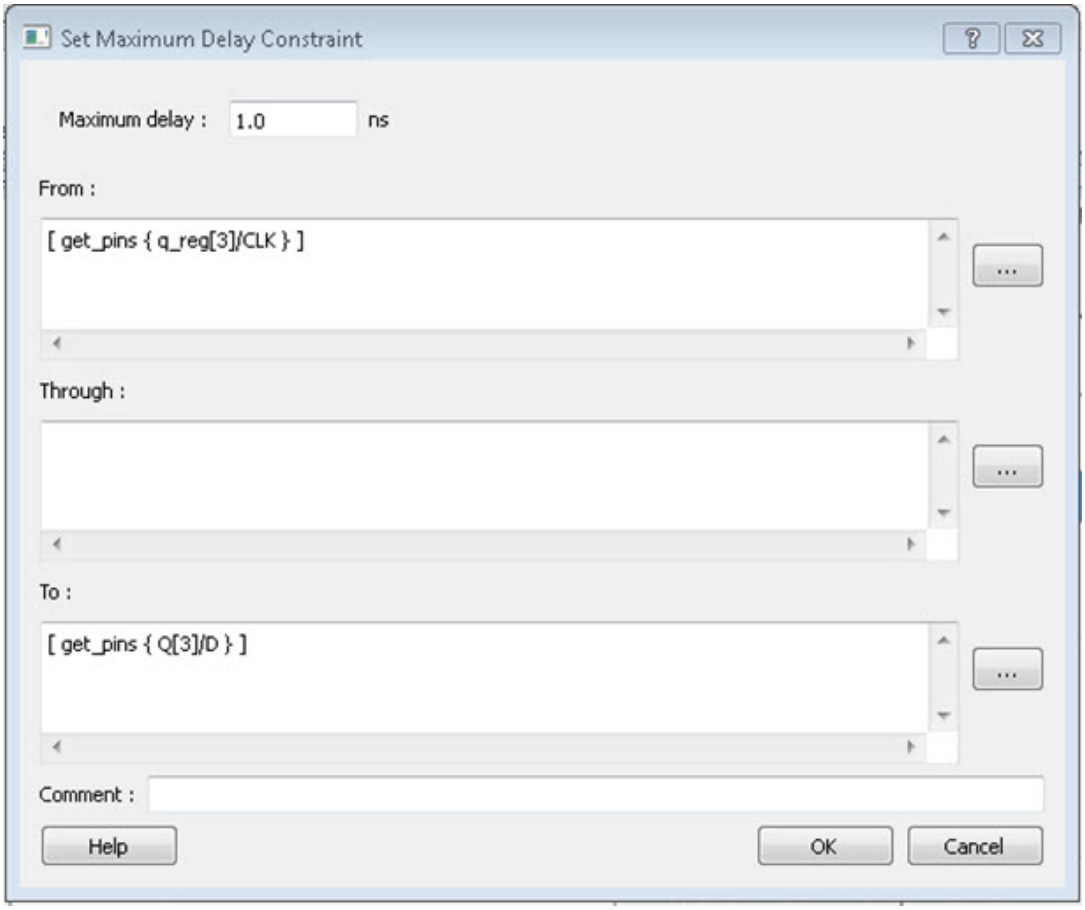


Figure 33 · Add Maximum Delay Constraint

5. Click **OK** to exit the Add Constraint Dialog box.
6. Click **Save** in the Constraints Editor.
7. Exit the Constraints Editor.
8. Exit SmartTime.
9. Rerun Place and Route if the newly-added constraint that is added to a file (the Target file) is used for Place and Route and Verify Timing.
10. Open SmartTime Maximum/Minimum Delay Analysis View.

From SmartTime to Chip Planner

Cross-probing allows you to select a design object in one application and display the selected object in another application. Because Libero SoC allows you to cross-probe design objects from SmartTime to Chip Planner, you can better understand how the two applications interact with each other. With cross-probing, a timing path not meeting timing requirements can be fixed with relative ease when you see the less-than-optimal placement of the design object (in terms of timing requirements) in Chip Planner. Cross-probing from SmartTime to Chip Planner is available for the following design objects:

- Macros
- Ports
- Nets/Paths

Note: Cross-probing of design objects is available from SmartTime to Chip Planner but not vice versa.

Before you can cross-probe from SmartTime to Chip Planner, you must:

1. Complete the Place and Route step on the design.
2. Open both SmartTime and Chip Planner.

Cross-Probing Examples

To cross-probe from SmartTime to Chip Planner, a design macro in SmartTime is used.

Design Macro Example

1. Make sure that the design has successfully completed the Place and Route step.
2. Open SmartTime Maximum/Minimum Analysis View.
3. Open Chip Planner.
4. In the SmartTime Maximum Analysis View, right-click the instance Q[2] in the Timing Path Graph and choose **Show in Chip Planner**. Note that with cross-probing, the Q[2] macro is selected in Chip Planner's Logical View and highlighted (white) in the Chip Canvas. The Properties window in Chip Planner displays the properties of Q[2].

Note: Show in Chip Planner is grayed out if Chip Planner is not already open.

Note: You may need to zoom in to view the highlighted Q2 Macro in the Chip Canvas.

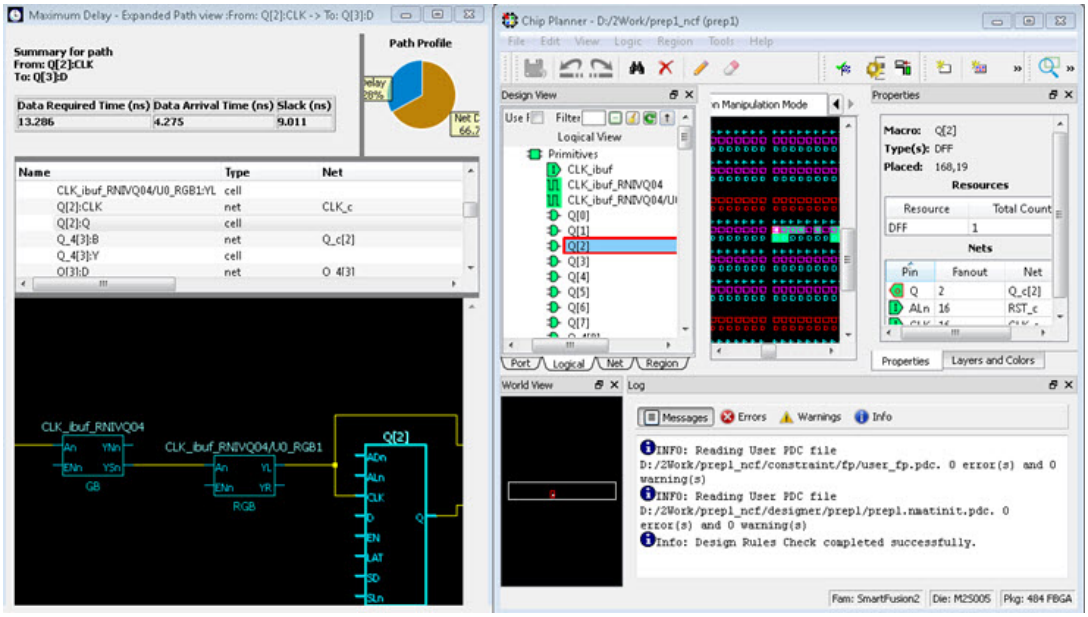


Figure 34 · Cross-Probing – Macro

Timing Path Example

1. Make sure that the design has successfully completed the Place and Route step.
2. Open the SmartTime Maximum/Minimum Analysis View.
3. Open Chip Planner.
4. In the SmartTime Maximum/Minimum Analysis View, right-click the net CLK_ibuf/U0/U_IOPAD:PAD in the Table and choose **Show Path in Chip Planner**. Note that the net is selected (highlighted in red) in the Chip Canvas view and the three macros connected to the net are also highlighted (white) in the Chip Canvas view.

Note: Show Path in Chip Planner is grayed out if Chip Planner is not already open.

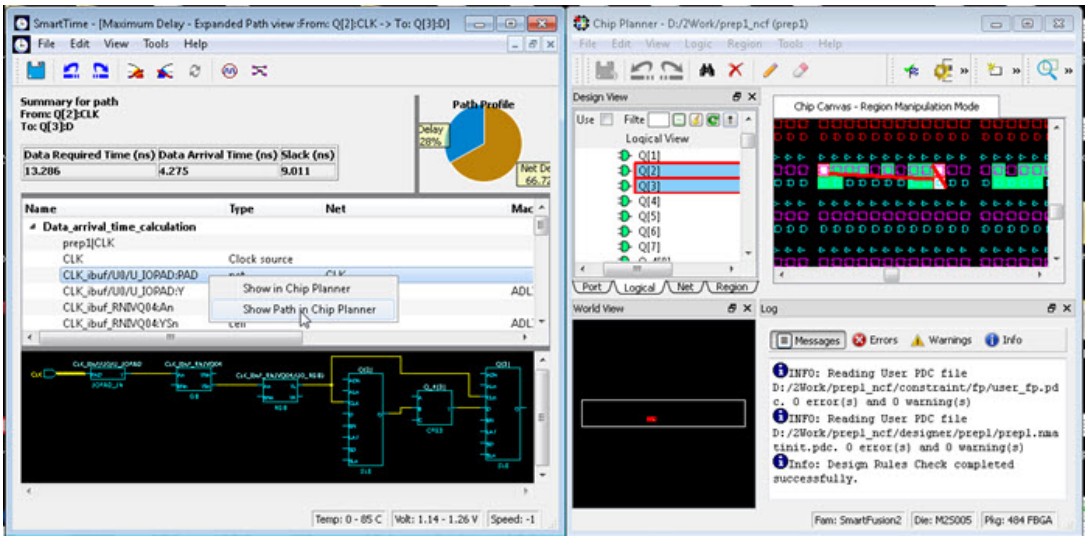


Figure 35 · Cross-Probing – Timing Path

Alternatively, right-click a path in the Max/Min Delay Analysis View and select **Show Path in Chip Planner** to cross-probe the path.

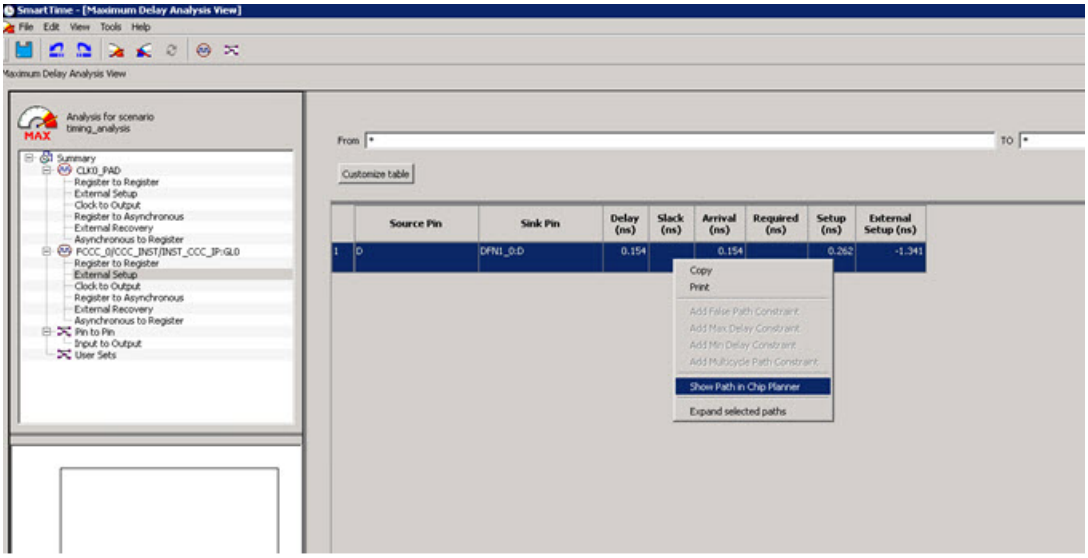


Figure 36 · Cross-Probing Path from Max/Min Delay Analysis View Table

Port Example

1. Make sure that the design has successfully completed the Place and Route step.
2. Open the SmartTime Maximum/Minimum Analysis View.
3. Open Chip Planner.
4. In the SmartTime Maximum/Minimum Analysis View, right-click the Port “CLK” in the Path and choose **Show in Chip Planner**. Note that the Port “CLK” is selected and highlighted in the Chip Planner Port View.

Note: Show in Chip Planner is grayed out if Chip Planner is not already open.

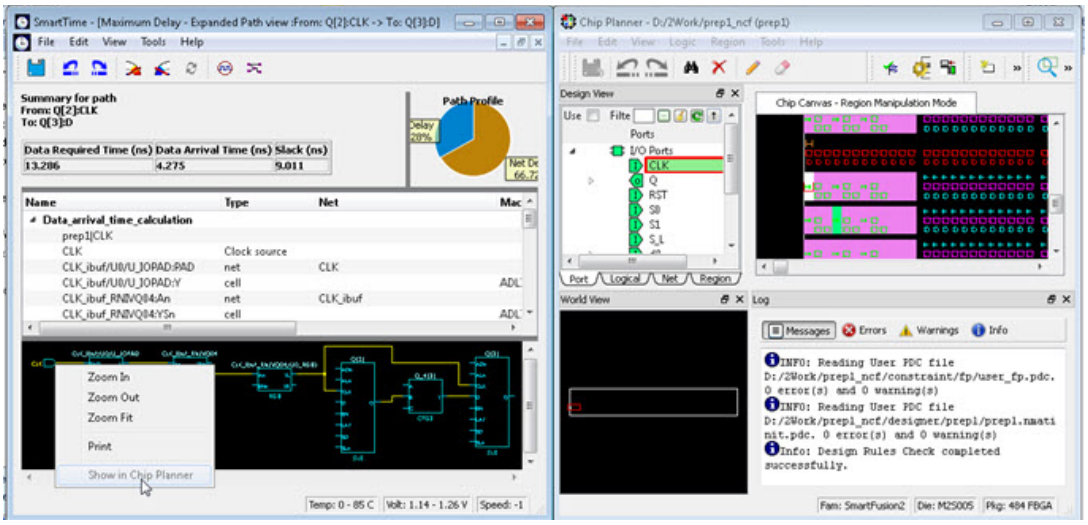


Figure 37 · Cross-Probing – Port

From the Properties View inside Chip Planner, you will find useful information about the Port “CLK” you are cross-probing:

- Port Type
- Port Placement Location (X-Y coordinates)
- I/O Bank Number
- I/O Standard
- Pin Assignment

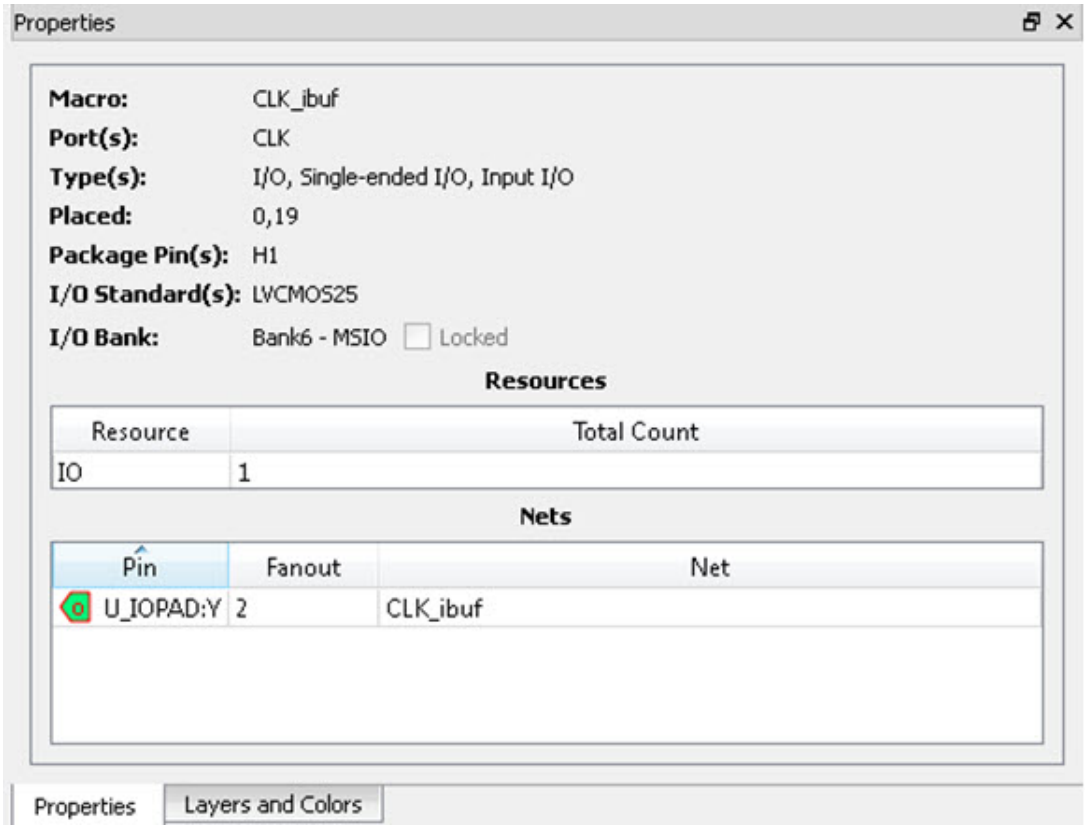


Figure 38 · Properties View of Port “CLK”

SmartTime Tutorials

Tutorial 1 - 32-Bit Shift Register with Clock Enable

This tutorial section describes how to enter a clock constraint for the 32-bit shift register on SmartFusion2 device. You will use the SmartTime Constraints Editor and perform post-layout timing analysis using the SmartTime Timing Analyzer.

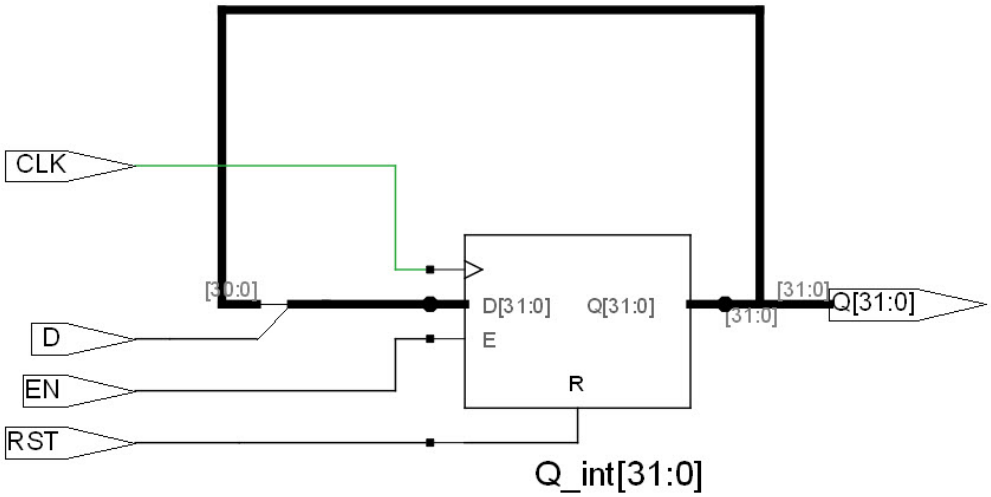


Figure 39 · 32-bit Shift Register

Use the links below to go directly to a topic:

- Add a Clock Constraint
- Run Place and Route
- Maximum Delay Analysis with Timing Analyzer
- Minimum Delay Analysis with Timing Analyzer
- Changing Constraints and Observing Results

To set up your project:

1. Invoke Libero SoC. From the **Project** menu, choose **New Project**.
2. Enter **sf2_shift32** for your new project name and browse to a folder for your project location.
3. Select **Verilog** as the Preferred HDL Type.
4. Leave all other settings at the default values.

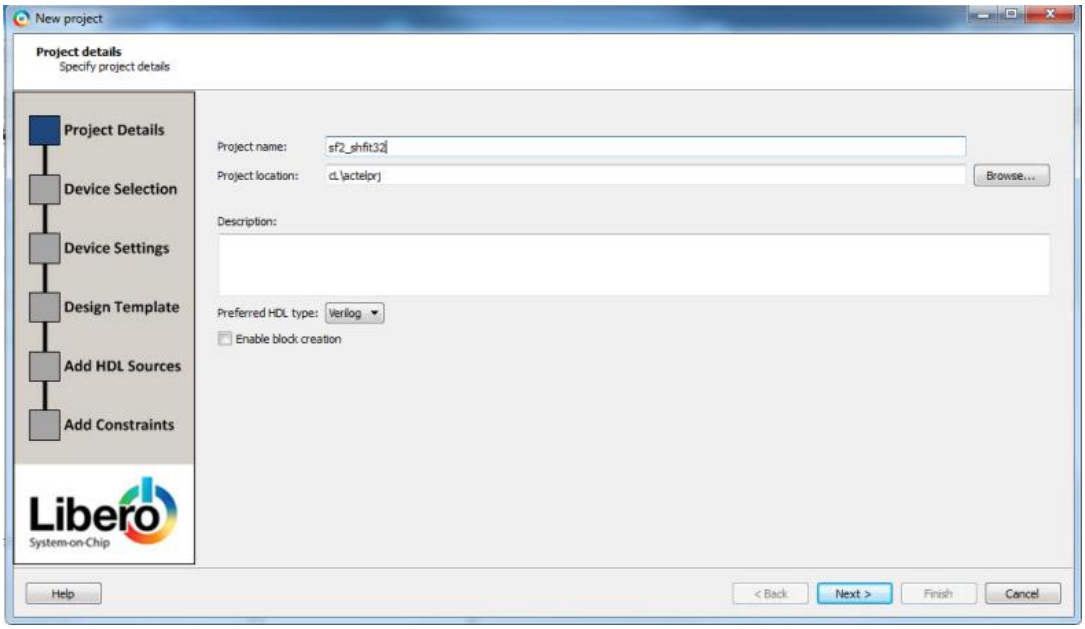
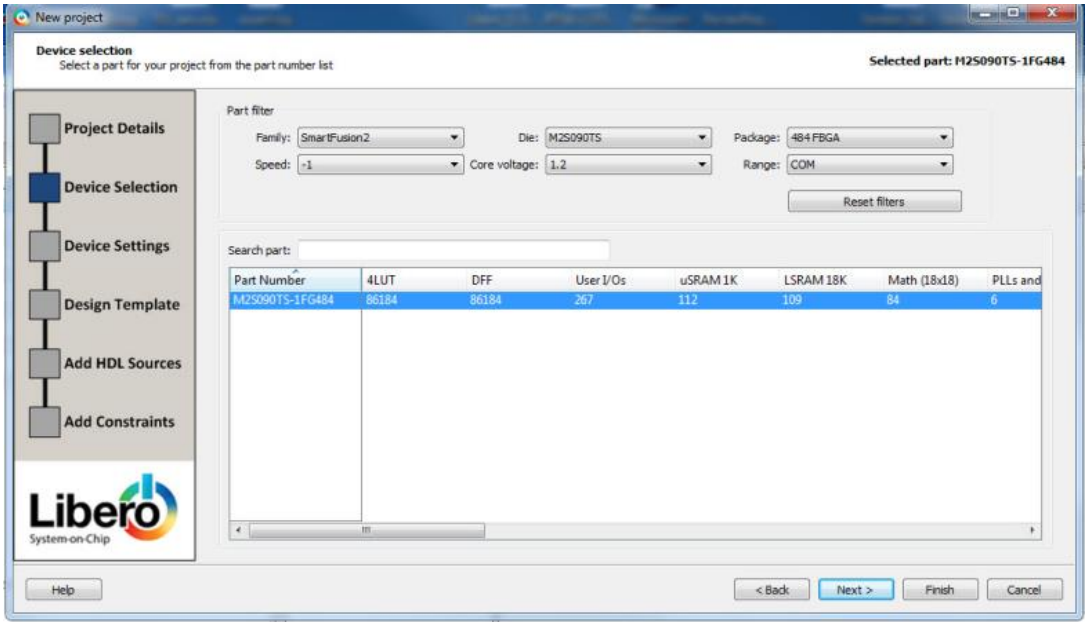


Figure 40 · New Project Creation - 32 Bit Shift Register

5. Click Next to go to Device Selection page. Make the following selection from the pull-down menu:
    - **Family**: SmartFusion2
    - **Die**: M2S090TS
    - **Package**: 484FBGA
    - **Speed**:STD
    - **Core Voltage**: 1.2 V
    - **Range**: COM
6. Click the M2S090TS-1FG484 part number and click **Next**.



7. Accept the default settings in the Device Settings page and click **Next**.
8. Accept the default settings in the Design Template page and click **Next**.
9. Click **Next** to go to the Add Constraints Page.

10. We are not adding any constraints. Click **Finish** to exit the New Project Creation wizard.
11. To add a new HDL file, select **File> New> HDL**. The Create a new HDL file dialog box opens. Name the HDL file as **shift_reg32** as shown below and click **OK**.

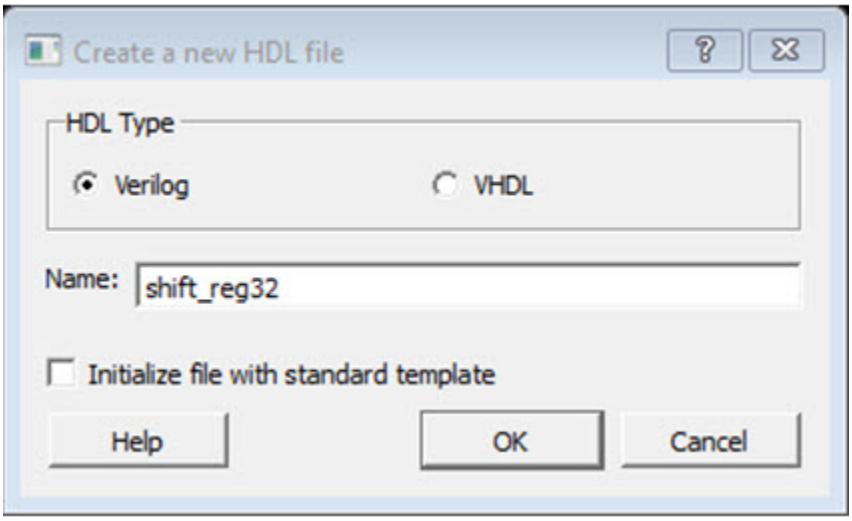


Figure 41 · Create a new HDL file Dialog Box

12. Copy and paste the code shown below into the Verilog file:

```
module shift32 ( Q,CLK,D,EN,RESET);
input D,EN,CLK,RESET;
output[31:0] Q;
reg [31:0] Q_int;
assign Q=Q_int;
always@ (posedge CLK)
begin
if(RESET)
Q_int<=0;
else begin
if(EN)
Q_int<={Q_int[30:0],D};
end
end
endmodule
```

13. Check the HDL file to confirm that there are no syntax errors.
14. Confirm that the shift_reg32 design appears in the Design Hierarchy window, as shown in the figure below.

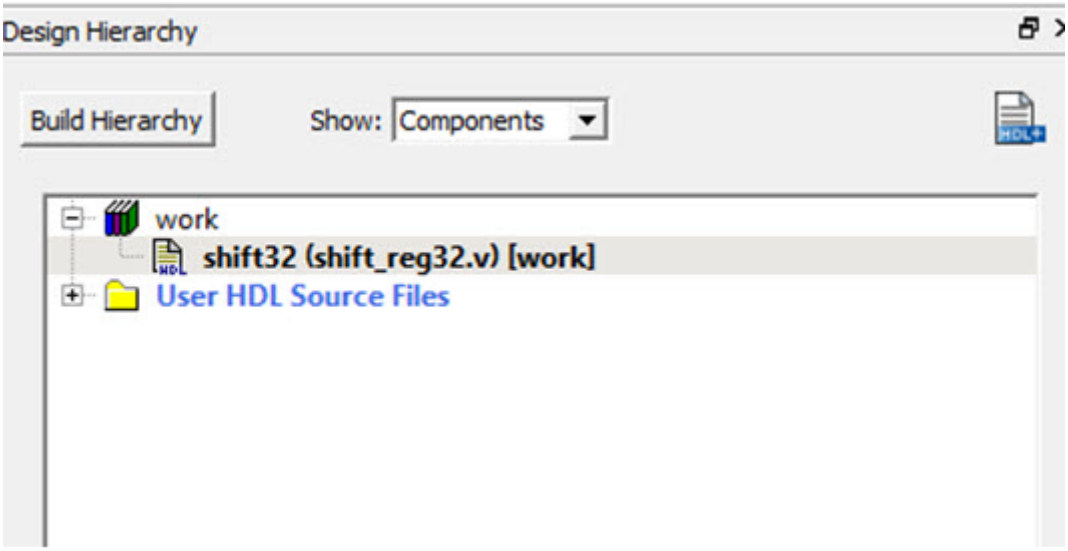


Figure 42 · shift_reg32 in the Design Hierarchy Window

15. In the Design Flow window, double-click **Synthesize** to run Synplify Pro with default settings. A green check mark appears next to Synthesize when Synthesis is successful (as shown in the figure below).

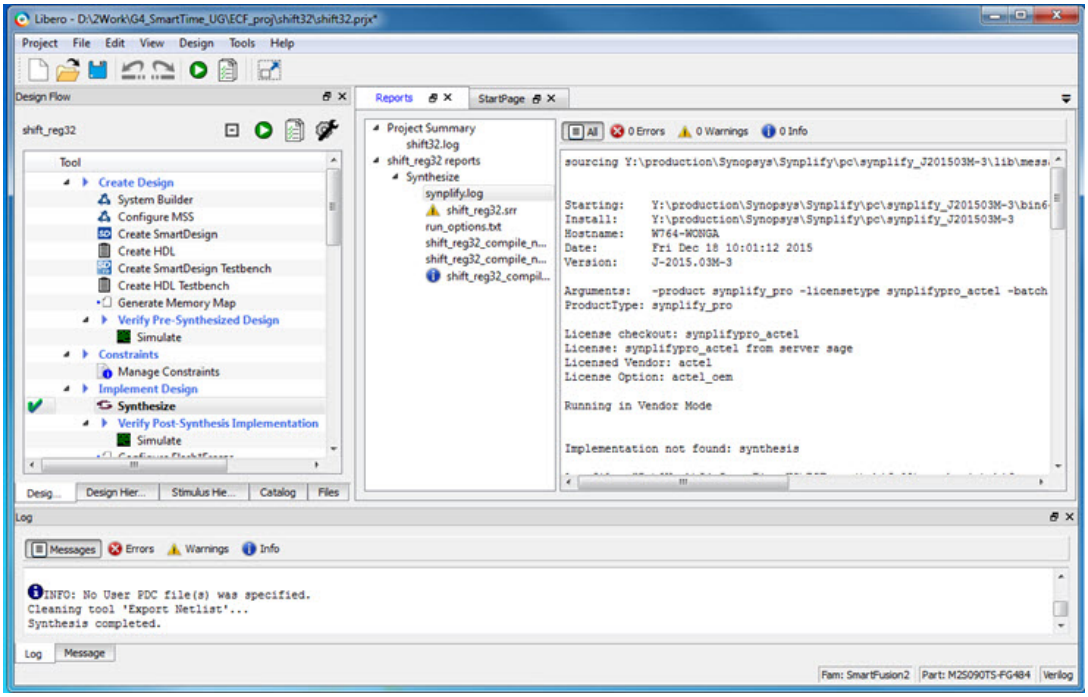


Figure 43 · Synthesis and Compile Complete - 32-Bit Shift Register with Clock Enable

Add a Clock Constraint - 32 Bit Shift Register

To add a clock constraint to your design:

1. In the Design Flow window, double-click **Manage Constraints**. The Constraint Manager appears (as shown in the figure below.)

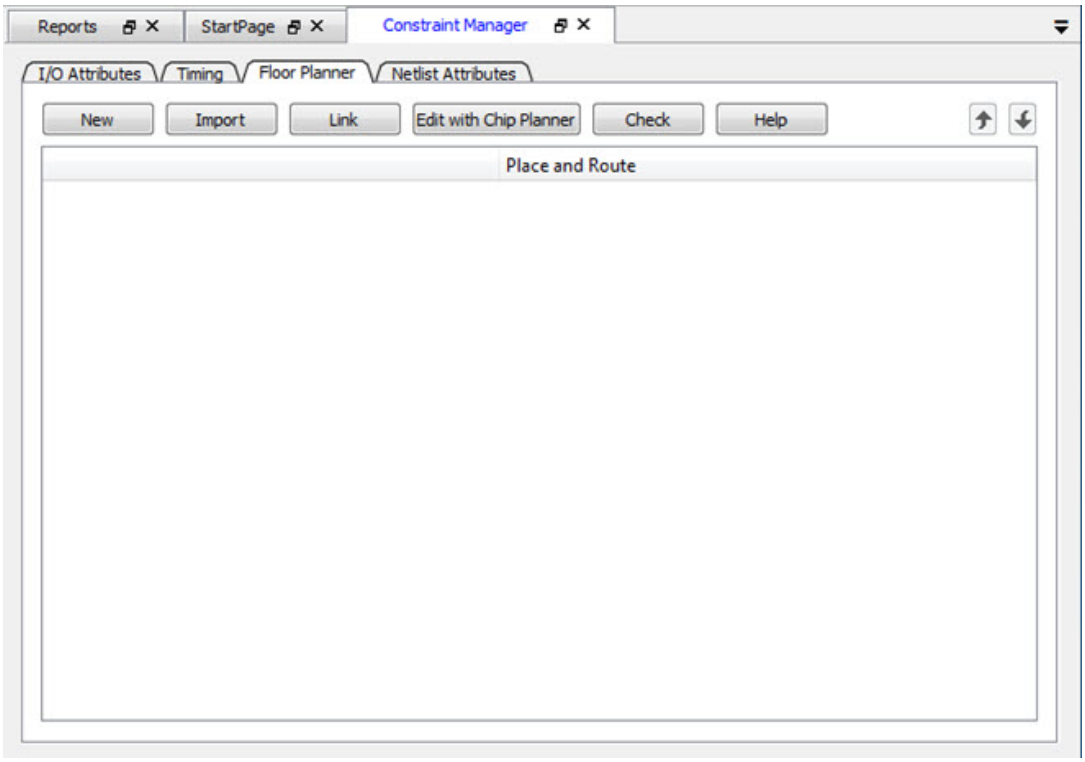


Figure 44 · Constraint Manager

2. Click the **Timing** tab.
3. Click **Edit with Constraints Editor > Edit Place and Route Constraints**. The Constraints Editor appears.

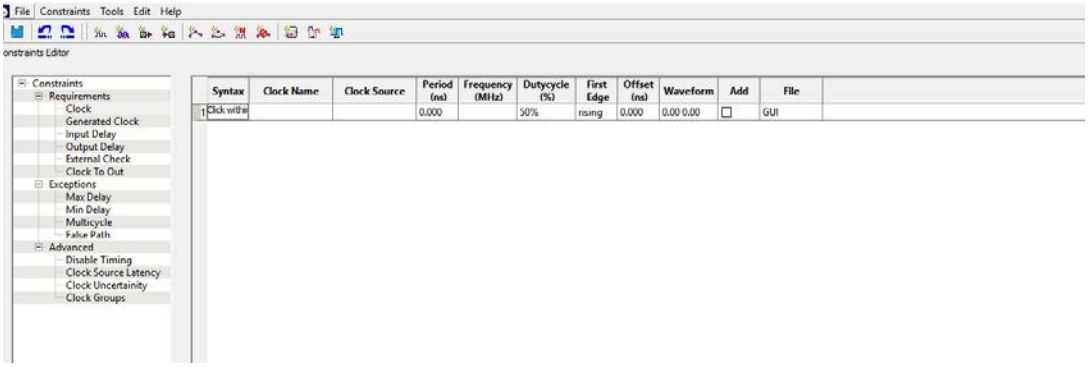


Figure 45 · Constraints Editor – Add clock constraint

4. In the Constraints Editor, right-click **Clock** under Requirement and select **Add Clock Constraint**.

   The Create Clock Constraint Dialog Box appears.

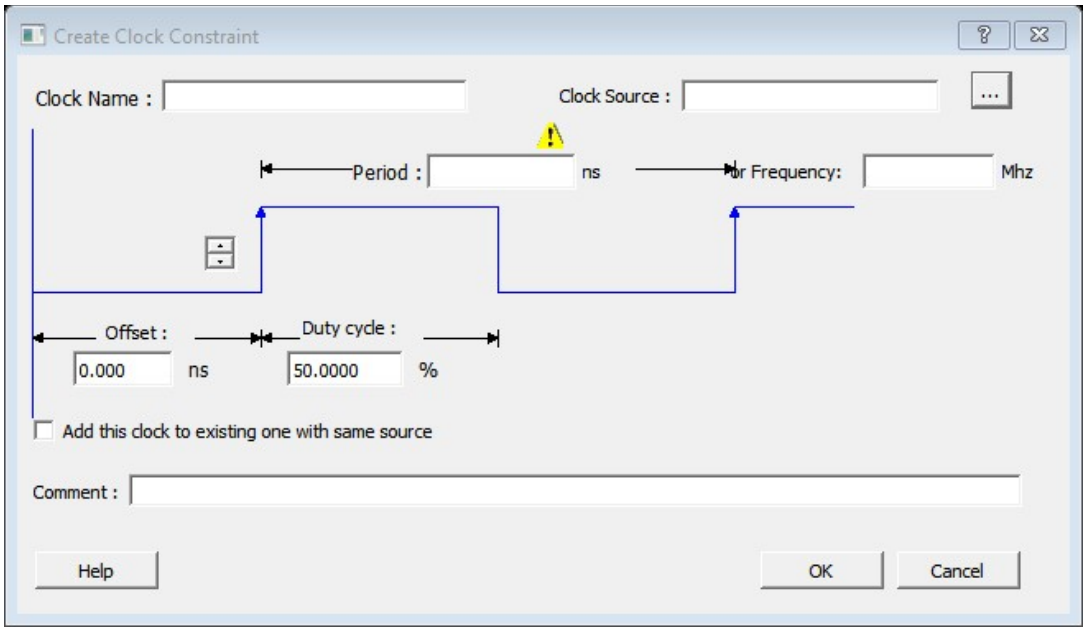


Figure 46 · Create Clock Constraint Dialog Box

5. From the **Clock Source** drop-down menu, choose the **CLK** pin.
6. Enter **my_clk** in the Clock Name field.
7. Set the Frequency to 250 MHz (as shown in the figure below) and leave all other values at the default settings. Click **OK** to continue.

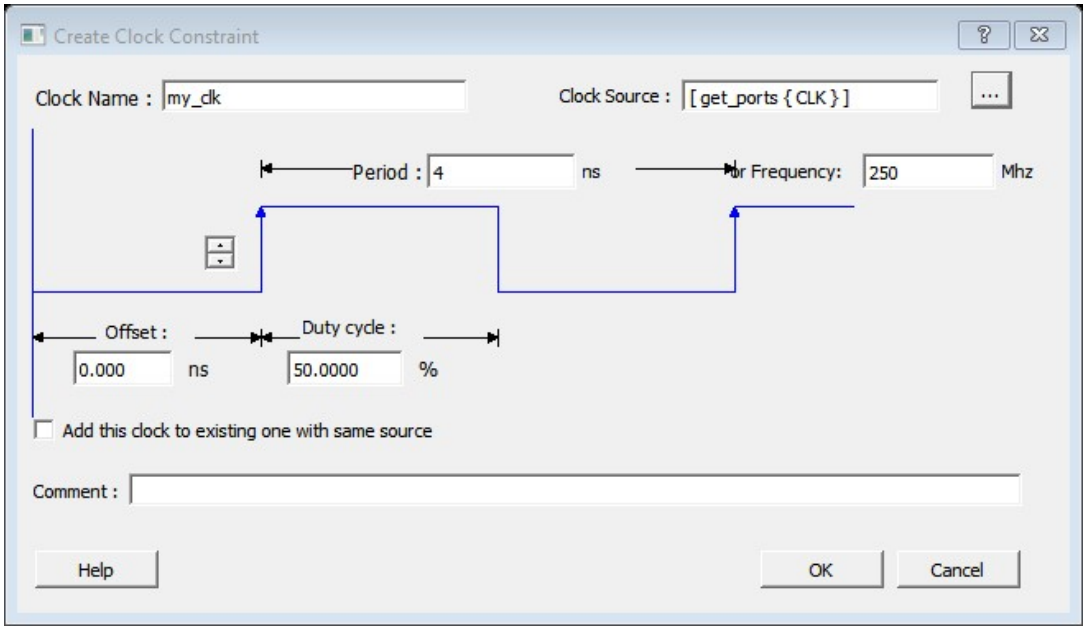


Figure 47 · Add a 250 MHz Clock Constraint

The clock constraint appears in the SmartTime Constraints Editor (as shown in the figure below).

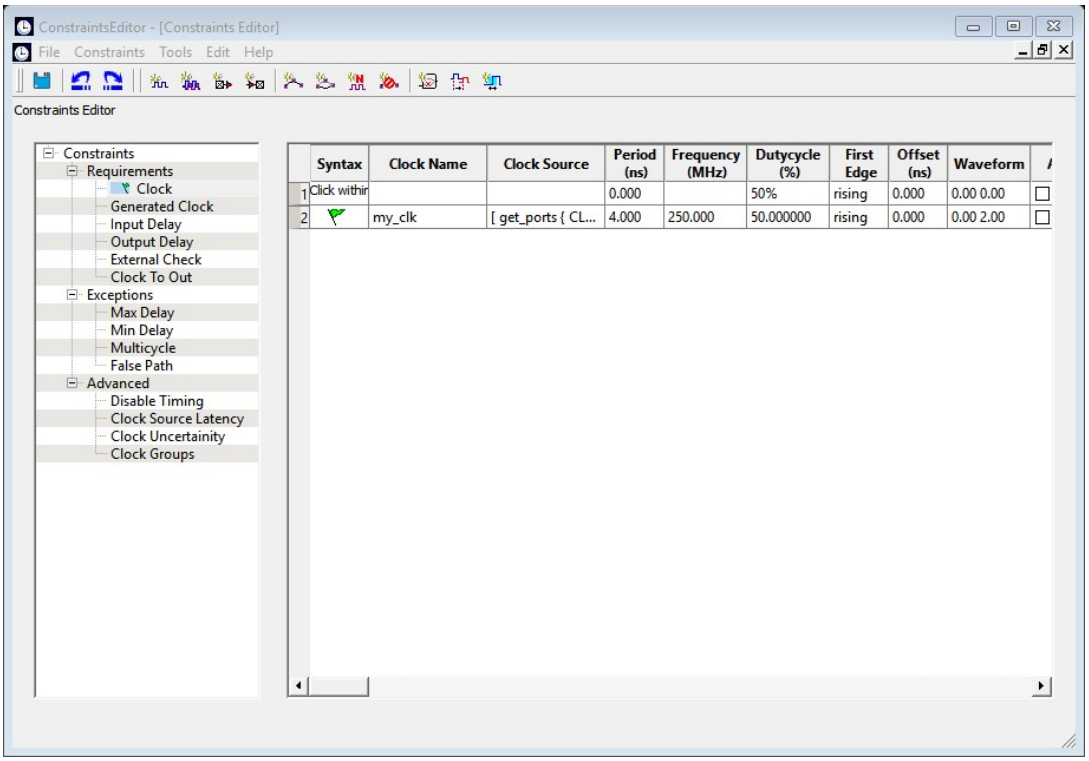


Figure 48 · 250 MHz Clock Constraint in the Constraint Editor

8. From the **File** menu, choose **Save** to save the constraints.
9. From the SmartTime **File** menu, choose **Exit** to exit SmartTime. Libero creates a constraint file to store the clock constraint. This file is listed and displayed in the Constraint Manager. It is named user.sdc and is designated as Target.

   Note: A target file is used to store newly added constraints from the Constraint Editor. When the Constraint Editor is invoked and no SDC timing constraint file is present, Libero SoC creates the user.sdc file (and marks it as target) to store the timing constraints you create in the Constraint Editor.
10. In the Constraint Manager, check the checkbox under Place and Route and the checkbox under Timing Verification to associate the constraint file to the tools. The constraint file is used for both Place and Route and Timing Verification.

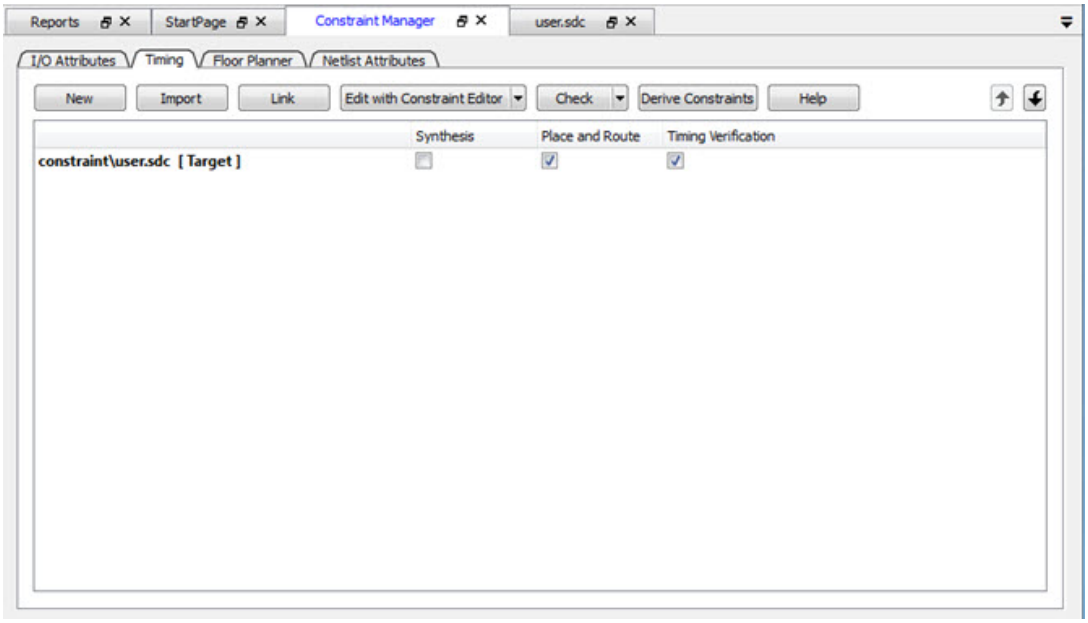


Figure 49 · SDC Constraint File and Tool Association

Run Place and Route

1. Right-click **Place and Route** and choose **Configure Options**.
2. Click the checkbox to enable Timing-Driven layout in Layout Options and leave the other values at the default settings (as shown in the figure below). Click **OK** to continue.

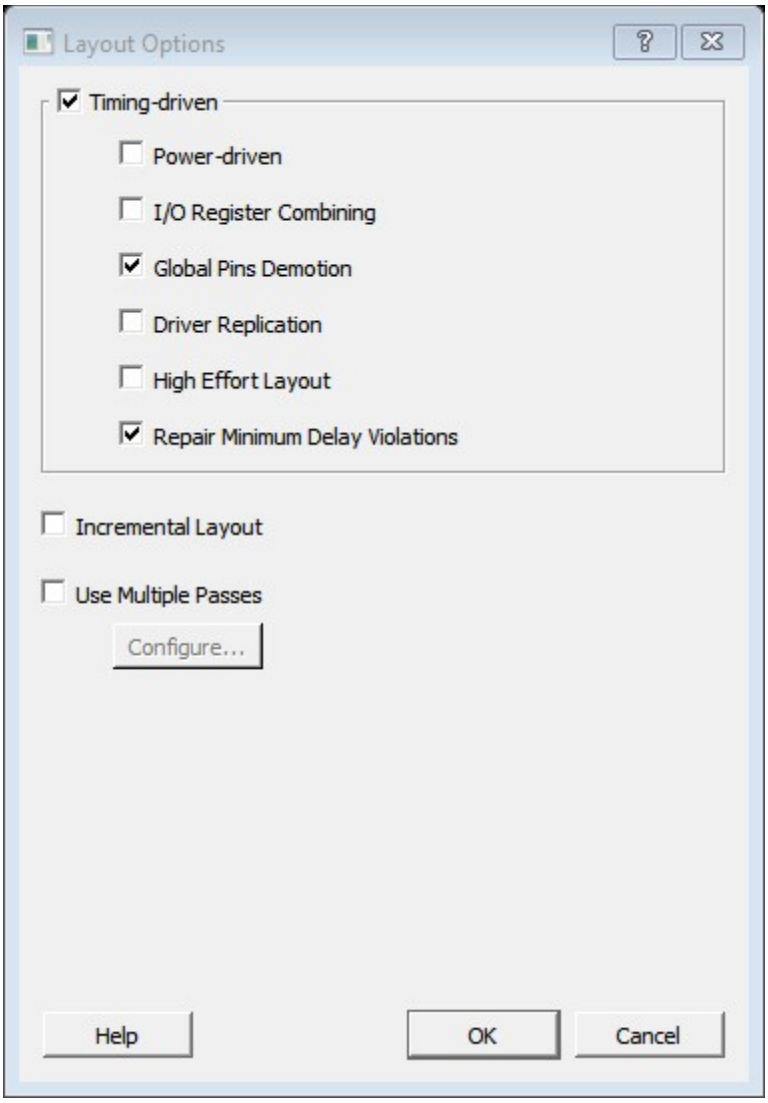


Figure 50 · Layout Options Dialog Box

3. Double-click **Place and Route** inside the Design Flow window to start the Place and Route.

A green check mark appears next to Place and Route after successful completion of Place and Route.

Maximum Delay Analysis with Timing Analyzer- 32-Bit Shift Register Example

The SmartTime Maximum Delay Analysis window displays the design maximum operating frequency and lists any setup violations.

To perform Maximum Delay Analysis:

1. Right-click **Open SmartTime** in the Design Flow window and choose **Open Interactively** to open SmartTime. The Maximum Delay analysis window appears. A green check next to the clock name indicates there are no timing violations for that clock domain. The Summary page displays a summary of the clock domain timing performance.

   The Maximum Delay Analysis Summary displays:

   - Maximum operating frequency for the design
   - External setup and hold requirements

- Maximum and minimum clock-to-out times. In this example, the maximum clock frequency for CLK is 609.75 MHz.

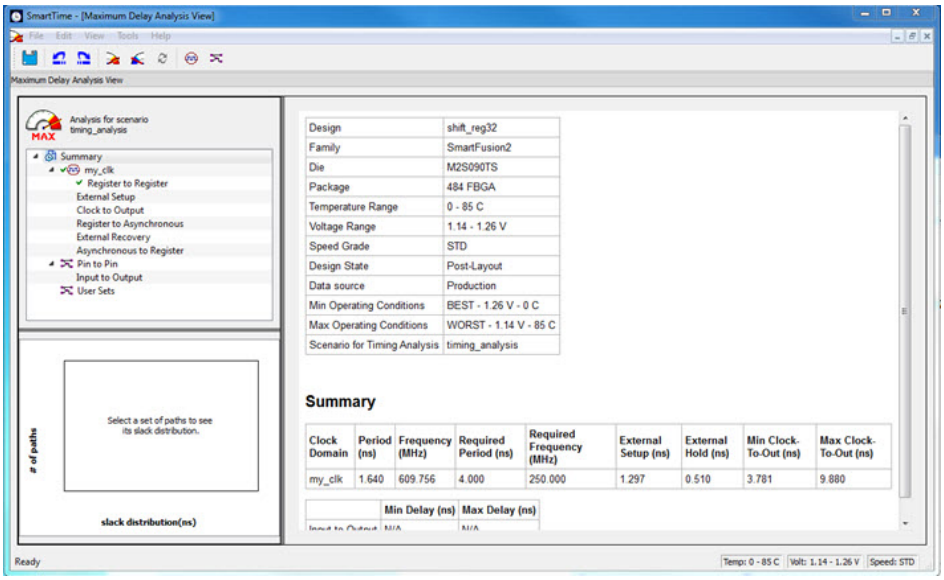


Figure 51 · Maximum Delay Analysis - Summary

2. Expand **my_clk** to display the Register to Register, External Setup and Clock to Output path sets.
3. Select **Register to Register** to display the register-to-register paths. The window displays a list of register-to-register paths and detailed timing analysis for the selected path (as shown in the figure below). Note that all the slack values are positive, indicating that there are no setup time violations

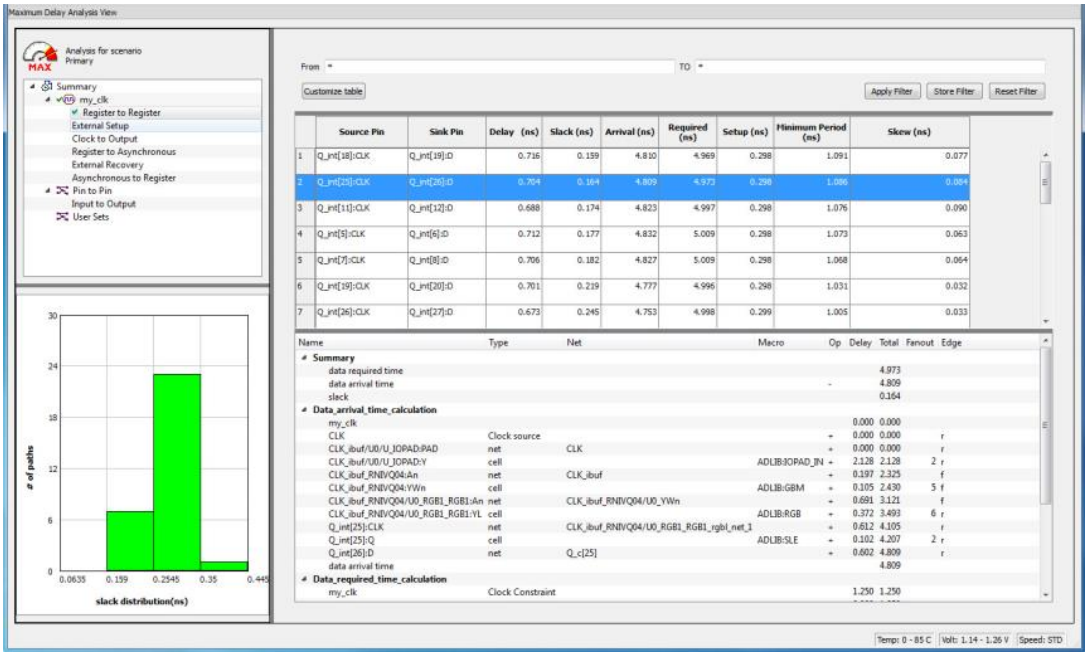


Figure 52 · SmartTime Register to Register Delay

4. Double-click a path row to open the Expanded Path window. The window shows a calculation of the data arrival and required times along with a schematic of the path (as shown in the figure below).

Note: The Timing Numbers in these reports may vary slightly with different versions of the Libero Software, and may not be exactly the same as what you will see when you run the tutorial.

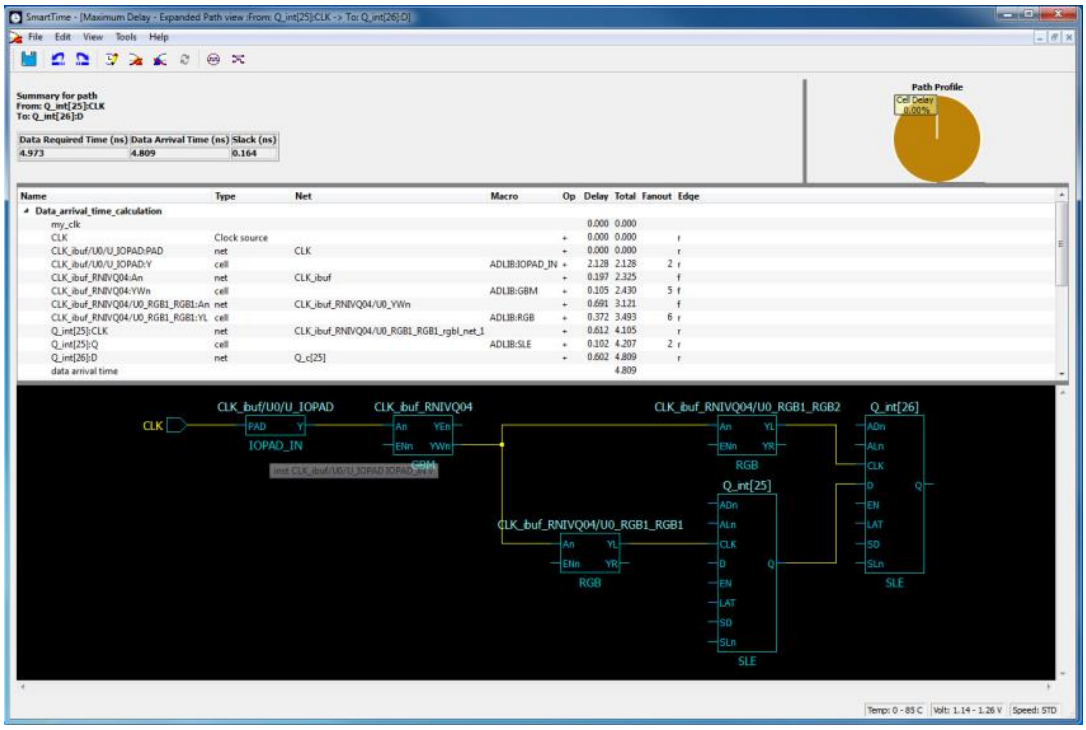


Figure 53 · Register-to-Register Expanded Path View

5. Select **External Setup** to display the Input to Register timing. Select **Path 3**. The Input Arrival time from the EN pin to Q_int[27]:EN is 4.547 ns (as shown in the figure below).

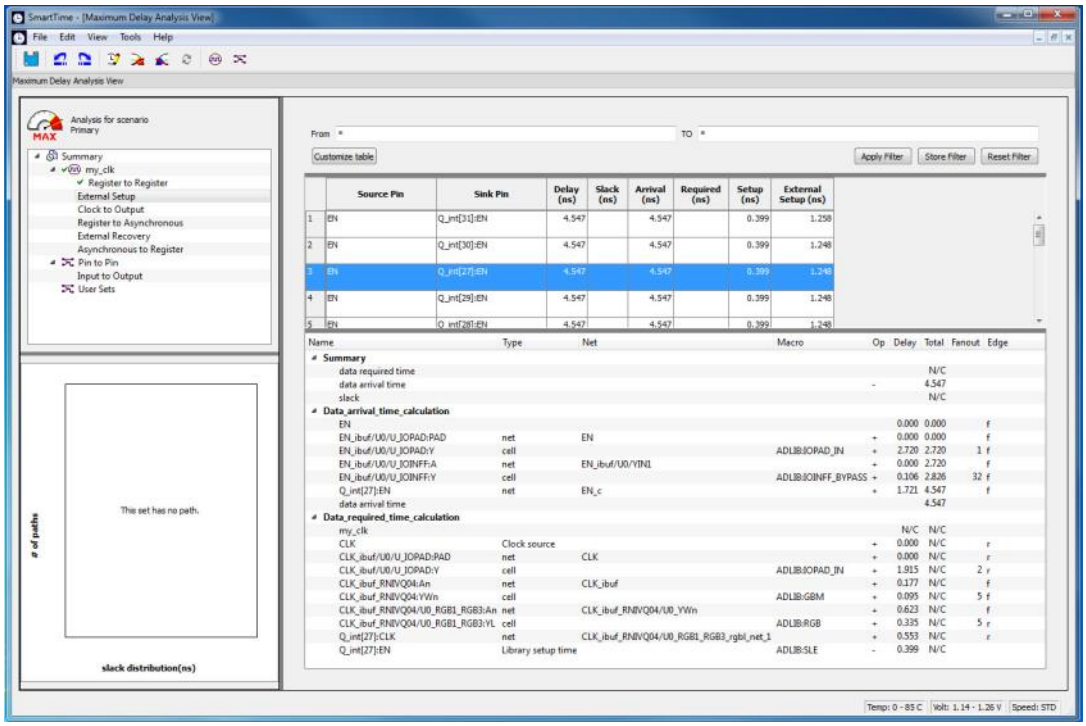


Figure 54 · SmartTime - Input to Register Path Analysis

6. Select **Clock to Output** to display the register to output timing. Select Path 1. The maximum clock to output time from Q_int[16]:CLK to Q[16] is 9.486ns .

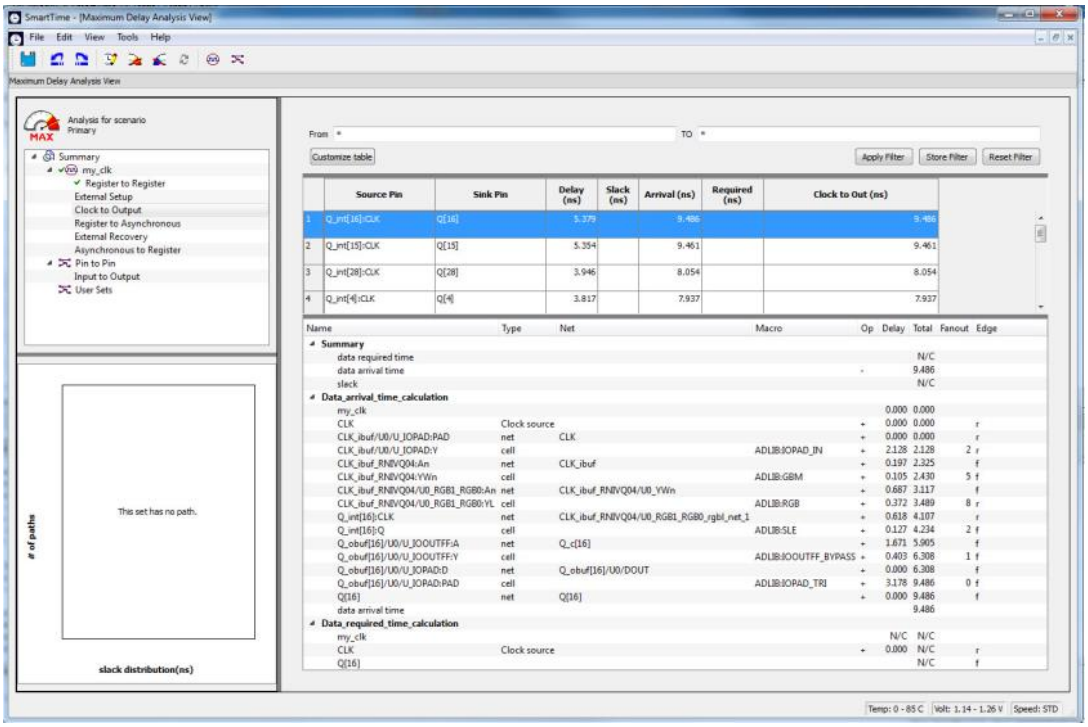


Figure 55 · SmartTime Clock to Output Path Analysis

Minimum Delay Analysis with Timing Analyzer - 32-Bit Shift Register Example

The SmartTime Minimum Delay Analysis window identifies any hold violations that exist in the design.

To perform Minimum Delay Analysis:

1. From the SmartTime Analysis window, choose **Tools > Minimum Delay Analysis**. The Minimum Delay Analysis View appears, as shown in the figure below.

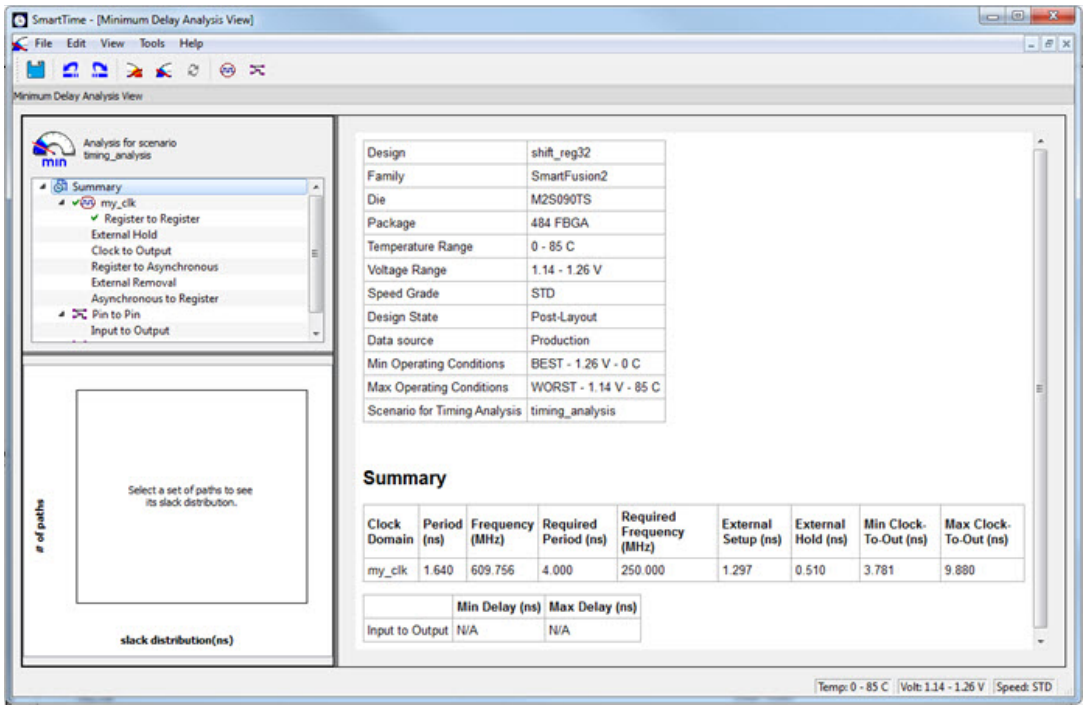


Figure 56 · SmartTime Minimum Delay Analysis View- Summary

2. Expand **my_clk** to display Register to Register, External Hold, Clock to Output, Register to Asynchronous, External Removal and Asynchronous to Register path sets.
3. Click **Register to Register** to display the reg to reg paths. The window displays a list of register to register paths and detailed timing analysis for the selected path. Note that all slack value are positive, indicating that there are no hold time violations.
4. Click to select the first path and observe the hold analysis calculation details, as shown in the figure below.

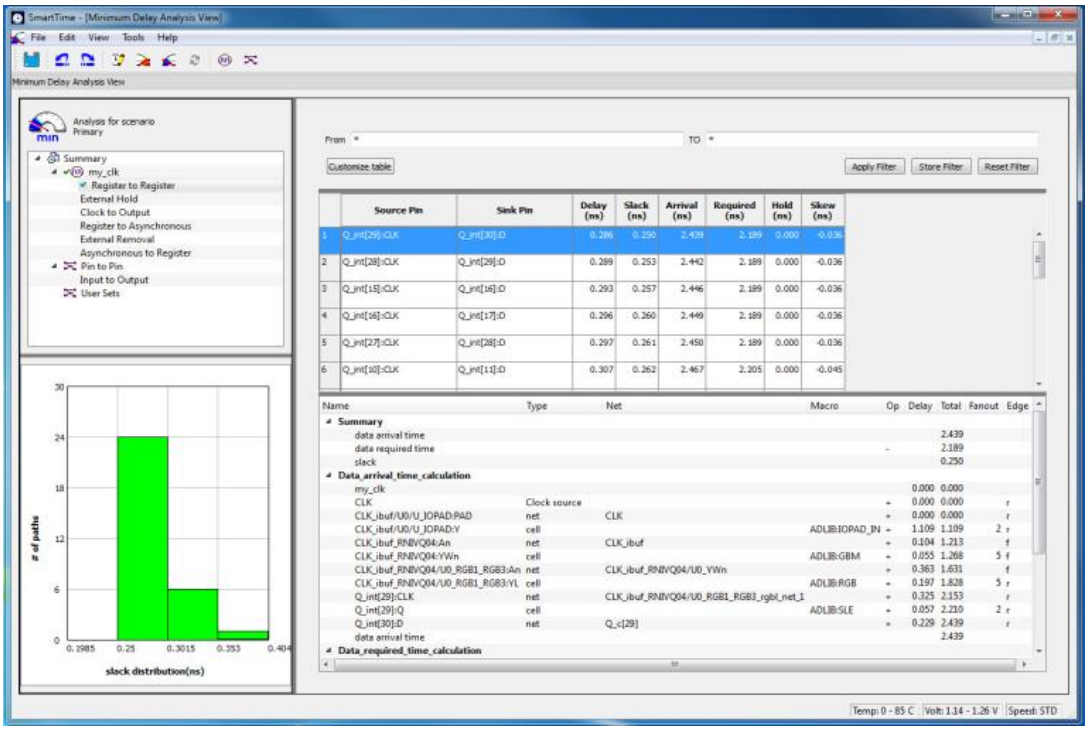


Figure 57 · SmartTime Minimum Delay Analysis

Changing Constraints and Observing Results - 32-Bit Shift Register Example

You can use the Constraints Editor to change your constraints and view the results in your design. To do so:

1. Open the Constraints Editor (**Constraints Manager > Timing Tab > Edit Constraints with Constraint Editor > Edit Timing Verifications Constraints**).

The Constraints Editor displays the clock constraint at 250 MHz that you entered earlier.

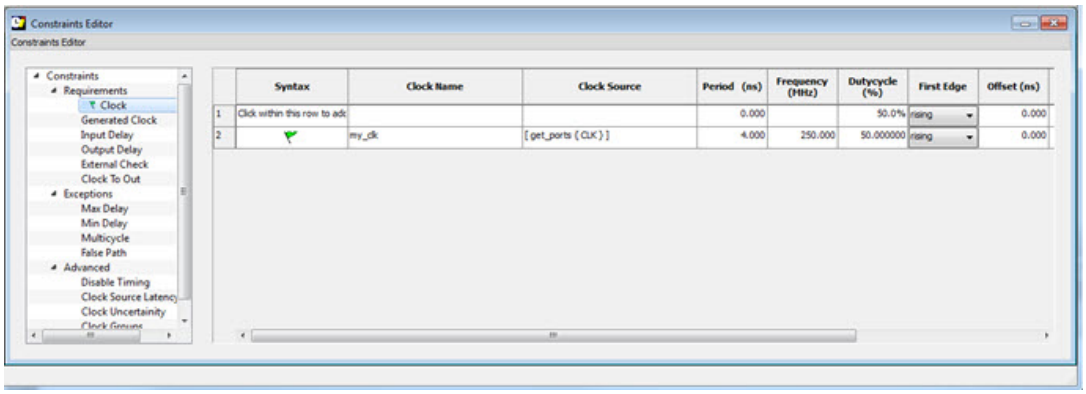


Figure 58 · Clock Constraint Set to 250 MHz

2. Select the second row. Right click and choose **Edit Clock Constraint**. This opens the Edit Clock Constraint dialog box. Change the clock constraint from 250 MHz to **800** MHz and click the green check mark to continue.
3. Click **Open SmartTime > Open Interactively**.
4. Choose **Maximum Delay Analysis View** to view the max delay analysis.
5. Expand **my_clk** in the Maximum Delay Analysis window. Click **Register to Register** to observe the timing information. Note that the slacks decrease after you increase the frequency. You may see the slacks go negative indicating Timing Violations. Negative slacks are shown in red.

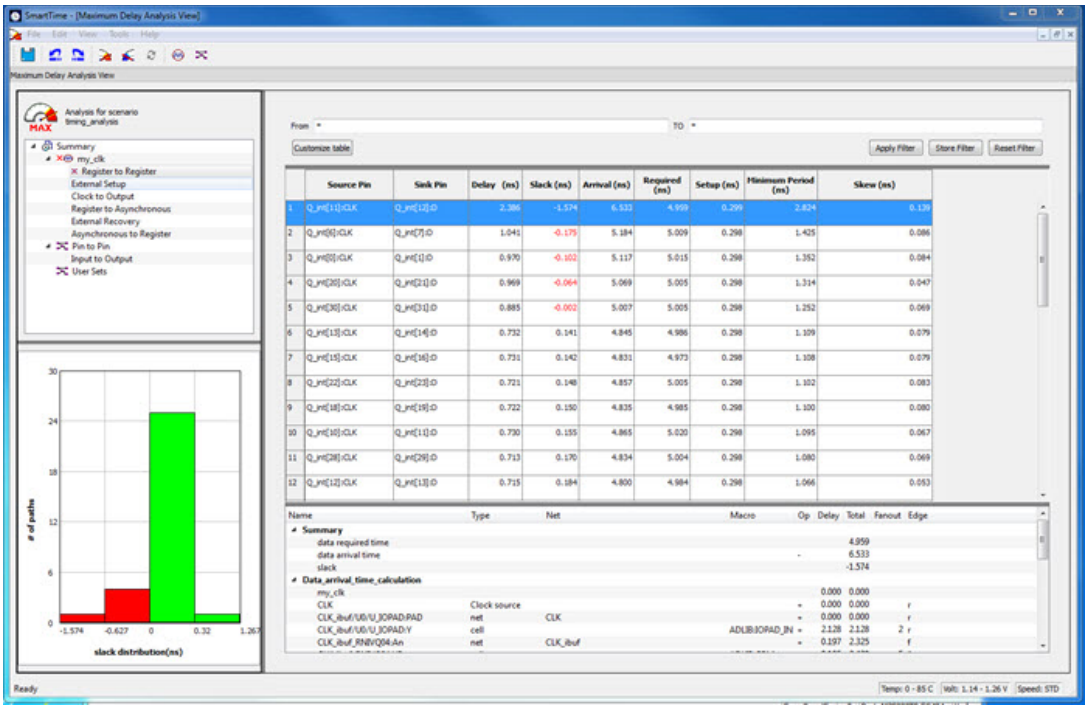


Figure 59 · Maximum Delay Analysis After Setting Clock Constraint to 800 MHz

Note: The actual timing numbers you see may be slightly different.

6. Close SmartTime. Click **No** when prompted to save changes.

Tutorial 2 - False Path Constraints

This section describes how to enter false path constraints in SmartTime. You will import an RTL source file from the design shown below. After routing the design, you will analyze the timing, set false path constraints, and observe the maximum operating frequency in the SmartTime Timing Analysis window.

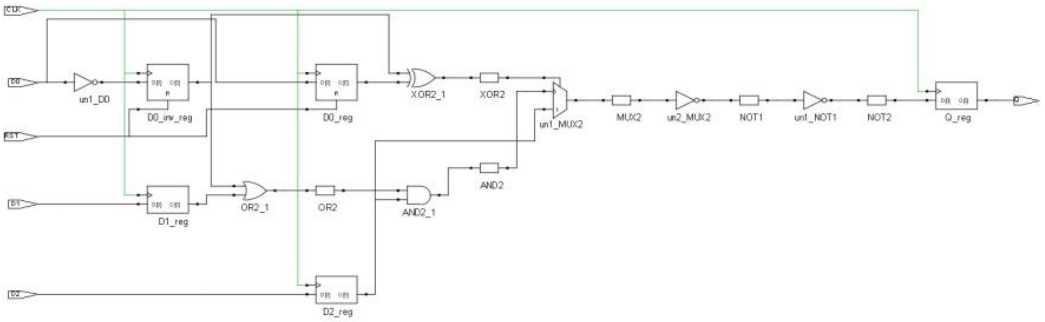


Figure 60 · Example Design with False Paths

Set Up Your False Path Example Design Project

1. Open Libero and create a new project (from the **Project** menu, choose **New Project**).
2. Name the project **false_path** and set the project location according to your preferences. Click **Next**. Enter the following values for your Device Selection settings:
    - **Family**: SmartFusion2
    - **Die**: M2S050
    - **Package**: 484 FBGA

- **Speed**: STD
- **Die Voltage**: 1.2 V
- **Range**: COM

3. Click **Finish** to create the new project.

Import the false_path Verilog File and Add Constraints

You must import the false_path.v Verilog source file into your design for this tutorial.

Then run Libero SoC.

To import the Verilog Source File:

1. From the **File** menu, choose **Import > HDL Source Files**.
2. Browse to the location of the false_path.v you saved and select it. Click **Open** to import the file.
3. Verify that the file appears in Design Hierarchy
4. In the Design Flow window, double-click **Synthesize** to run synthesis. A green check mark appears when the Synthesis step completes successfully.
5. Expand **Edit Constraints**. Right-click **Timing Constraints** and choose **Open Interactively**.
6. Double-click on **Manage Constraints**. Select the Timing tab, pull down the **Edit with Constraint Editor** sub-menu, and select the "Edit Place and Route Constraints". The Constraints Editor will open.
7. Double-click on the **Requirements**: **Clock** and the **Create Clock Constraint** dialog box will open.
8. Double click the browse button for Clock Source, and select CLK; name it clk (or whatever you want).
9. Set the frequency to be 100 MHz.

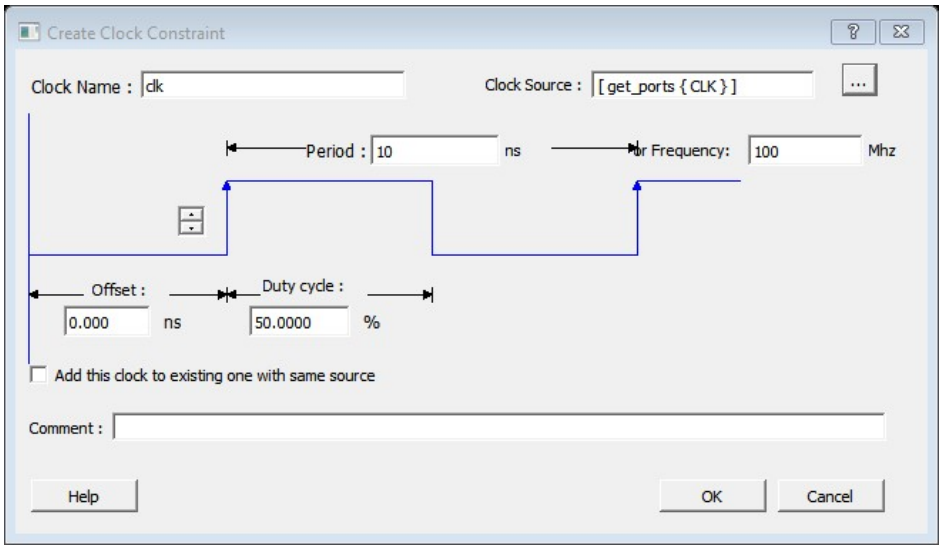


Figure 61 · Clock constraint of 100MHz

- Click OK to return to the Constraints Editor and observe that the clock information has been filled in as shown in the figure below.

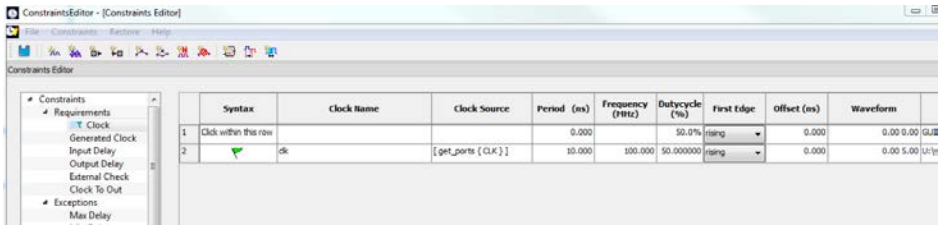


Figure 62 · Clock Constraint of 100 MHz in false_path design

10. Save your changes (**File > Save**) and close the Constraints Editor (**File > Close**).

11. In the Constraint Manager, check the checkbox under Place and Route and the checkbox under Timing Verification to associate the constraint file to both tools. The constraint file is used for both Place and Route and Timing Verification.

Place and Route Your FALSE_PATH Design

To run Place and Route on false_path design:

1. In Libero SoC, right-click **Place and Route** and choose **Configure Options**.

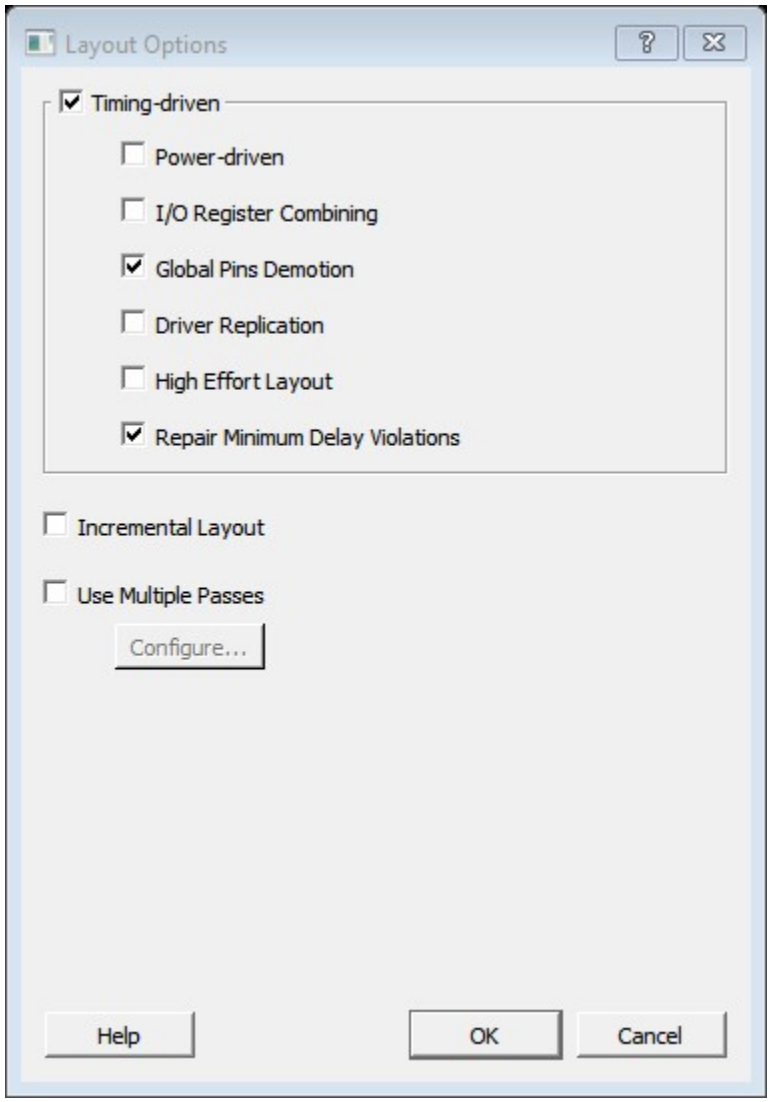


Figure 63 · Layout Options Dialog Box

2. Click the checkbox to enable Timing-Driven layout in Layout Options and leave the other values unchecked. Click **OK** to close the Layout Options dialog box.
3. Right-click **Place and Route** and choose **Run**.

A green check mark appears next to Place and Route in the Design Flow window when Place and Route completes successfully.

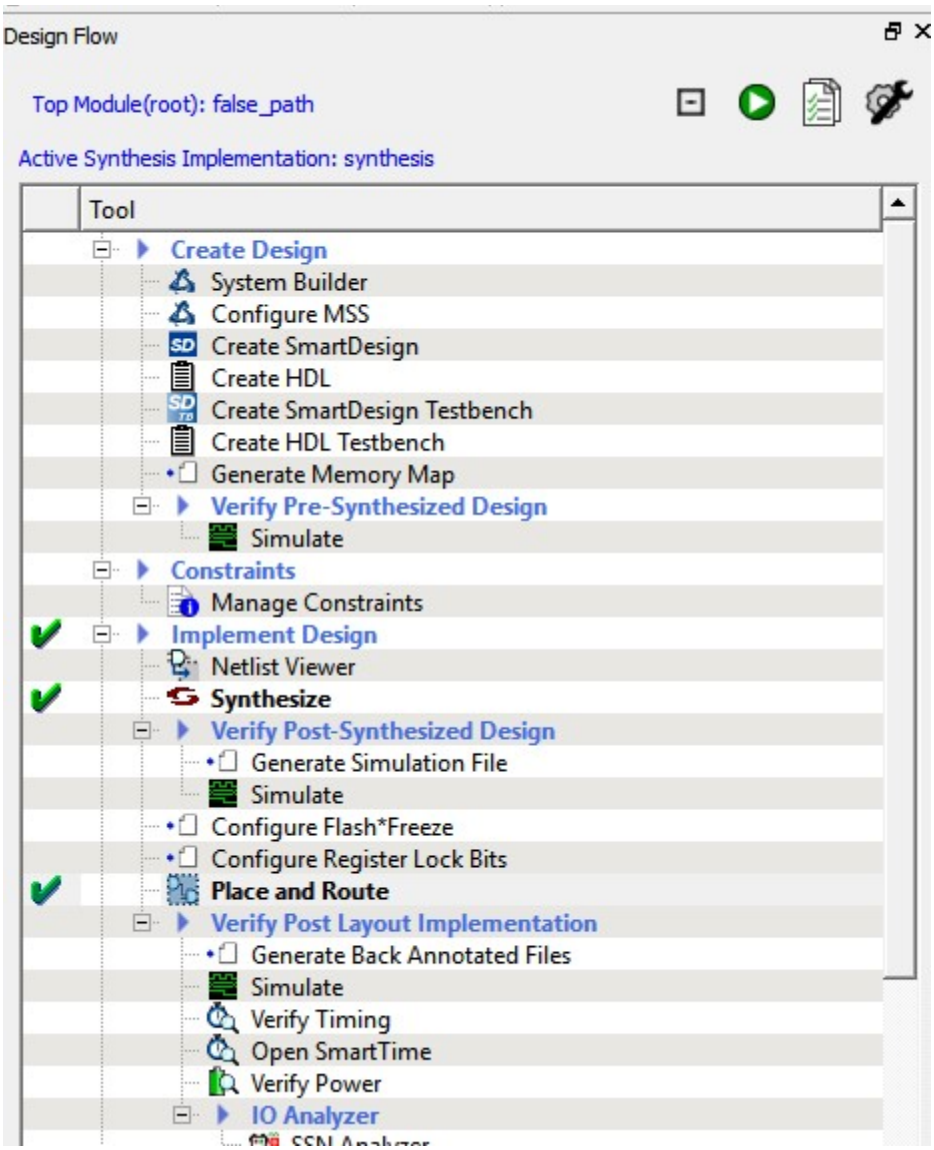


Figure 64 · Synthesize and Place and Route Successful Completion

Timing Analysis - Maximum Clock Frequency

The SmartTime Maximum Delay Analysis View displays the design maximum operating frequency and lists any setup violations.

To perform Maximum Delay Analysis:

1. Expand **Verify Post Layout Implementation**. Right-click **Open SmartTime** and choose **Open Interactively** to open SmartTime. The Maximum Delay Analysis View appears (as shown in the figure below). The Maximum Delay Analysis View displays a summary of design performance and indicates that the design will operate at a maximum frequency of 442.48 MHz.

   Note: You may see a slightly different maximum frequency with a different version of Libero SoC.

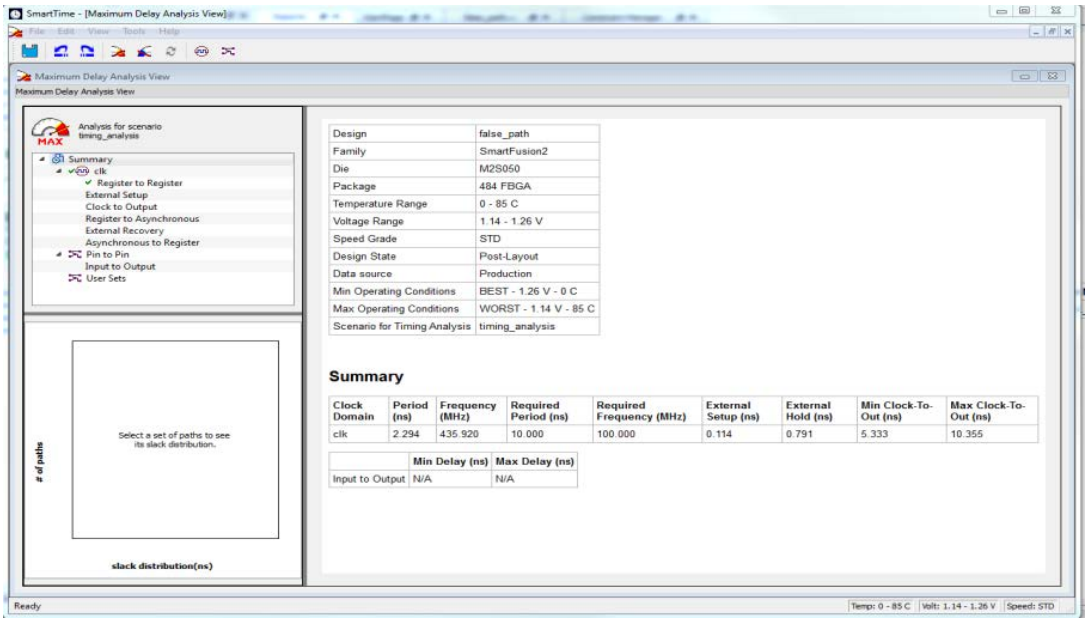


Figure 65 · Maximum Delay Analysis Summary

2. Expand **clk** to expand the display and show the Register to Register path sets.
3. Select **Register to Register** to display the register-to-register paths. Notice that the slack values are positive.
4. Double-click to select and expand the row in the path list with the path is from the CLK pin of flip-flop D0_reg to the D input of flip flop Q_reg. Note that the path goes through the S input of multiplexer un1_MUX2.

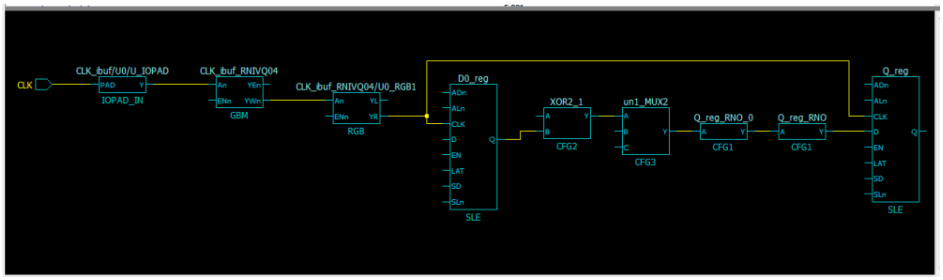


Figure 66 · Expanded Path

Looking at the code in false_path.v, we can see on lines 51 and 52, that D0_reg and D)_inv_reg are always the inverse of each other in "operational" mode (ie except for when RST is active). Line 56 says that XOR2 is the XOR of these two signals, and hence always 1 (again, except for when RST is active). And finally line 59 says that XOR2 is the select of MUX2.

We might reasonably decide that we are not interested in the reset mode delay for this design; and hence this path is a false path for our timing analysis purposes.

```
43      if (RST)
44      begin
45          D0_reg      <= 1'b0;
46          D0_inv_reg  <= 1'b0;
47      end
48
49      else
50      begin
51          D0_reg      <= D0;
52          D0_inv_reg  <= ~D0;
53      end
54  end
55
56  assign XOR2 = D0_reg ^ D0_inv_reg;
57  assign OR2  = D0_inv_reg || D1_reg;
58  assign AND2 = OR2 && D2_reg;
59  assign MUX2 = (XOR2) ? (D2_reg) : (AND2);
60
61
```

Figure 67 · Analyzing the false paths

Similar analysis shows that the path from D0_inv_reg:CLK to Q_reg:D shares exactly the same false-path characteristic. We should disable both paths.

5. Re-start the Libero Constraints Editor. The Constraints Editor must be running in order for us to use the back-annotation feature of StartTime. Go to the Constraint Manager tab, Timing sub-tab; and again pull down the "Edit with Constraint Editor" , and choose "Edit Timing Verification Constraints".
6. Leave this running and go back to SmartTime. From the **Tools** menu select **Max Delay Analysis**.
7. To set the path from D0_inv_reg:CLK to Q_reg :D as false, select the row containing this path in the Register to Register path set, right-click and choose **Add False Path Constraint** (as shown in the figure below). The Set False Path Constraint dialog box appears (it may pop-behind; check other Constraint Manager windows).

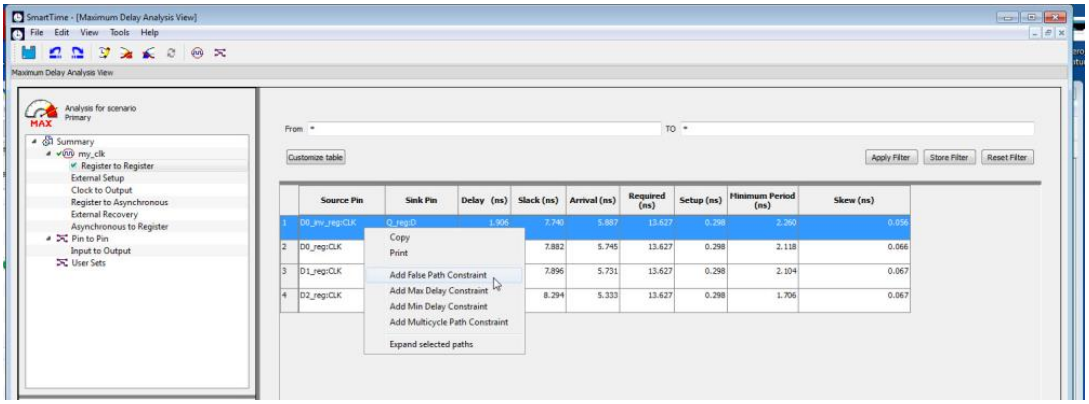


Figure 68 · Right-Click > Add False Path Constraint

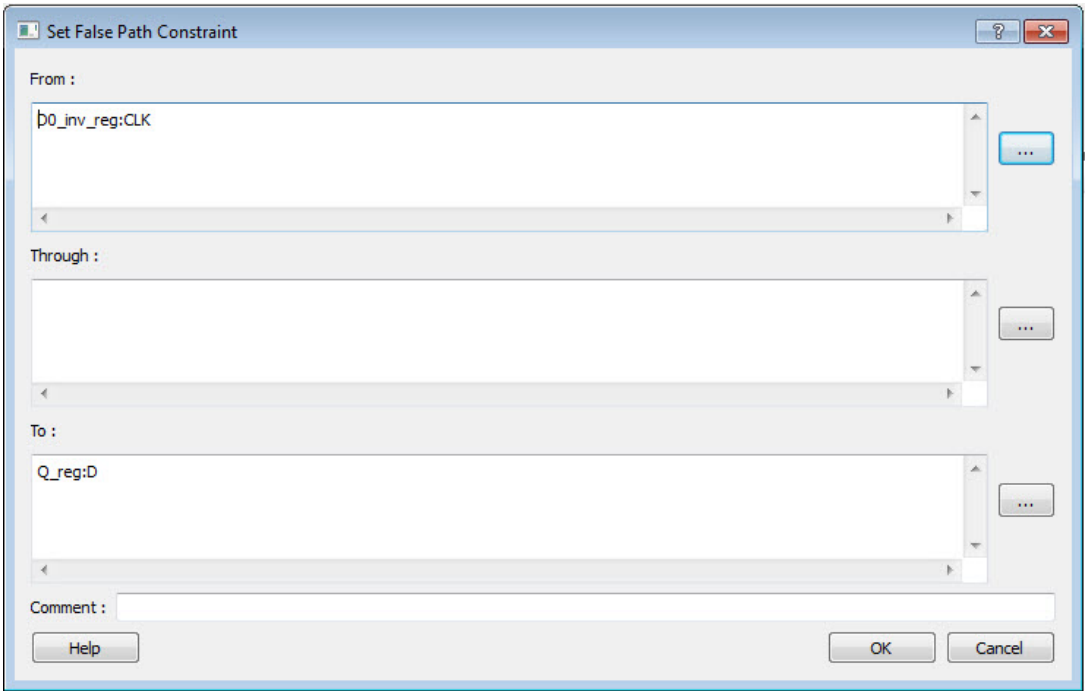


Figure 69 · Set False Path Constraint Dialog Box

8. **Click** OK to close the Set False Path Constraint dialog box.
9. Check the Constraints Editor window, there should now be an entry under **Exceptions** > **False Path**
10. Return to the SmartTime window and repeat for the D0_reg:CLK -> Q_reg:D path.
11. Since we are only interested in timing analysis through the MUX when select = 1, we can also ignore the MUX "0" path from D1_reg:D through the AND2. We make this a false path, also.
12. At this point the Constraints Editor should now look as follows. Save the file and exit the Constraints Editor and SmartTime.

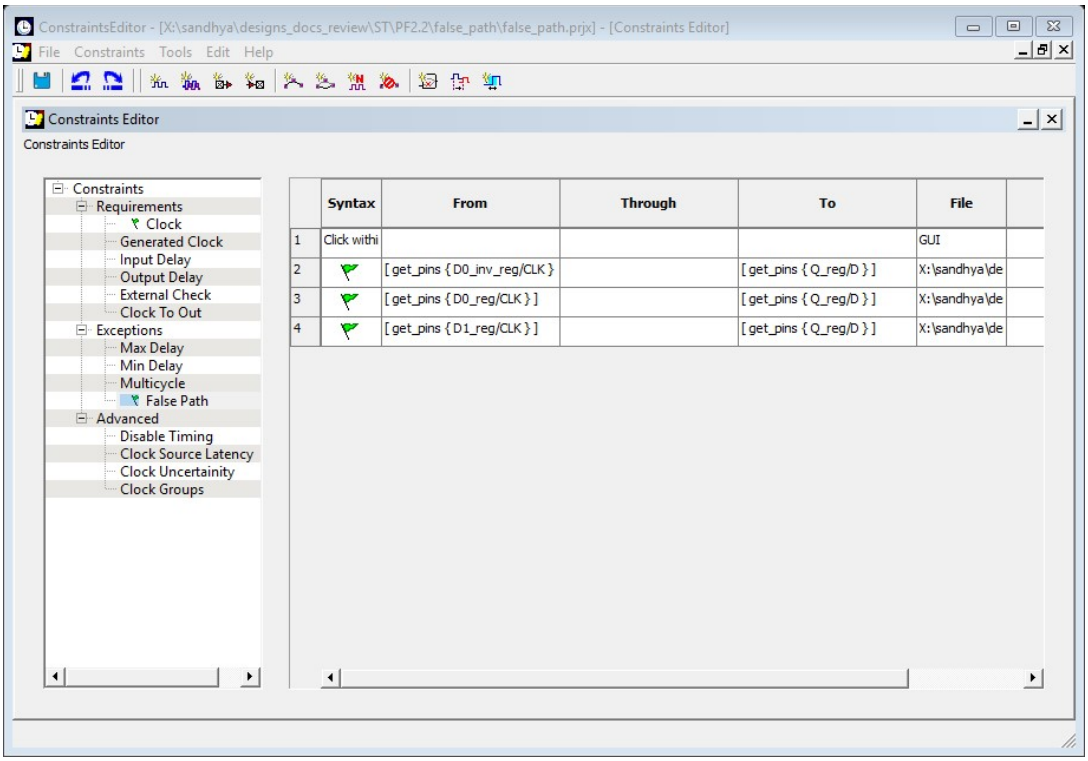


Figure 70 · False Path Constraints in the SmartTime Constraint Editor

13. Place and Route is now invalidated, and needs to be re-run before we can do timing analysis again. This is because we have changed the constraint file that we are using for both P&R and for Timing Analysis. It is possible to use different constraint files, in which case we would not need to re-run P&R.
14. Right-click on **Open SmartTime** and choose **Update and Open Interactively**. You will see that Place and Route is run automatically before SmartTime is re-started.
15. View the summary in the Maximum Delay Analysis View (**Tools > Max Delay Analysis**). Note that SmartTime now reports the maximum operating frequency as 586.17 MHz, as shown in the figure below.

Note: The maximum operating frequency may vary slightly with a different version of the Libero software.

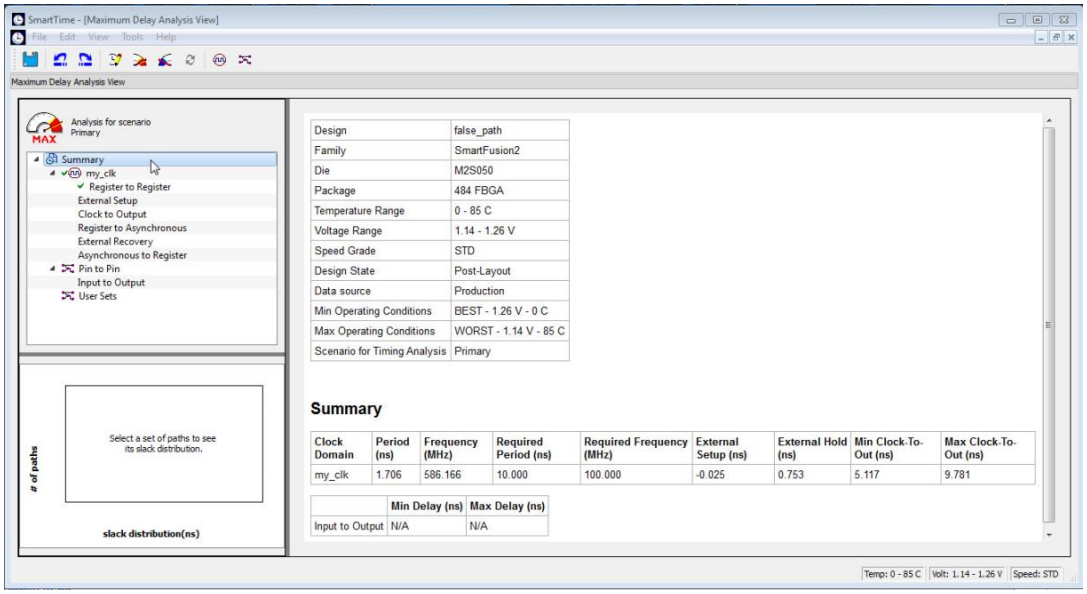


Figure 71 · Maximum Delay Analysis View - Summary

16. Select the Register to Register set for my_clk. Observe that only one path is visible, from D2_reg: CLK to Q_reg:D. This is the only path that propagates a signal (as shown in the figure below).

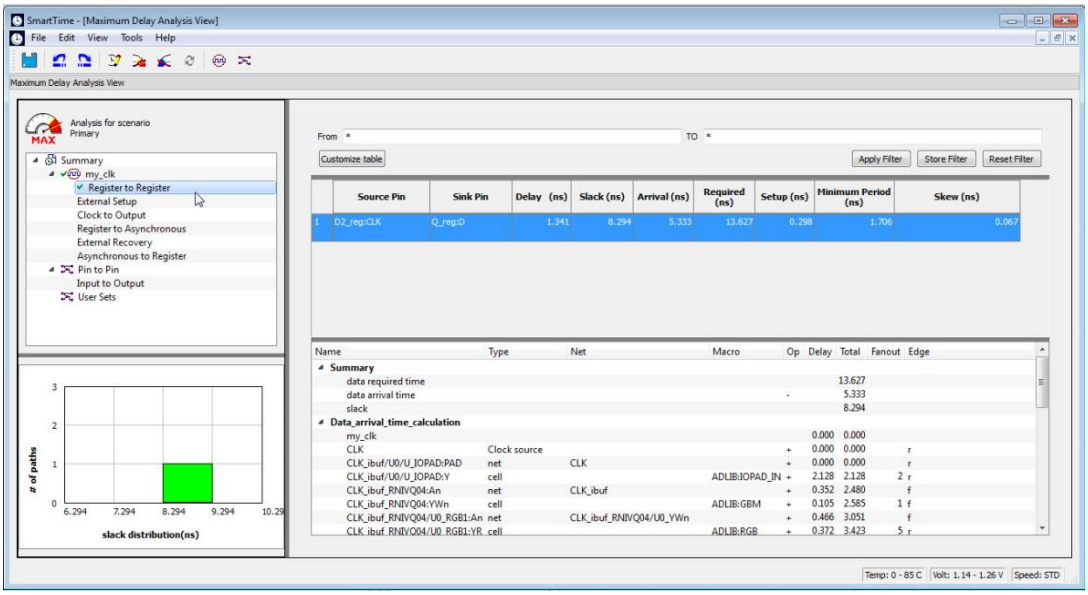


Figure 72 · Maximum Delay Analysis View - Register to Register

17. Close SmartTime.
18. Close Libero SoC.

false_path.v

```
//////////////////////////////////////////////////////////////
// Company: Microsemi Corp
//
// File history:
//      0.1 Initial Version
//
// Description:
// Simple example design to demonstrate use of timing
//   constraints.
//
// Targeted device: Family::SmartFusion2; Die::M2S050;
//   Package::484 FBGA;
//
// Author: Joe X
//
//////////////////////////////////////////////////////////////

module false_path (D0, D1, D2, RST, CLK, Q);

input   D0;
input   D1;
input   D2;
input   RST;
input   CLK;
output  Q;

reg     D0_reg;
```

```
reg     D0_inv_reg;
reg     D1_reg;
reg     D2_reg;

reg    Q_reg;

wire    XOR2 /*synthesis syn_keep=1*/;
wire    AND2 /*synthesis syn_keep=1*/;
wire    OR2  /*synthesis syn_keep=1*/;
wire    MUX2 /*synthesis syn_keep=1*/;
wire    NOT1 /*synthesis syn_keep=1*/;
wire    NOT2 /*synthesis syn_keep=1*/;

assign Q = Q_reg /*synthesis syn_keep=1*/;

always @(posedge CLK or posedge RST)
begin
    if (RST)
    begin
        D0_reg      <= 1'b0;
        D0_inv_reg  <= 1'b0;
    end

    else
    begin
        D0_reg      <= D0;
        D0_inv_reg  <= ~D0;
    end
end

assign XOR2 = D0_reg ^ D0_inv_reg;
assign OR2  = D0_inv_reg || D1_reg;
assign AND2 = OR2 && D2_reg;
assign MUX2 = (XOR2) ? (D2_reg) : (AND2);



always @(posedge CLK)
begin
    D1_reg      <= D1;
    D2_reg      <= D2;

    Q_reg <= NOT2;
end

not u1 (NOT1, MUX2);
not u2 (NOT2, NOT1);


endmodule
```

Dialog Boxes

Add Path Analysis Set Dialog Box

Use this dialog box to specify a custom path analysis set.

Note: The Analysis menu is available only in Maximum or Minimum Delay Analysis view.

To open the **Add Path Analysis Set** dialog box (shown below) from the SmartTime Timing Analyzer, choose any path and right click to select **Add Set**

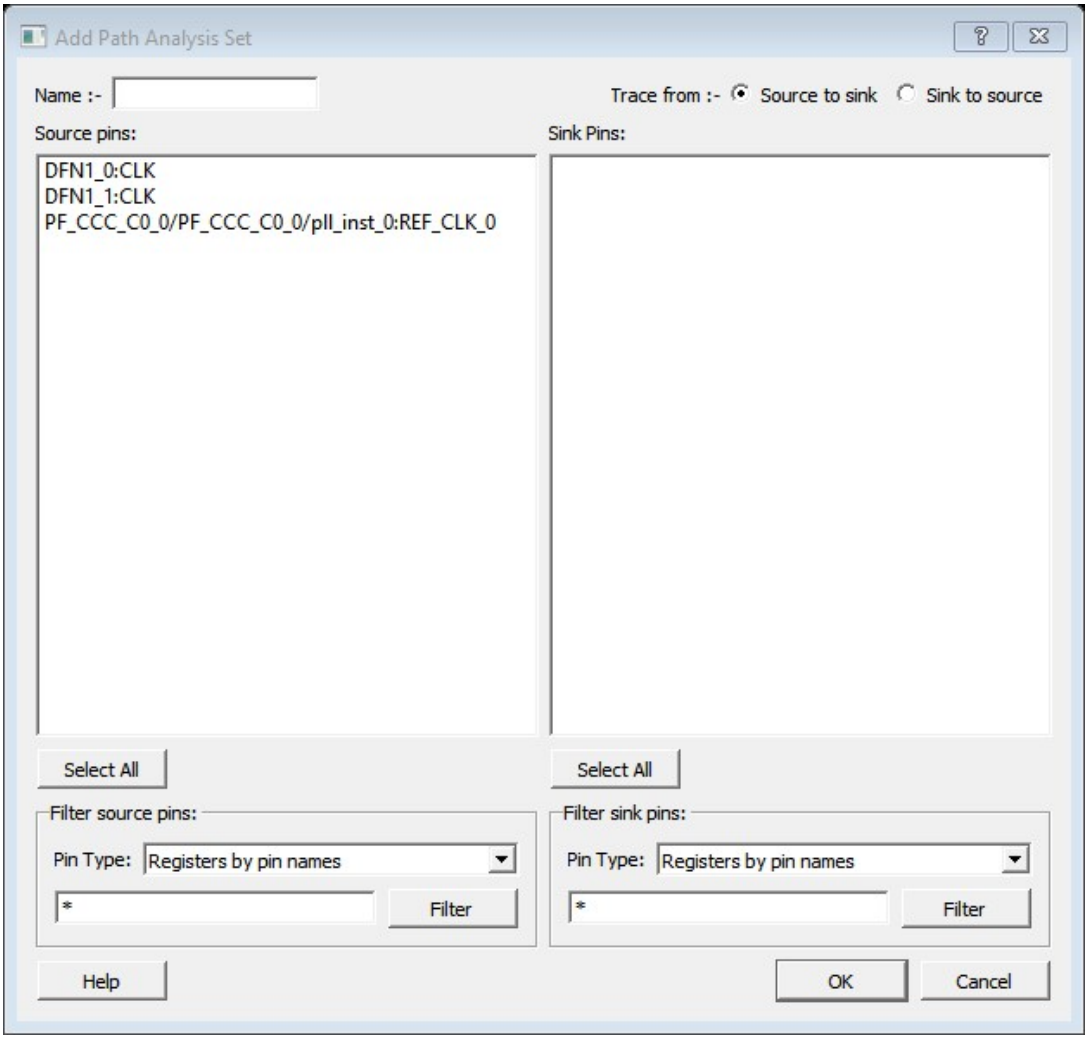


Figure 73 · Add Path Analysis Set Dialog Box

Name

Enter the name of your path set.

Trace from

Select whether you want to trace connected pins from **Source to sink** or from **Sink to source**. By default, the pins are traced Source to sink.

Source Pins

Displays a list of available and valid source pins. You can select multiple pins. To select all source pins, click the **Select All** button beneath the Source Pins list.

Select All

Selects all the pins in the Source Pins list to include in the path analysis set.

Filter Source Pins

Enables you to specify thesource **Pin Type** and the **Filter**. The default pin type is Registers by pin name. You can specify any string value for the **Filter**. If you change the pin type, the **Source Pins** shows the updated list of available source pins.

Sink Pins

Displays list of available and valid pins. You can select multiple pins. To select all source pins, click the **Select All** button beneath the **Sink Pins list.**

Select All

Selects all the pins in the Sink Pins list to include in the path analysis set.

Filter Sink Pins

Enables you to specify thesink **Pin Type** and the **Filter**. The default pin type is Registers (by pin). You can specify any string value for the **Filter**. If you change the pin type, the **Sink Pins** shows the updated list of available sink pins.

Analysis Set Properties Dialog Box

Use this dialog box to view information about the user created set.

To open the **Analysis Set Properties** dialog box (shown below) from the Timing Analysis View, right-click any user-created set in the Domain Browser, and choose **Properties** from the shortcut menu.

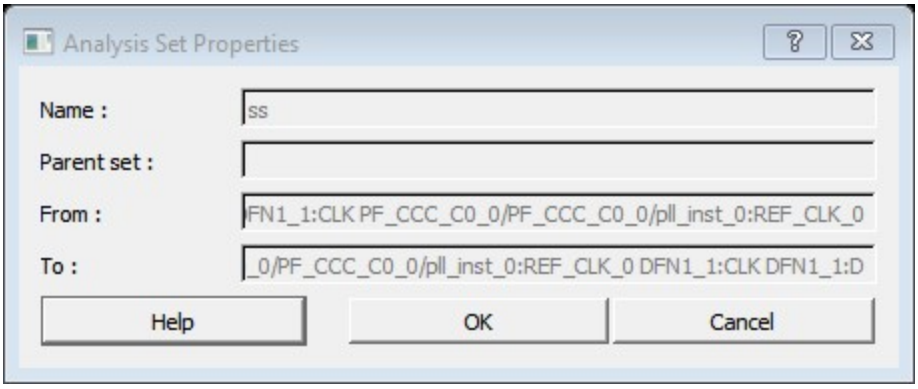


Figure 74 · Analysis Set Properties Dialog Box

Name

Specifies the name of the user-created path set.

Parent Set

Specifies the name of the parent path set to which the user-created path set belongs.

Creation filter

From

Specifies a list of source pins in the user-created path set.

To

Specifies a list of sink pins in the user-created path set.

Edit Filter Set Dialog Box

Use this dialog box to specify a filter.

To open the **Edit Filter Set** dialog box (shown below) from the SmartTime Max/Min Delay Analysis view, right-click an existing filter set in the clock domain browser, and then choose **Edit Set** from the shortcut menu.

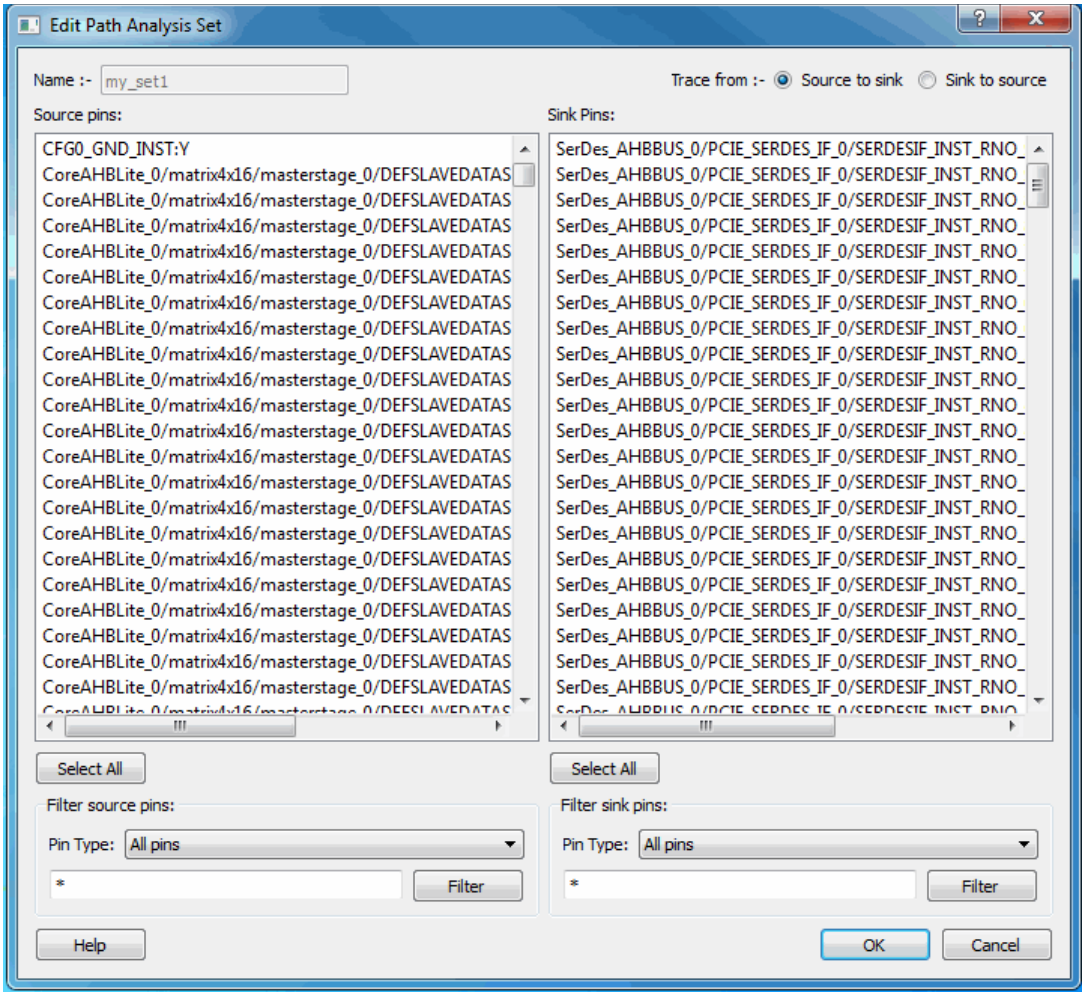


Figure 75 · Edit Path Analysis Set Dialog Box

Name

Specifies the name of the path you want to edit.

Creation filter

Source Pins - Displays a list of source pins in the user-created path set.

Sink Pins - Displays a list of sink pins in the user-created path set.

See Also

Using filters

Customize Analysis View Dialog Box

Use this dialog box to customize the timing analysis grid.

To open the **Customize Analysis View** dialog box (shown below) from the SmartTime Max/Min Delay Analysis View, click the **Customize table** button (circled in red in the figure below) in the Max/Min Delay Analysis View.

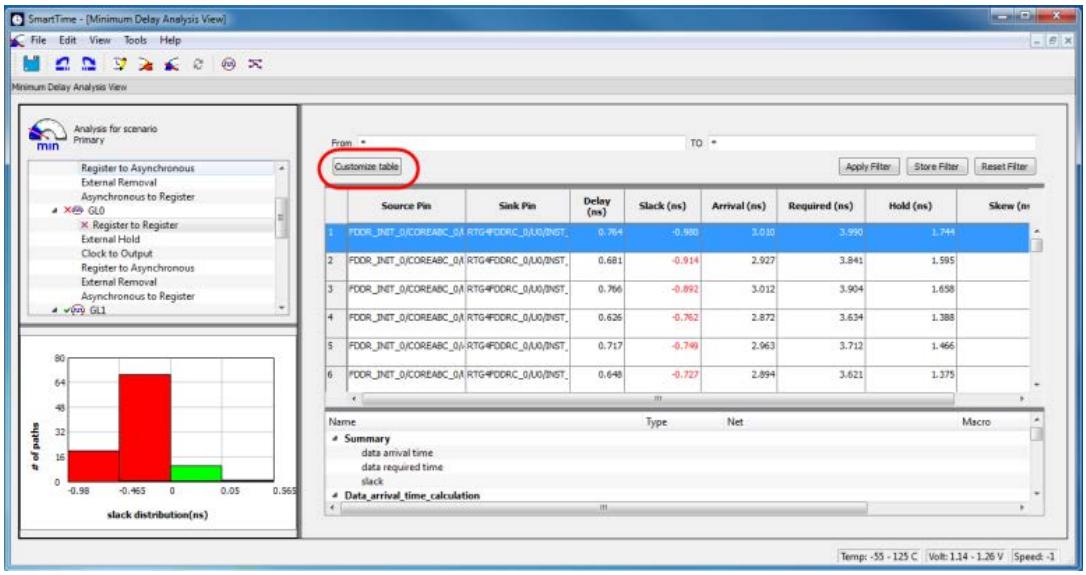


Figure 76 · Customize Table Button

The Customize Paths List Table Dialog Box appears.

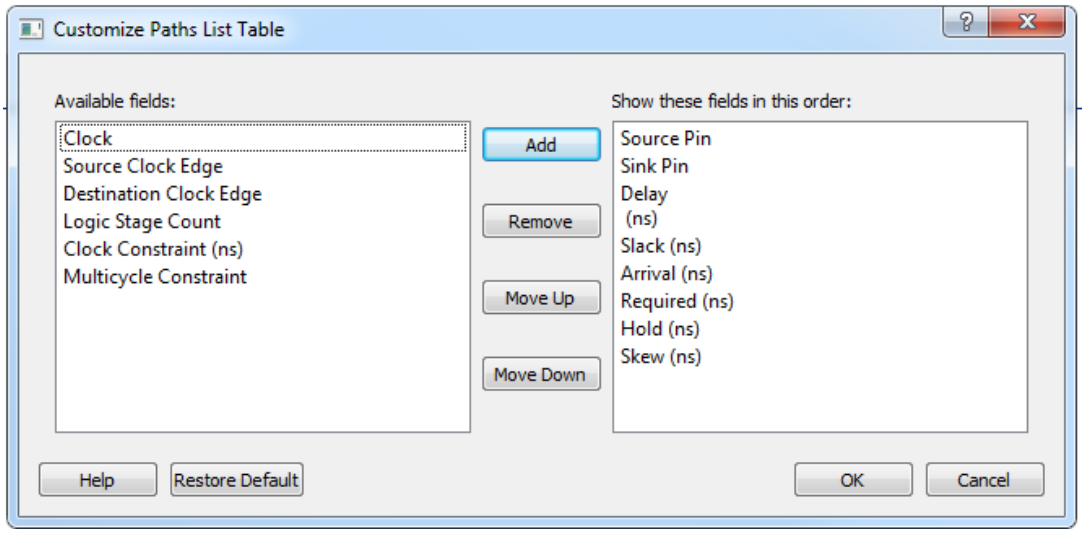


Figure 77 · Customize Paths List Dialog Box

Available Fields

Displays a list of all the available fields in the timing analysis grid.

Show These Fields in This Order

Shows the list of fields you want to see in the timing analysis grid. Use **Add** or **Remove** to move selected items from **Available fields** to **Show these fields in this order** or vice versa. You can change the order in which these fields are displayed by using **Move Up** or **Move Down**.

Restore Defaults

Resets all the options in the General panel to their default values.

Manage Clock Domains Dialog Box

Use this dialog box to specify the clock pins you want to see in the Expanded Path view.

To open the Manage Clock Domain dialog box (shown below) from the SmartTime Max/Min Delay Analysis view, click the  icon.

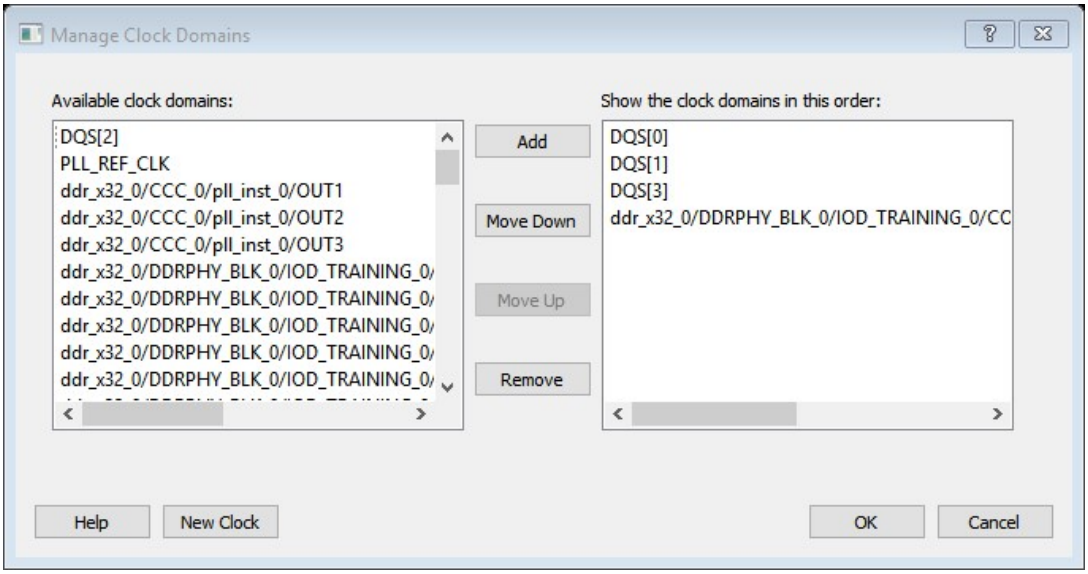


Figure 78 · Manage Clock Domains Dialog Box

Available Clock Domains

Displays alphanumerically sorted list of available clock pins. The first clock pin is selected by default.

Show the Clock Domains in this Order

Shows the clock pins you want to see in the Expanded Path view. Use **Add** or **Remove** to move selected items from **Available clock domains** to **Show the clock domains in this order** or vice versa. You can change the order in which these clock pins are displayed by using **Move Up** or **Move Down**.

New Clock

See Also

Managing Clock Domains

Set False Path Constraint Dialog Box

Use this dialog box to define specific timing paths as being false.

This constraint removes timing requirements on these false paths so that they are not considered during the timing analysis. The path starting points are the input ports or register clock pins and path ending points are the register data pins or output ports. This constraint disables setup and hold checking for the specified paths.

Note: The false path information always takes precedence over multiple cycle path information and overrides maximum delay constraints.

To open the Set False Path Constraint dialog box (shown below) from the SmartTime Constraints Editor, choose **Constraints > Exceptions False Path > Add False Path Constraint**.

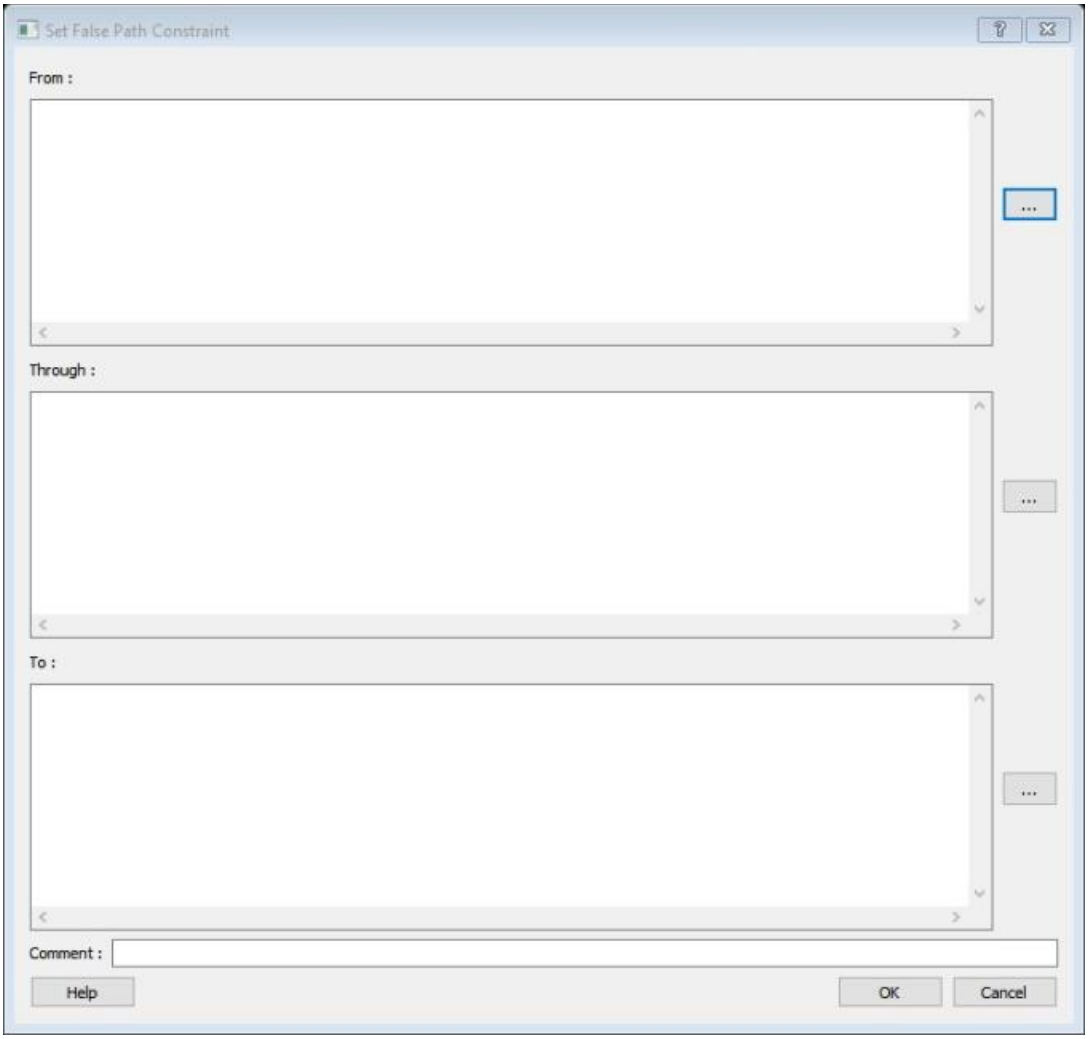


Figure 79 · Set False Path Constraint Dialog Box

From

Specifies the starting points for false path. A valid timing starting point is a clock, a primary input, an inout port, or a clock pin of a sequential cell.

Through

Specifies a list of pins, ports, cells, or nets through which the disabled paths must pass.

To

Specifies the ending points for false path. A valid timing ending point is a clock, a primary output, an inout port, or a data pin of a sequential cell.

Comment

Enables you to provide comments for this constraint.

SmartTime Options Dialog Box

Use this dialog box to specify the SmartTime options to perform timing analysis.

This interface includes the following categories:

- General
- Analysis
- Advanced

To open the SmartTime Options dialog box (shown below) from the SmartTime tool, choose **Tools > Options**.

General

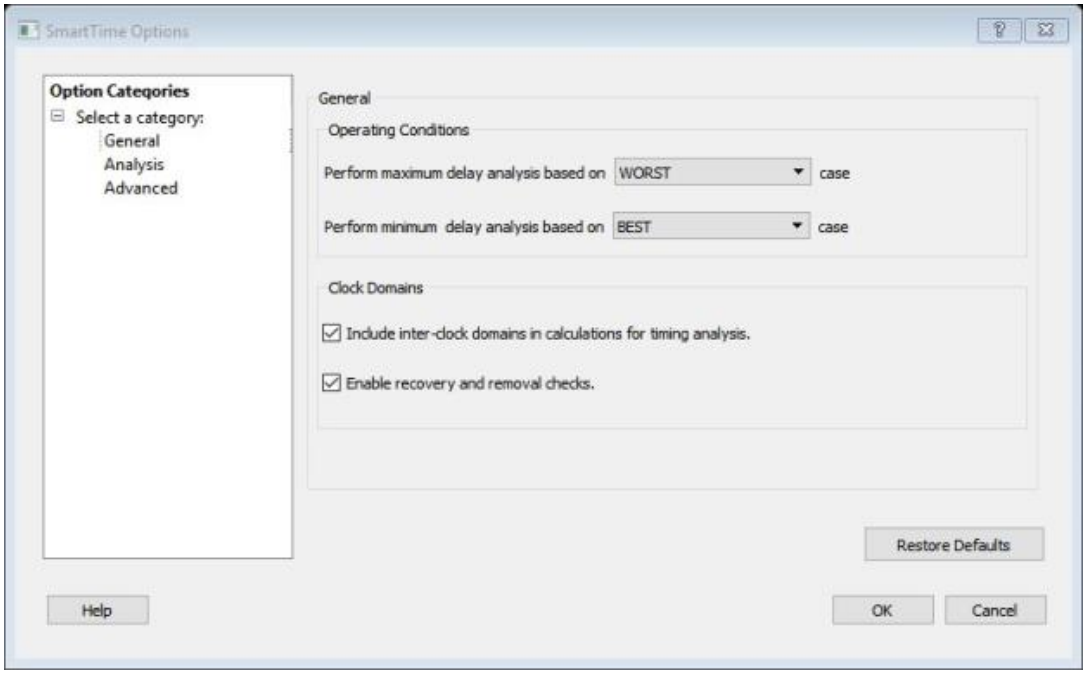


Figure 80 · SmartTime Options- General Dialog Box for SmartFusion2, IGLOO2 and RTG4

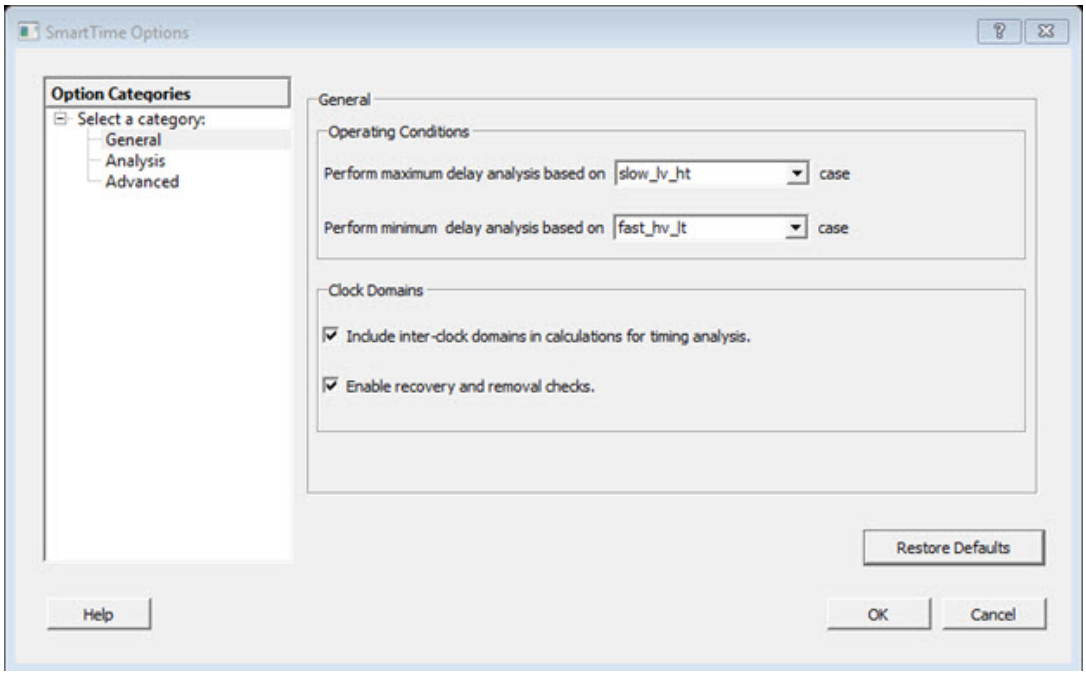


Figure 81 · SmartTime Options - General Dialog Box for PolarFire

Operating Conditions

Allows you to perform maximum or minimum delay analysis based on the Best, Typical, or Worst case. By default, maximum delay analysis is based on WORST case and minimum delay analysis is based on BEST case.

Clock Domains

- **Include inter-clock domains in calculations for timing analysis**: Enables you to specify if SmartTime must use inter-clock domains in calculations for timing analysis. By default, this option is unchecked.
- **Enable recovery and removal checks**: Enables SmartTime to check removal and recovery time on asynchronous signals. Additional sets are created in each clock domain in Analysis View to report the corresponding paths.

Restore Defaults

Resets all the options in the General panel to their default values.

Analysis

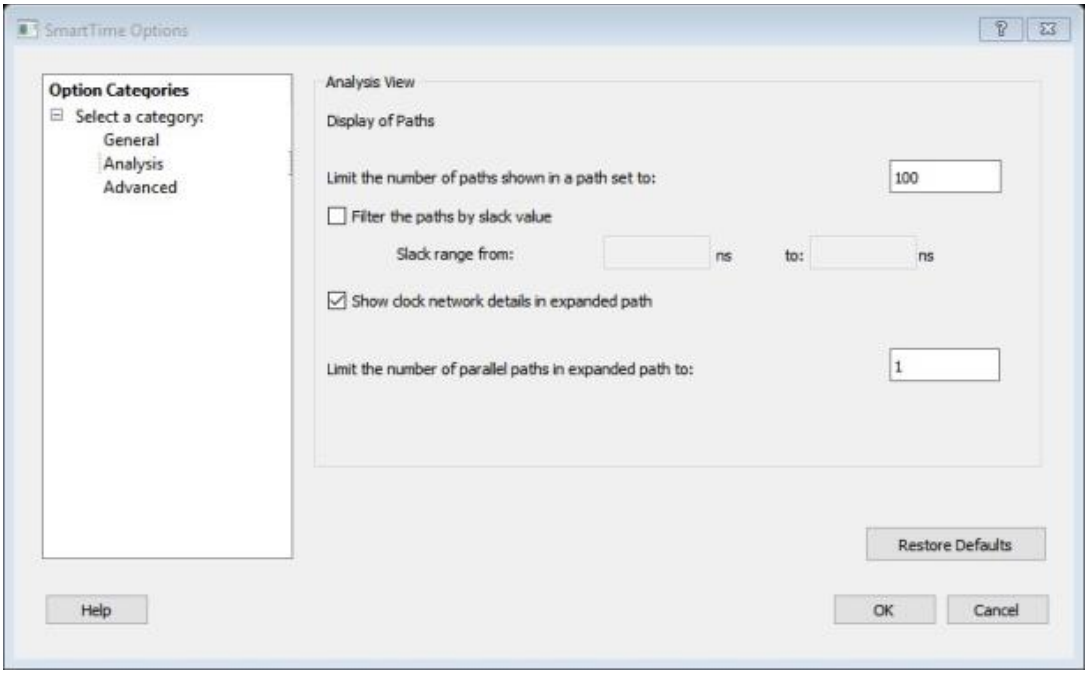


Figure 82 · SmartTime Options - Analysis View Dialog Box

Display of Paths

Limits the number of paths shown in a path set for timing analysis. The default value is 100. You must specify a number greater than 1.

Filter the paths by slack value

Specifies the slack range between minimum slack and maximum slack. This option is unchecked by default.

Show clock network details in expanded path

Displays the clock network details as well as the data path details in the Expanded Path views.

Limit the number of parallel paths in expanded path to: For each expanded path, specify the maximum number of parallel paths that SmartTime displays. The default number of parallel paths is 1.

Restore Defaults

Resets all the options in the Analysis View panel to their default values.

Advanced

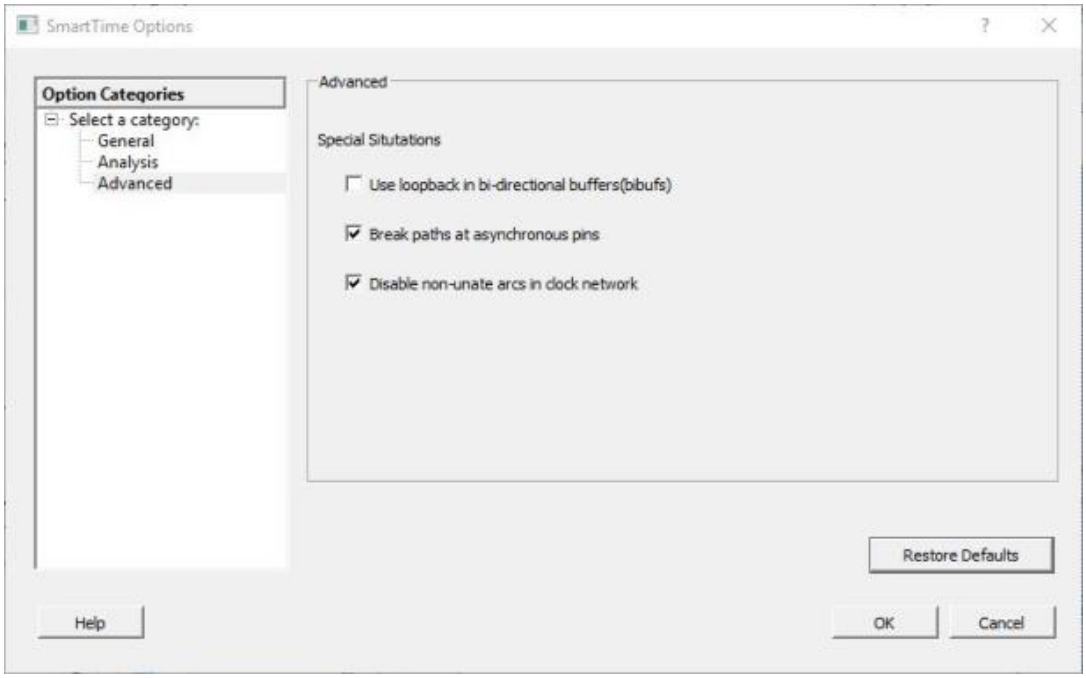


Figure 83 · SmartTime Options - Advanced Dialog Box

Special Situations

Enables you to specify if you need to use loopback in bi-directional buffers (bibufs) and/or break paths at asynchronous pins.

Scenarios

Enables you to select the scenario to use for timing analysis and for timing-driven place-and-route.

Restore Defaults

Resets all the options in the Analysis View panel to their default values.

Store Filter as Analysis Set Dialog Box

Use this dialog box to specify a filter.

To open the **Store Filter as Analysis Set** dialog box (shown below) from the SmartTime Timing Analyzer, select a path and click the **Store Filter** button in the Analysis View Filter.

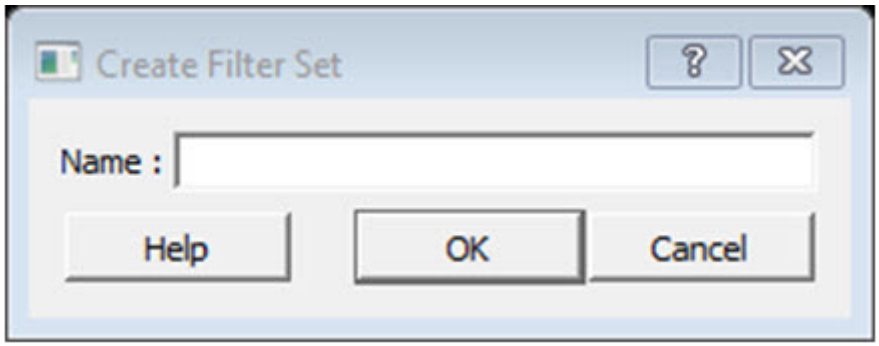


Figure 84 · Store Filter as Analysis Set Dialog Box

Name

Specifies the name of the filtered set.

See Also

Using filters

Timing Bottleneck Analysis Options Dialog Box

Use this dialog box to customize the timing bottleneck report.

You can set report bottleneck options for the following categories:

- General pane
- Bottleneck pane
- Sets pane

To open the Timing Bottleneck Analysis Options dialog box (shown below) from the SmartTime tool, choose **Tools > Bottleneck Analysis**.

General Pane

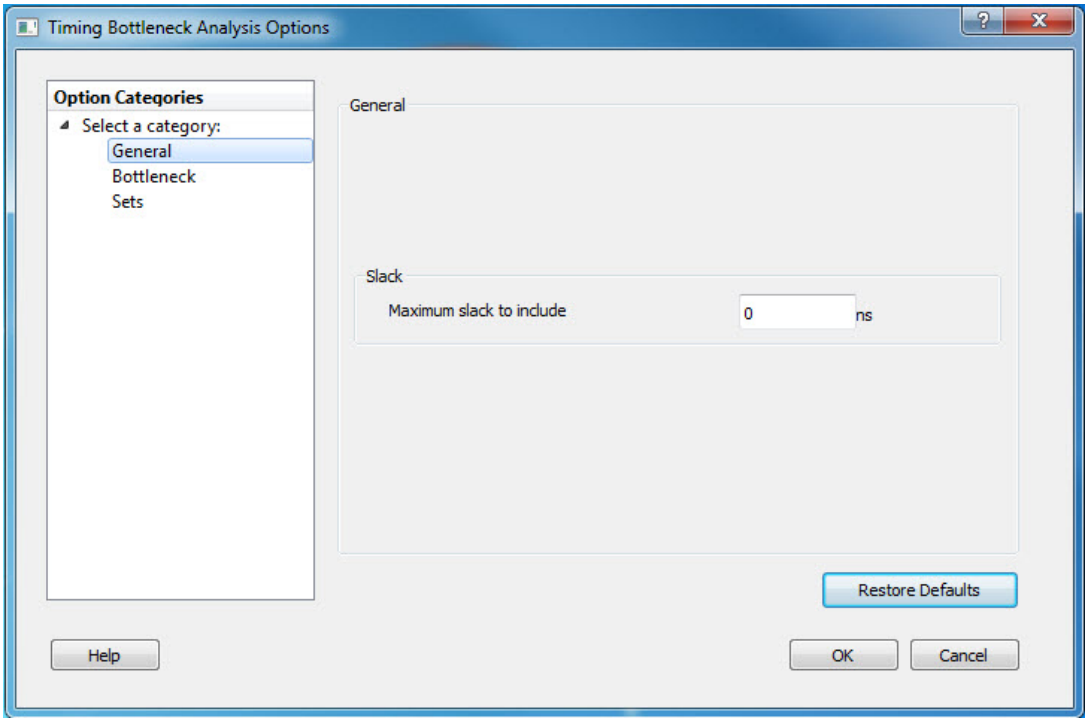


Figure 85 · Timing Bottleneck Report - General Pane Dialog Box

Slack

Lets you specify whether the reported paths will be filtered by threshold, and if so what will be the maximum slack to report. By default the paths are filtered by slack, and the slack threshold is 0.

Restore Defaults

Resets all the options in the General pane to their default values.

Bottleneck Pane

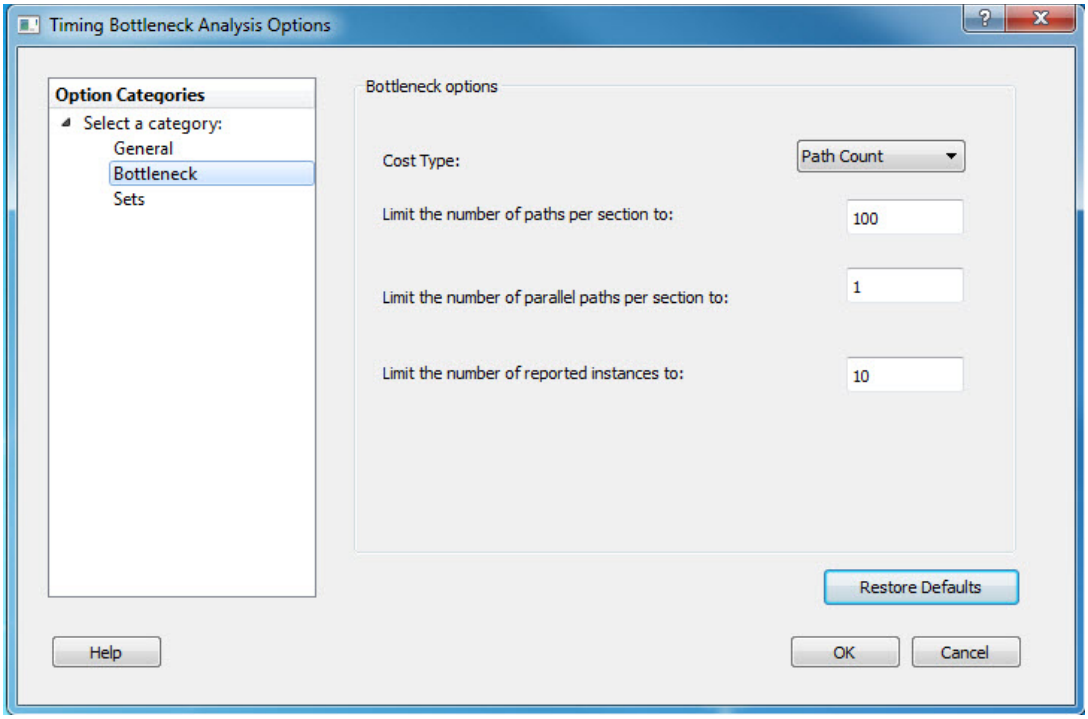


Figure 86 · Timing Bottleneck Report - Bottleneck Pane Dialog Box

Bottleneck Options

Cost Type: Select the cost type that SmartTime will include in the bottleneck report. By default, path count is selected. You may select one of the following two items from the drop-down list:

- **Path count**: This cost type associates the severity of the bottleneck to the count of violating/critical paths that traverse the instance. This is the default.
- **Path cost:** This cost type associates the severity of the bottleneck to the sum of the timing violations for the violating/critical paths that traverse the instance.

Limit the number of paths per section to: Specify the maximum number of paths per set type that SmartTime will include per section in the report. The default maximum number of paths reported is 100.

Limit the number of parallel paths per section to: For each expanded path, specify the maximum number of parallel paths that SmartTime will include in the report. Only cells that lie on these violating paths are reported. The default number of parallel paths is 1.

Limit the number of reported instances: Specify the maximum number of cells that SmartTime will include per section in the report. The default number of cells is 10.

Restore Defaults

Resets all the options in the Bottleneck panel to their default values.

Sets Pane

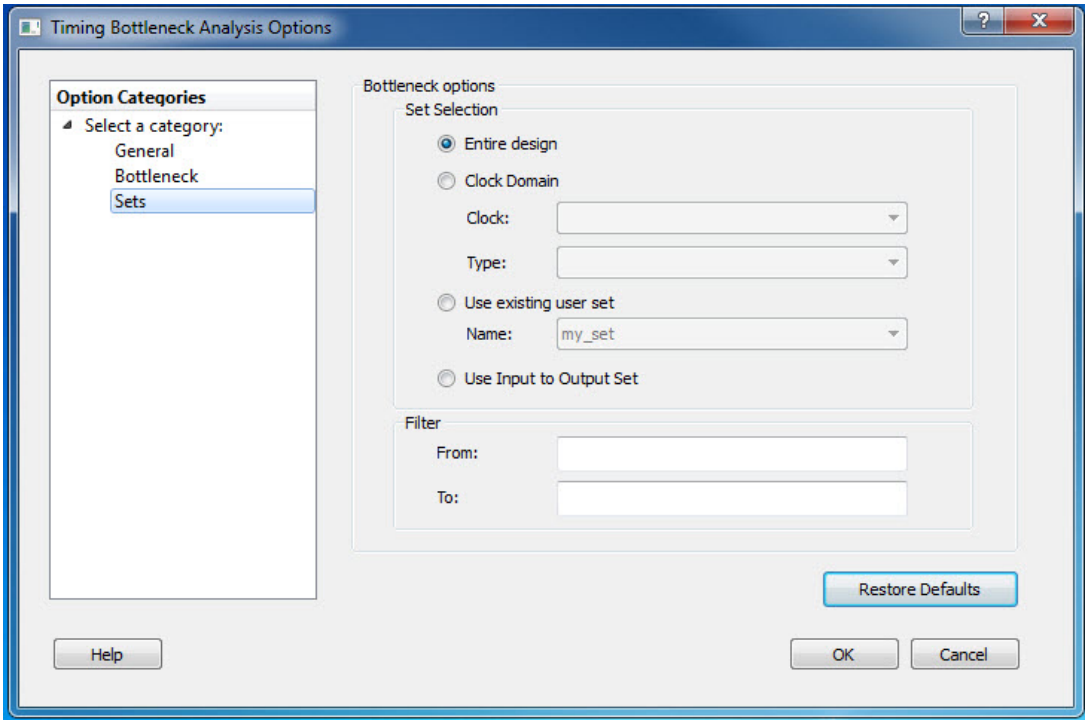


Figure 87 · Timing Bottleneck Report - Sets Pane Dialog Box

This pane has four mutually exclusive options:

- Entire Design
- Clock Domain
- Use existing user set
- Use Input to Output Set

Entire Design: Select this option to display the bottleneck information for the entire design.

Clock Domain: Select this option to display the bottleneck information for the selected clock domain. You can specify the following options:

- Clock: Allows pruning based on a given clock domains. Only cells that lie on these violating paths are reported.
- Type: This option can only be used in conjunction with -clock. The acceptable values are:

Value	Description
Register to Register	Paths between registers in the design
Asynchronous to Register	Paths from asynchronous pins to registers
Register to Asynchronous	Paths from registers to asynchronous pins
External Recovery	The set of paths from inputs to asynchronous pins
External Setup	Paths from input ports to register
Clock to Output	Paths from registers to output ports

Use existing user set: Displays the bottleneck information for the existing user set selected. Only paths that lie within the name set are will be considered towards the bottleneck report.

Filter: Allows you to filter the bottleneck report by the following options:

- From: Reports only cells that lie on violating paths that start at locations specified by this option.
- To: Reports only cells that lie on violating paths that end at locations specified by this option.

Filter defaults to all outputs.

Restore Defaults

Resets all the options in the Paths panel to their default values.

See Also

Bottleneck Analysis

Timing Datasheet Report Options Dialog Box

Use this dialog box to select the output format for your timing datasheet report.

To open the **Timing Datasheet Report Options** dialog box (shown below) from the SmartTime Max/Min Delay Analysis view, choose **Tools > Reports > Datasheet**.

You can generate your report in one of two formats:

Plain Text

Select this option to save your report to disk in plain ASCII text format.

Comma Separated Values

Select this option to save your report to disk in comma-separated value format (.CSV) format, which you can import into a spreadsheet.

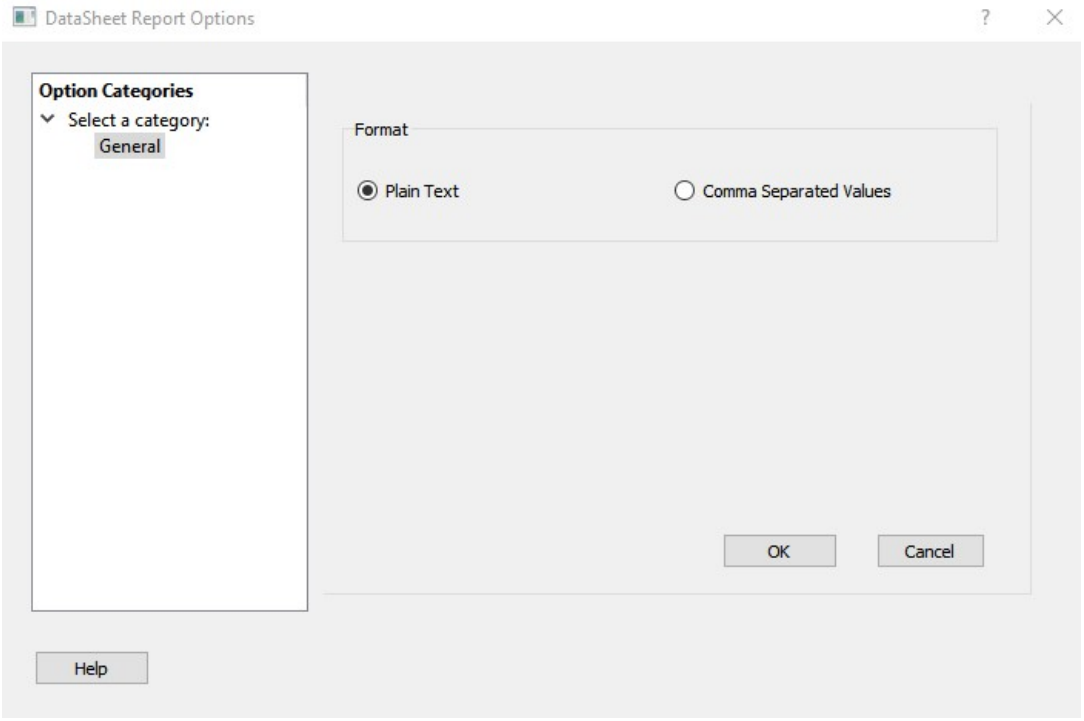


Figure 88 · Report Options Dialog Box

Note: This Datasheet Report feature is not supported for PolarFire.

Timing Report Options Dialog Box

Use this dialog box to customize the timing report.

You can set report options for the following categories:

- General
- Paths
- Sets
- Clock Domains

To open the Timing Report Options dialog box (shown below) from the SmartTime Max/Min Delay Analysis View, choose **Tools > Reports> Timer**.

General

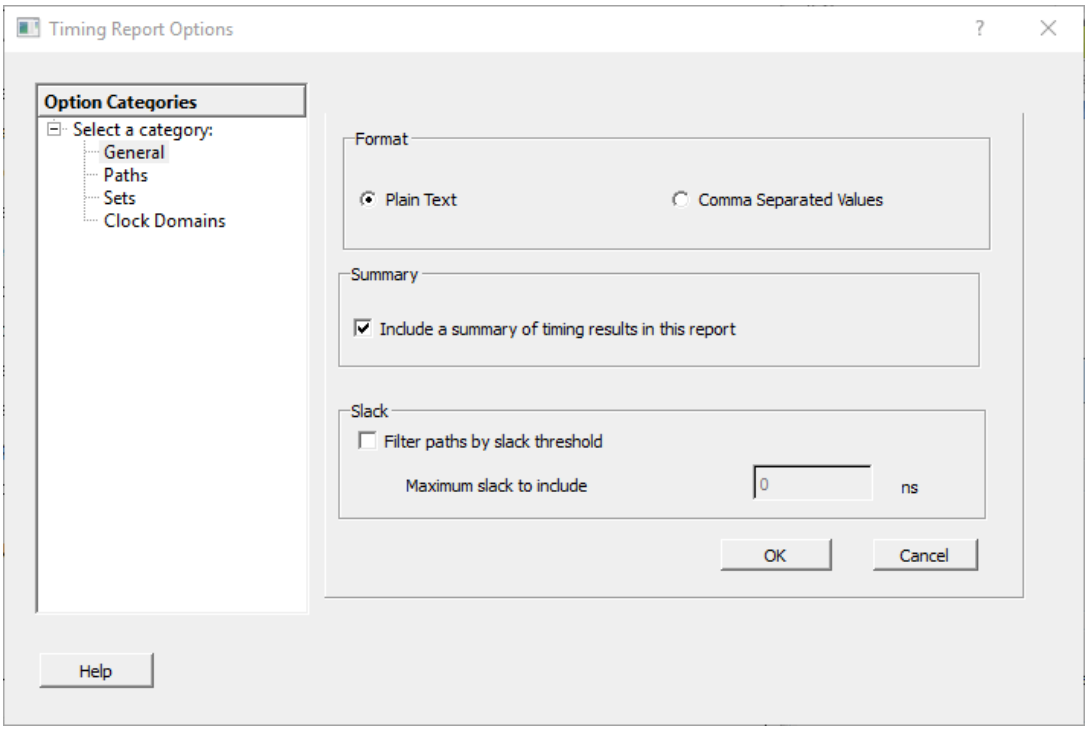


Figure 89 · Timing Report Options - General Dialog Box

Format

Specifies whether or not the report will be exported as a Comma Separated Value (CSV) file or a plain text file. By default, the **Plain Text** option is selected.

Summary

Specifies whether or not the summary section will be included in the report. By default, this option is selected.

Analysis

Specifies the type of analysis to be included in the timing report. It can be either a Maximum Delay Analysis report or Minimum Delay Analysis report. By default, the Maximum Delay Analysis report is included in the timing report.

Slack

Specifies whether the reported paths will be filtered by threshold, and if so what will be the maximum slack to report. By default, the paths are not filtered by slack.

Paths

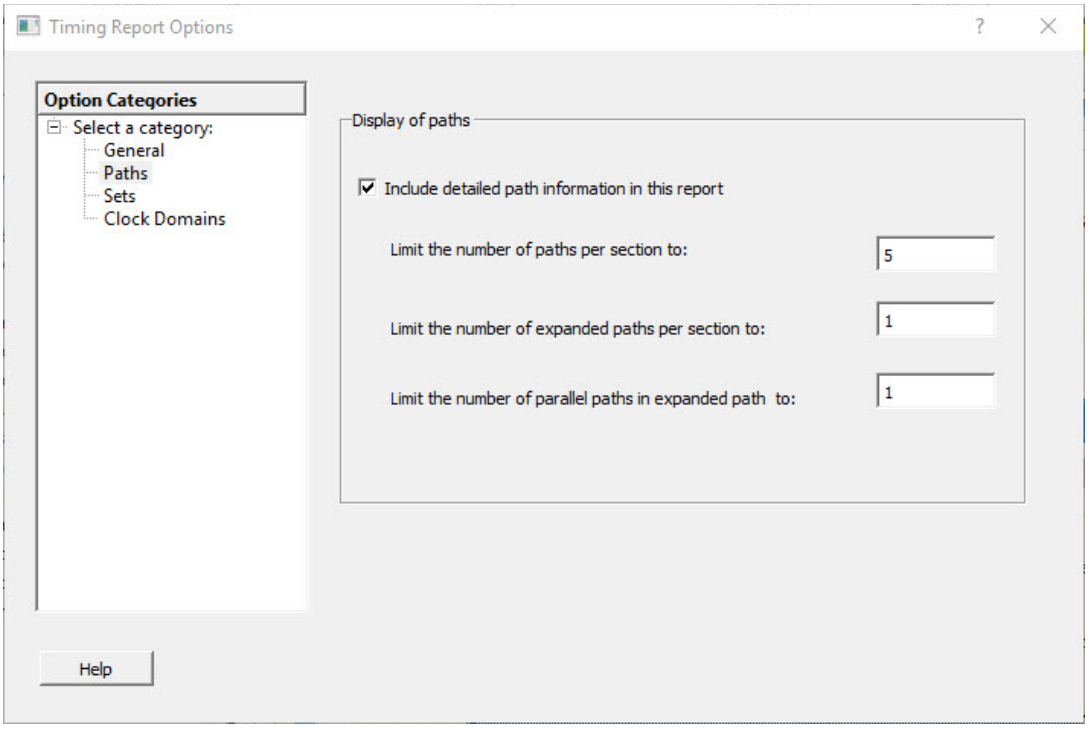


Figure 90 · Timing Report Options - Paths Dialog Box

Display of Paths

Include detailed path information in this report: Check this box to include the detailed path information in the timing report.

Limit the number of reported paths per section to: Specify the maximum number of paths that SmartTime will include per section in the report.

Limit the number of expanded paths per section to: Specify the maximum number of expanded paths that SmartTime will include per section in the report.

Limit the number of parallel paths in expanded path to: For each expanded path, specify the maximum number of parallel paths that SmartTime will include in the report. The default number of parallel paths is 1.

Sets

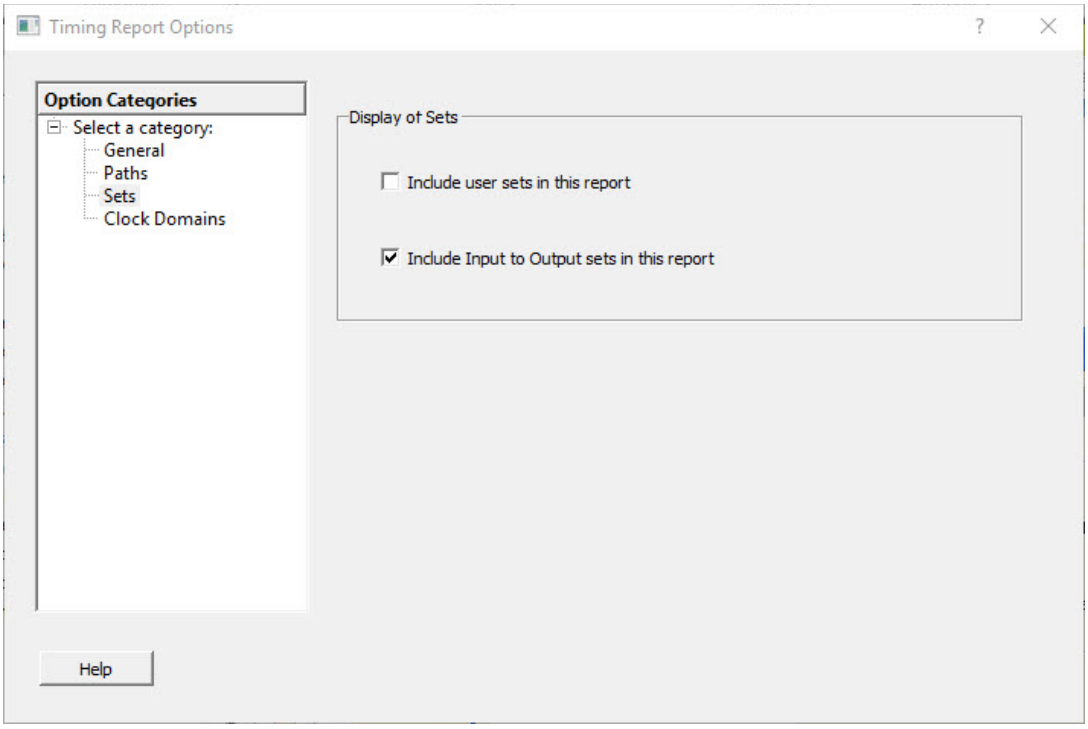


Figure 91 · Timing Report Options - Sets Dialog Box

Display of Sets

Specifies whether or not the user sets will be included in the timing report.

User sets are either filters that you have created and stored on the default paths sets (Register to Register, Inputs to Register, etc.) or Pin to Pin user sets. By default, the paths for these sets are not reported.

In addition, specify whether the Inputs to Output sets will be included in the report. By default, the Input to Output sets are reported.

Clock Domains

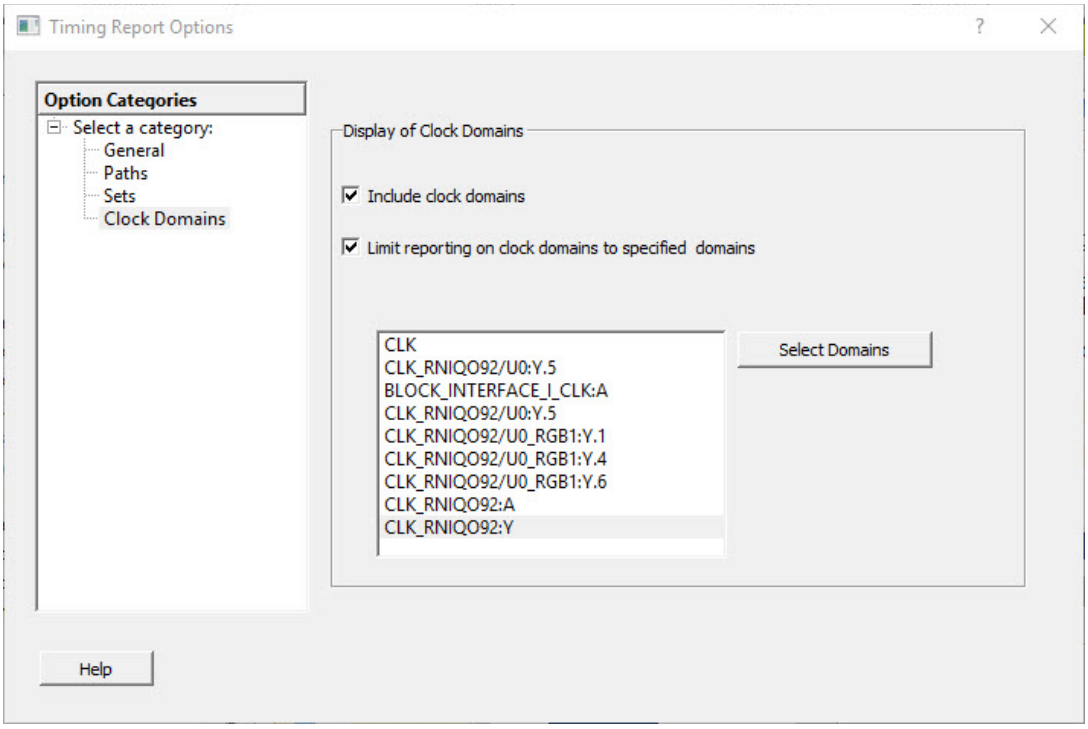


Figure 92 · Timing Report Options - Clock Domains Dialog Box

Display of Clock Domains

Lets you specify what clock domains will be included in the report. By default, the current clock domains used by the timing engine will be reported.

Include Clock Domains

Enables you to include or exclude clock domains in the report. Click the checkbox to include clock domains.

Limit reporting on clock domains to specified domains

Lets you include one or more of the clock domain names in the box, or include additional clock domain names using **Select Domains.**

See Also

Generating a datasheet report

Understanding datasheet reports

Timing Violations Report Options Dialog Box

Use this dialog box to customize the timing violation report.

You can set report violation options for the following categories:

- General
- Paths

To open the Timing Report Options dialog box (shown below) from the SmartTime tool, choose **Tools > Reports > Timing Violations**.

General

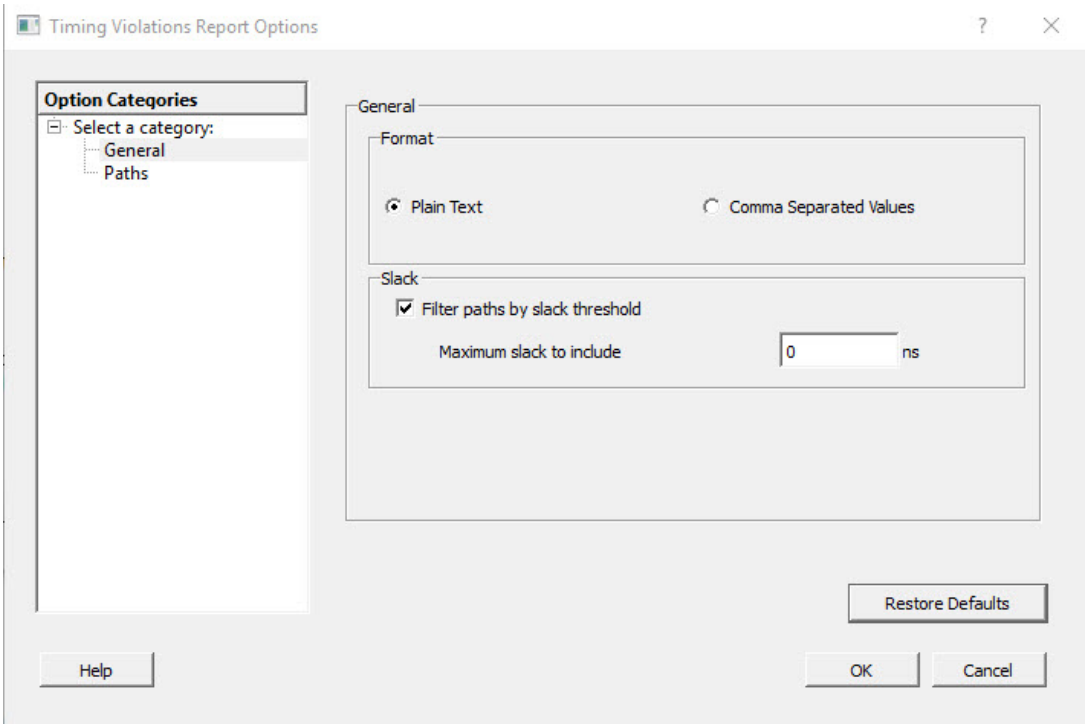


Figure 93 · Timing Violations Report - General Dialog Box

Format

Specifies whether or not the report will be exported as a Comma Separated Value (CSV) file or a plain text file. By default, the **Plain Text** option is selected.

Analysis

Lets you specify what type of analysis will be reported in the report. By default, the report includes Maximum Delay Analysis.

Slack

Lets you specify whether the reported paths will be filtered by threshold, and if so what will be the maximum slack to report. By default the paths are filtered by slack, and the slack threshold is 0.

Restore Defaults

Resets all the options in the General panel to their default values.

Paths

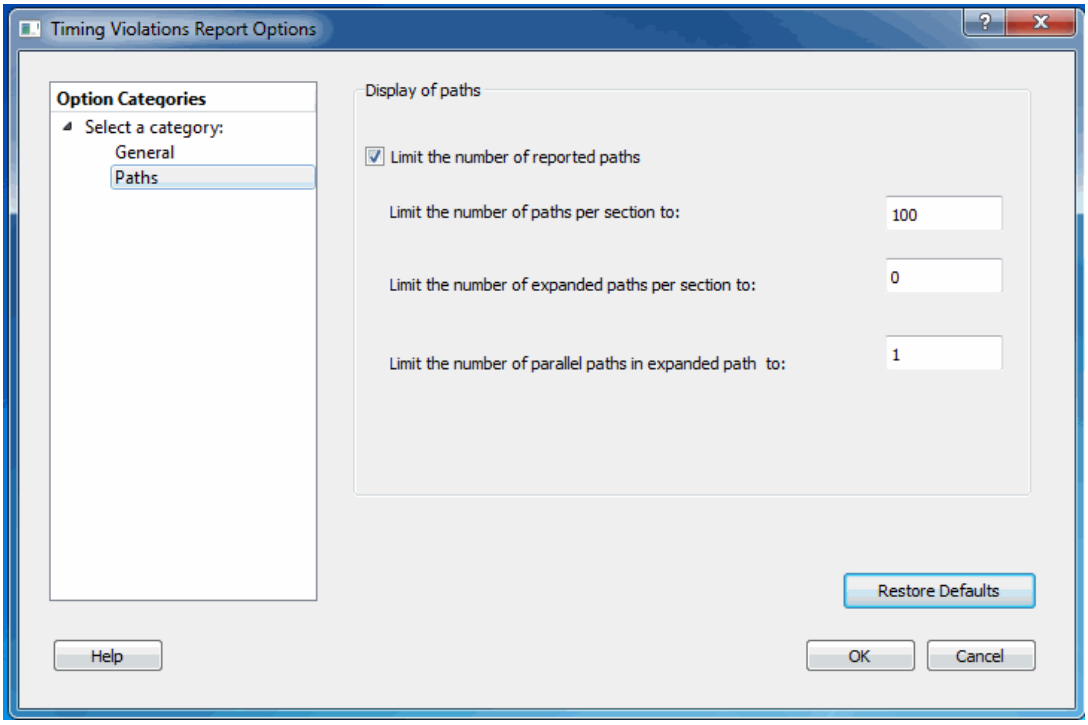


Figure 94 · Timing Violations Report - Paths Dialog Box

Display of paths

Limit the number of reported paths: Check this box to limit the number of paths in the report. By default, the number of paths is limited.

Limit the number of paths per section to: Specify the maximum number of paths that SmartTime will include per section in the report. The default maximum number of paths reported is 100.

Limit the number of expanded paths per section to: Specify the maximum number of expanded paths that SmartTime will include per section in the report. The default number of expanded paths is 0.

Limit the number of parallel paths in expanded path to: For each expanded path, specify the maximum number of parallel paths that SmartTime will include in the report. The default number of parallel paths is 1.

Restore Defaults

Resets all the options in the Paths panel to their default values.

See Also

Generating timing violation report

Understanding timing violation report

Data Change History - SmartTime

The data change history lists features, enhancements and bug fixes for the current software release that may impact timing data of the current design.

To generate a data change history, from the **Help** menu, choose **Data Change History**. This opens a data change history in text format.

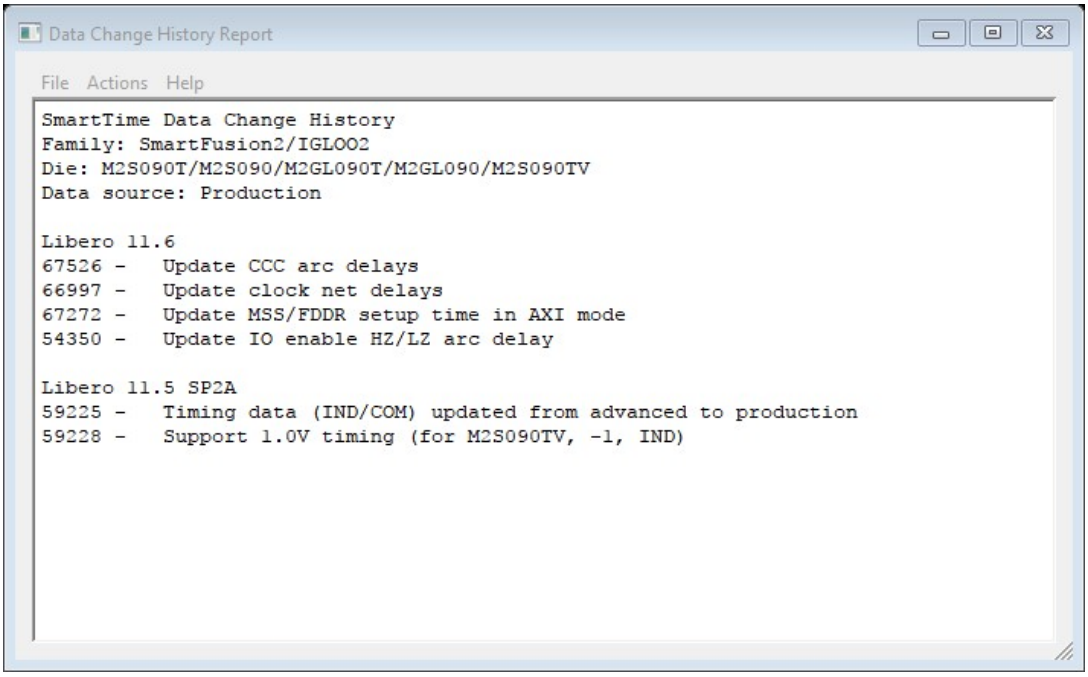


Figure 95 · SmartTime Data Change History Report

Tcl Commands

For details about the Tcl commands supported by SmartTime, refer to the SmartFusion2, IGLOO2, RTG4 Tcl Commands Reference Guide or the PolarFire FPGA Tcl Commands Reference Guide.

Glossary

arrival time

Actual time in nanoseconds at which the data arrives at a sink pin when considering the propagation delays across the path.

asynchronous

Two signals that are not related to each other. Signals not related to the clock are usually asynchronous.

capture edge

The clock edge that triggers the capture of data at the end point of a path.

clock

A periodic signal that captures data into sequential elements.

critical path

A path with the maximum delay between a starting point and an end point. In the presence of a clock constraint, the worst critical path between registers in this clock domain is the path with the worst slack.

dynamic timing analysis

The standard method for verifying design functionality and performance. Both pre-layout and post-layout timing analysis can be performed via the SDF interface.

exception

See timing exception.

explicit clock

Clock sources that can be traced back unambiguously from the clock pin of the registers they deserve, including the output of a DLL or PLL.

filter

A set of limitations applied to object names in timing analysis to generate target specific sets.

launch edge

The clock edge that triggers the release of data from a starting point to be captured by another clock edge at an end point.

minimum period

Timing characteristic of a path between two registers. It indicates how fast the clock will run when this path is the most critical one. The minimum period value takes into consideration both the skew and the setup on the receiving register.

parallel paths

Paths that run in parallel between a given source and sink pair.

path

A sequence of elements in the design that identifies a logical flow starting at a source pin and ending at a sink pin.

path details

An expansion of the path that shows all the nets and cells between the source pin and the sink pin.

path set

A collection of paths.

paths list

Same as path set.

post-layout

The state of the design after you run Layout. In post-layout, the placement and routing information are available for the whole design.

potential clock

Pins or ports connected to the clock pins of sequential elements that the Static Timing Analysis (STA) tool cannot determine whether they are is enabled sources or clock sources. This type of clock is generally associated with the use of gated clocks.

pre-layout

The state of the design before you run Layout. In pre-layout, the placement and routing information are not available.

recovery time

The amount of time before the active clock edge when the de-activation of asynchronous signals is not allowed.

removal time

The amount of time after the active clock edge when the de-activation of asynchronous signals is not allowed.

required time

The time at which the data must be at a sink pin to avoid being in violation.

requirement

See timing requirement.

scenario (timing constraints scenario)

Set of timing constraints defined by the user.

setup time

The time in nanoseconds relative to a clock edge during which the data at the input to a sequential element must remain stable.

sink pin

The pin located at the end of the timing path. This pin is usually the one where arrival time and required time are evaluated for path violation.

skew

The difference between the clock insertion delay to the clock pin of a sink register and the insertion delay to the clock pin of a source register.

slack

The difference between the arrival time and the required time at a specific pin, generally at the data pin of a sequential component.

slew rate

The time needed for a signal to transition from one logic level to another.

source pin

The pin located at the beginning of a timing path.

STA

See static timing analysis.

standard delay format (SDF)

Standard Delay Format, a standard file format used to store design data suited for back-annotation.

static timing analysis

An efficient technique to identify timing violations in a design and to ensure that all timing requirements are met. It is well suited for traditional synchronous designs. The main advantages are that it does not require input vectors, and it exclusively covers all possible paths in the design in a relatively short run-time.

synopsys design constraint (SDC)

A standard file format for timing constraints. Synopsys Design Constraints (SDC) is a Tcl-based format used by Synopsys tools to specify the design intent, including the timing and area constraints for a design. Microsemi SoC tools use a subset of the SDC format to capture supported timing constraints. You can import or export an SDC file from the Designer software. Any timing constraint that you can enter using Designer tools, can also be specified in an SDC file.

timing constraint

A requirement or limitation on the design to be satisfied during the design implementation.

timing exception

An exception to a general requirement usually applied on a subset of the objects on which the requirement is applied.

timing requirement

A constraint on the design usually determined by the specifications at the system level.

virtual clock

A virtual clock is a clock with no source associated to it. It is used to describe clocks outside the FPGA that have an impact on the timing analysis inside the FPGA. For example, if the I/Os are synchronous to an external clock.

WLM

Wire Load Model. A timing model used in pre-layout to estimate a net delay based on the fan-out.