Power Supply Transients on RTAX-S and RTSX-SU Devices

1. Background:

SEE events during operation of power regulators cause the output of the regulator to be as high as the regulator input for short duration of times in order of tenths of microseconds. Consequently any device that is powered by the regulator could see this supply glitch during normal operation of the device. This report summarizes the experiments and data collected to study the impact of these power supply glitches on the RTAX-S and RTSX-SU devices on PCB boards.

2. Initial Evaluation:

2.1. V_{CCA} and V_{CCI} AC stress testing on RTAX-S devices

Initial RTAX-S AC pulsing experiment was performed on a small sample size of devices. A total of eight RTAX2000S-CQ352 devices programmed with the EAQ (Enhanced Antifuse Qualification) design from two different wafer lots, D3HY41 and D33Y41, were stressed at V_{CCA} = 4.0V (1.5 VDC + 2.5 V pulse) with repetitive 1msec AC pulse for 10seconds (~ 100 pulses). V_{CCA} AC pulsing waveform is shown in Figure 1 below. This stress condition was applied on the devices with clocks running at 20MHz and the functionality of the devices was monitored.

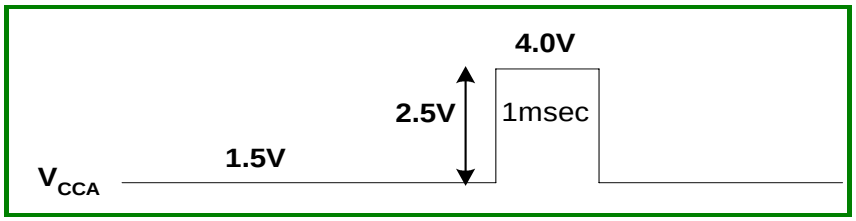

Figure 1: RTAX-S V_{CCA} AC Pulse Testing

All eight devices were tested on ATE (Automated Test Equipment) for post V_{CCA} stress. All devices passed functional, parametric tests and no delta shifts in delay or increase in currents was observed.
Same eight devices were then subjected to an AC pulse stress on the 3.3V V_{CCI} supply. A 5.8V AC peak or (3.3 VDC + 2.5V pulse) with repetitive 1mS AC pulse was applied on V_{CCI} Supply for 10sec (~100 pulses). This stress condition was applied on the devices

with the clocks running at 20MHz and the functionality of the devices monitored on bench setup. The V_{CCI} AC pulsing waveform is shown below in Figure 2 .

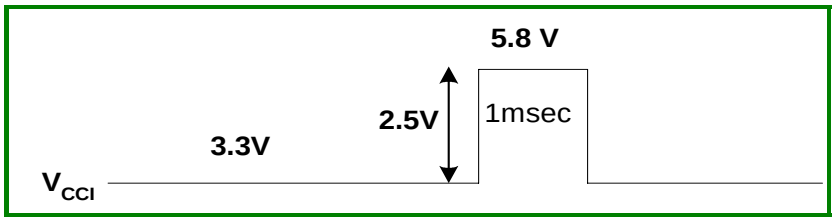

Figure 2: RTAX-S V_{CCI} AC Pulse Testing

The devices were tested on ATE after V_{CCI} AC stress. All devices passed functionality and no delay delta shifts or increase in supply current were observed.

Conclusion:

- No damage was observed with V_{CCA} AC stress of 4.0V and V_{CCI} AC stress of 5.8V.
- There was no I_{CCA}/I_{CCI} increase or functional failures for V_{CCA} AC pulse of 4.0V and V_{CCI} AC pulse of 5.8V for 1mS on RTAX-S devices using eight units as sample size.

2.2. V_{CCA} DC stress testing on RTAX-S Devices

The initial RTAX-S DC stress experiment was done on a small sample size of five devices. Two RTAX2000S-CQ352 EAQ devices from wafer lot D3HY31 were stressed at DC V_{CCA} voltage of 3.0V with clocks running at 2 MHz and functionality of the devices monitored. V_{CCA} voltage ramped in increments of 0.1V and the Standby I_{CCA} current was measured at nominal V_{CCA} voltage of 1.5V at pre and post V_{CCA} DC stress. No increase in currents or loss of functionality observed. Post stress ATE testing of these devices did not show any delay shifts. Additional three RTAX2000S-CQ352 devices from the same wafer lot were stressed to determine the V_{CCA} level at which damage occurs. All three devices were damaged at a V_{CCA} DC voltage of 5.0V. Standby I_{CCA} current is compared at nominal V_{CCA} voltage of 1.5V at pre and post stress for these devices. All three devices showed increased currents at DC V_{CCA} voltage of 5.0V on the bench set up and the post ATE testing showed gross functional and parametric failures.

Conclusion:

- No damage was observed with V_{CCA} DC stress of 3.0V.
- RTAX-S V_{CCA} damage occurred at a DC voltage of 5.0V.

2.3. V_{CCI} DC stress testing on RTAX-S Devices

The above devices that were used for initial evaluation of V_{CCA} and V_{CCI} AC stress experiments were also used for V_{CCI} DC stress experiment. All 8 devices were stressed at DC V_{CCI} voltage of 4.0V. V_{CCI} voltage was ramped from 3.3V to 4.0V with increments

of 0.1V, clocks running at 20MHz while functionality of the device was monitored. I_{CCI} current was monitored during the ramp up and ramp down sequence of V_{CCI}. Standby I_{CCI} current is compared at nominal V_{CCI} voltage of 3.3V pre and post DC stress. No increase in current or loss of functionality was observed with all the devices. The devices were then tested on ATE for delay delta measurements and showed no shifts in deltas. All eight devices were then stressed at DC V_{CCI} voltage of 5.8V for two to three seconds duration. All devices passed functional and parametric tests at post DC stress ATE testing.

Conclusion:

- All eight devices passed after V_{CCI} DC stress of 4.0V
- No damages or loss of functionality or increase in currents observed for the devices that were stressed up to V_{CCI} DC voltage of 5.8V for two to three seconds.

2.4. V_{CCA} AC stress testing on RTSX-SU Devices

The initial RTSX-SU **V_{CCA}** AC stress experiment was conducted on small sample size of 10 devices. Two RTSX72SU-CQ256 P7/SSU (programmed) devices from wafer lot D303Y11 were stressed at V_{CCA} voltage of 5.5V (2.5 VDC + 3.0 V pulse) with repetitive 1msec AC pulse for 10seconds (~100 pulses). This stress condition was applied on devices with clocks running at 20MHz and functionality of the device monitored. V_{CCA} AC pulsing waveform is shown below in Figure 3.

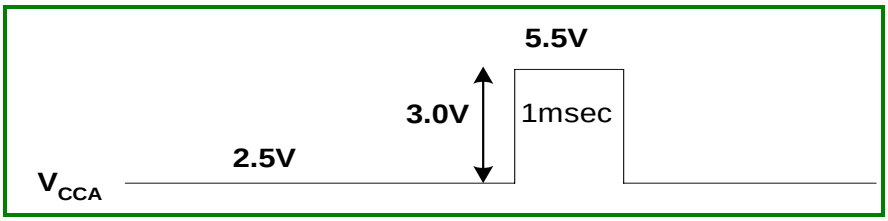

Figure 3: RTSX-SU V_{CCA} AC Pulse Testing

There were no functional failures observed or I_{CCA} increase for an AC pulse of 1msec at post stress ATE testing. AC pulse test was repeated on four RTSX72SU devices each from additional two different wafer lots (D1MM81 and D1N8A1) using the same AC stress condition described above. All eight devices were tested for functionality on ATE after V_{CCA} AC stress. All devices passed functionality and no delta shifts in delay or increase in currents were observed.

Conclusion:

- 10 devices from three different wafer lots passed functional and parametric tests after V_{CCA} AC stress of 5.5V.
- No increase in currents or delta shifts in delay were observed at post ATE tests.

2.5. V_{CCA} DC stress testing on RTSX-SU Devices

The above devices that were used for V_{CCA} AC stress experiment were also used for DC V_{CCA} stress experiment. Two devices from wafer lot D303Y11 were stressed at V_{CCA} DC voltage of 4.5V with similar set up as RTAX-S devices with clocks running and monitoring functionality. V_{CCA} current was measured at nominal V_{CCA} voltage of 2.5V at pre and post DC stress with both states of the clocks on the bench. ATE testing showed both devices did not show any loss of functionality, increase in I_{CCA} or increased delays. These two devices were stressed to damage V_{CCA} level with clocks running and the functionality of the devices being monitored. Both devices were damaged at a DC V_{CCA} voltage of 7.1V. I_{CCA} current was measured at V_{CCA} = 2.5V at pre and post stress and showed clock buffer damage for both the devices. One device (SN6855) showed an increase in current and loss of functionality where as the second device (SN6898) passed functionality but failed I_{CCA} test. Table1 below shows pre and post stress I_{CCA} current measurements for the two devices.

Devices	Pre Stress I_{CCA}	Post Stress I_{CCA}
SN6855	2mA (Clk_hi/lo)	Clk_hi = 21mA Clk_lo = 506mA
SN6898	2mA (Clk_hi/lo)	Clk_hi = 58mA Clk_lo = 83mA

Table 1: Pre and Post I_{CCA} DC stress currents

Eight devices that were used for V_{CCA} AC stress experiment from two different wafer lots (D1MM81 and D1N8A1) and additional 4 devices (total of 12 devices) were stressed at V_{CCA} ranging from 5.0V to 6.5V for 1sec with clocks running and the functionality of the devices being monitored on the bench. Standby I_{CCA} current is compared at nominal V_{CCA} voltage of 2.5V at pre and post DC stress. 3 devices from wafer lot D1MM81 were damaged at V_{CCA} = 6.0V and one device failed at V_{CCA} = 6.5V. Two devices from wafer lot D1N8A1 were damaged at V_{CCA} = 6.0V and two at V_{CCA} = 6.5V, four devices were good at V_{CCA} = 6.5V. The four devices that passed at V_{CCA} = 6.5V on the bench were tested on ATE for post stress measurements. Three of four devices passed functional and parametric tests and one device failed functional test and passed other parametric tests. No increase in currents was observed for these devices. Table 2 below shows post DC stress bench testing results on these devices.

Wafer Lot#	# of Devices	Damaged @ V_{CCA} = 6.0V	Damaged @ V_{CCA} = 6.5V	Good @ V_{CCA} = 6.5V
D1N8A1	8	2	2	4
D1MM81	4	3	1	0

Table 2: Post V_{CCA} DC stress result

Conclusion:

- RTSX-SU devices did not fail when subjected to a DC voltage of 4.5V
- The minimum V_{CCA} damage level for RTSX-SU devices was found to be 6.0V DC.

3. Additional Testing on Larger Sample Size:

3.1. V_{CCA} and V_{CCI} AC stress experiments of RTAX-S Devices

The sample size for the above experiments was increased to collect additional data points. This additional data was collected at single voltage levels and devices did not get stressed to damage voltage levels. A total of 26 RTAX2000S-CQ352 EAQ devices from wafer lot D3T0N1 were stressed at V_{CCA} = 4.0V (1.5 VDC + 2.5 V pulse) with repetitive 1mS AC pulse (~ 100 pulses). The Same AC stress condition that was described in Figure 1 is applied to V_{CCA} with clocks running at 20MHz and functionality of the devices monitored on the bench. All devices were then tested for functionality at post AC stress. All devices passed functional and delay measurements. No increase in currents or delay delta shifts was observed for these devices.
26 RTAX2000S-CQ352 devices from above sample were used for V_{CCI} AC stress experiment. All devices were stressed at V_{CCI} = 6.0V (3.3 VDC + 2.7V pulse) with repetitive 1mS AC pulse (~ 100 pulses). This stress condition was applied to the V_{CCI} supply with clocks running at 20MHz and functionality of the device being monitored on the bench setup. V_{CCI} AC pulsing waveform is shown below in Figure 4.

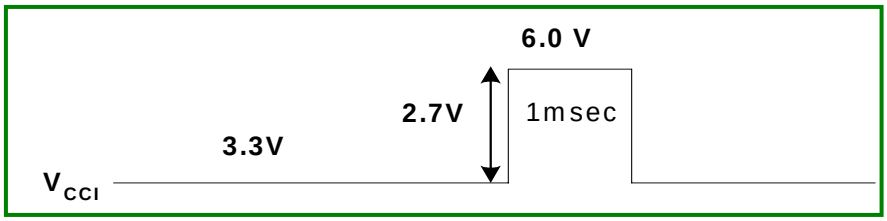

Figure 4: RTAX-S V_{CCI} AC Pulse Testing on Large Sample Size

All 26 devices passed functional and parametric tests at post AC stress ATE testing. No increase in currents or delay delta shifts was observed.

Conclusion:

- All 26 devices passed post V_{CCA} AC stress of 4.0V. No loss of functionality or increase in currents observed at post ATE V_{CCA} AC stress testing.
- All 26 devices passed post V_{CCI} AC stress of 6.0V. No loss of functionality or increase in currents observed at post V_{CCI} AC stress testing.

3.2. V_{CCA} and V_{CCI} DC stress experiments of RTAX-S Devices

The above devices that were used for V_{CCA} and V_{CCI} AC stress experiment were also used for 1.5V $\mathbf{V_{CCA}}$ and 3.3V V_{CCI} DC stress experiment. Total of 26 devices were stressed at V_{CCA} DC voltage of 3.5V for three to four seconds with clocks running at 20MHz and functionality of the devices being monitored on the bench. Standby I_{CCA} current was measured at nominal V_{CCA} voltage of 1.5V at pre and post V_{CCA} DC stress. All devices were then tested for functionality on ATE. All devices passed functional and parametric tests at post V_{CCA} DC stress of 3.5V. No increase in currents or delay delta shifts was observed.

These devices were then stressed at DC V_{CCI} voltage of 5.5V. The DC stress condition of 5.5V was applied on V_{CCI} supply for three to four seconds with clocks running and functionality of the devices being monitored during DC stress. Standby I_{CCI} current is measured at nominal V_{CCI} voltage of 3.3V for pre and post V_{CCI} DC stress. These devices were then tested for functionality. All 26 devices passed functional and parametric tests at post V_{CCI} DC stress ATE testing. No increase in currents or loss of functionality was observed.

Conclusion:

- All 26 RTAX-S devices passed V_{CCA} DC stress of 3.5V and V_{CCI} DC stress of 5.5V. All devices were functional after DC stress on V_{CCA} and V_{CCI} supplies.

3.3. V_{CCA} AC and DC stress experiments of RTSX-SU Devices

This experiment was performed on large sample of RTSX72SU devices. Total of 17 RTSX72SU-CQ256 P7/SSU devices from wafer lot D1N8A1 were stressed at V_{CCA} voltage of 5.5V (2.5 VDC + 3.0 V pulse) with repetitive 1mS AC pulse for 10seconds (~100 pulses). Same AC stress condition that was described in Figure 3 above was applied on V_{CCA} supply with clocks running and functionality of the devices monitored on the bench setup. All devices were then tested on ATE for post stress testing. All devices passed functionality and parametric tests after AC V_{CCA} stress of 5.5V with 1mS pulse. No I_{CCA} increase or delay delta shifts observed.

The above devices were then stressed at V_{CCA} DC voltage of 4.5V for three to four seconds with clocks running at 20MHz and device functionality monitored on the bench. Standby I_{CCA} current was measured at pre and post V_{CCA} DC stress at nominal V_{CCA} voltage of 2.5V. All devices passed post DC V_{CCA} stress of 4.5V on ATE. No functional or parametric failures were observed.

Conclusion:

- All 17 RTSX-SU devices passed after V_{CCA} AC stress of 5.5V and V_{CCA} DC stress of 4.5V.
- No loss of functionality or increase in I_{CCA} currents or delay delta shifts was observed for this stress condition.

All above experiments were performed at room temperature.

4. Summary of RTAX-S and RTSX-SU Power Supply Transients:

Initial evaluation of RTAX-S/RTSX-SU V_{CCA} and V_{CCI} AC pulsing and DC stress testing was completed to determine the voltage required to damage the devices. A larger sample size of RTAX-S and RTSX-SU devices stress data collection was collected at higher V_{CCA} and V_{CCI} levels which demonstrated these devices can withstand increased supply levels for short periods as described above.

RTAX-S devices from three different wafer lots were stressed at V_{CCA} overshoot voltage of 4.0V and V_{CCI} voltage of 6.0V with repetitive 1msec AC pulse for 10seconds. No increase in currents or loss of functionality was observed with these devices at post AC stress testing. RTAX-S EAQ devices stressed at V_{CCA} DC voltage of 3.5V and V_{CCI} DC voltage of 5.5V for three to four seconds. All devices passed post DC stress tests. No functional or increase in currents were observed with these devices. RTAX-S V_{CCA} damage level was found to be a DC voltage of 5.0V.

RTSX-SU devices from three different wafer lots were stressed at V_{CCA} overshoot voltage of 5.5V with repetitive 1msec pulse for 10seconds and V_{CCA} DC voltage of 4.5V for three to four seconds. No increase in currents or loss of functionality were observed with these devices at post AC and DC stress testing. All devices passed functional and parametric tests. The minimum V_{CCA} damage level for RTSX-SU devices was found to be a DC voltage of 6.0V.

5. Conclusion:

All RTAX-S and RTSX-SU devices were stressed beyond their maximum absolute recommended conditions using AC and DC stress and above data indicate the devices are robust and reliable. But Actel advises customers not to stress the devices beyond the datasheet limits.

RTAXS and RTXS are fundamentally suited for reliability in overstress conditions. This is due to the nature of programming the antifuses which require high voltages to be applied to the circuit during programming. As an example the RTAX-S is manufactured on a 0.15u process that normally uses 70Å gate oxides. This was beefed up to 90Å just to safely withstand the 6.2 Volt programming operation. To insure good programming yield these circuits have been stress tested three different times during manufacturing at the voltages of V_{CCA} = 2.6V for 100msec on RTAX-S and V_{CCA} = 5.25V for 100msec on RTSX-SU. Thus every RTAX-S and RTSX-SU device has been designed and tested to withstand these voltages and any weak transistors have already been removed from the population before shipment to the customer.

There is no such requirement for ASICs as they are only required to function at the nominal voltages. Hence they will be fundamentally more susceptible to overstress conditions. A recent article was presented at the IEEE Aerospace Conference detailing the better reliability of the RTAXS over an ASIC by a factor of 10. This result was based on thousands of parts and millions of device hours testing in very harsh condition