PB0056

Product Brief

RTG4 FPGAs in Plastic Package

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Microsemi

a Microchip company

Contents

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 3.0

Revision 3.0 was published in May 2020. The following is a summary of changes.

- Updated FCG1657 to "FC1657 and FCG1657" in *Table 1 • RTG4 FPGA Product Family* on page 3.
- Updated *Ordering Information* on page 5.
- Updated *RTG4 Device Marking Specifications* on page 5.

1.2 Revision 2.0

Revision 2.0 was published in February 2020. The following is a summary of changes.

- Updated Marketing Specifications and Ordering Information with prototype information.
- Updated Design Hardware section with RTG4 plastic package compatibility with ceramic packages.

1.3 Revision 1.0

Revision 1.0 was published in May 2019. It is the first publication of this document.

2 Introduction to RTG4 FPGAs

RTG4™ FPGAs in plastic package integrate Microsemi's fourth-generation flash-based FPGA fabric and high-performance interfaces, such as SerDes on a single chip, while maintaining the resistance to radiation-induced configuration upsets in radiation environments. For example, space flight, high-altitude aviation, medical electronics, and nuclear power plant control. The RTG4 family offers up to 151,824 registers, which are hardened by design against radiation-induced single event upsets (SEUs).

2.1 Features and Benefits

Following are the features supported in RTG4 FPGAs.

2.1.1 Radiation Tolerance

- Configuration memory upsets immunity to LET > 103 MeV.cm^2/mg
- Single-event latch-up (SEL) immunity to LET > 103 MeV.cm^2/mg
- SEU-hardened registers eliminate the need for triple-module redundancy (TMR)
  - Immune to single-event upsets (SEU) to LET > 37 MeV.cm^2/mg
  - SEU rate < 10^{-12} errors/bit-day (GEO Solar Min)
- SRAM has a built-in error detection and correction (EDAC)
  - Upset rate < 10^{-11} errors/bit-day (GEO Solar Min)
  - Single error correction and double error detection (SECDED)
- Single-event transient (SET) upset rate < 10^{-8} errors/bit-day (GEO Solar Min) with optional SET filter
- Total ionizing dose (TID) > 100 krad

2.1.2 High-Performance FPGA

- Efficient four-input look-up tables (LUTs) with carry chains for high system performance up to 300 MHz without SET filter
- 209 blocks of dual-port 24.5 kb SRAM (Large SRAM) with 250 MHz synchronous performance (512 × 36, 1 kb × 18)
- 462 DSP mathblocks with 18-bit × 18-bit input signed multiplication and 44-bit output accumulator
  - High-performance, 300 MHz (without SET filter) across military temperature: –55 °C to 125 °C
- 16 Spacewire clock and data recovery circuitry instances, allowing Spacewire interface up to 200 Mbps

Note: The Spacewire interface protocol is not included but can be implemented in the FPGA fabric.

2.1.3 High-Speed Serial Interfaces

Twenty-four lanes of 3.125 Gbps serialization/deserialization (SerDes) support the following.

- XGXS/XAUI extension (to implement a 10 Gbps XGMII Ethernet PHY interface)
- Native SerDes interface facilitates implementation of serial rapidIO (SRIO) in FPGA fabric or an SGMII interface to a soft Ethernet MAC
- PCI Express (PCIe) Gen1 hard IP core
  - ×1, ×2, and ×4 lane(s) PCI Express core
  - Up to 2 Kbytes maximum payload size
  - 64-bit/32-bit AXI/AHB master and slave interfaces to the application layer

2.1.4 High-Speed Memory Interfaces

Two high-speed DDR2/DDR3 memory controllers supporting the following.

- DDR2 and DDR3 at 333 MHz (667 Mbps) and LPDDR at 133 MHz (266 Mbps) at the maximum clock rate
- EDAC option with SECDED
- ×9, ×12, ×18, and ×36 bus widths

2.1.5 Specifications

- 1.2 V nominal core voltage
- Single-ended I/Os—LVCMOS 1.2 V to 3.3 V, LVTTL, and PCI
- Voltage reference I/Os with performance at 600+ Mbps
  - SSTL2, SSTL18, SSTL15, HSTL18, and HSTL15
- True LVDS (600+ Mbps) differential receiver and true current-mode driver, with a built-in termination.
- Clock sources include high-precision 50 MHz embedded RC oscillator
- Eight clock conditioning circuits (CCCs) with PLLs
  - Frequency: Input 10 MHz to 200 MHz and output 0.078 MHz to 425 MHz

The following table lists the peripherals and features of RTG4.

Table 1 • RTG4 FPGA Product Family

Peripherals	Features Package	RT4G150 FC1657 and FCG1657
Logic/DSP	Maximum logic elements (LUT4 + TMR flip-flop)[1]	151,824
	Mathblocks (18-bit × 18-bit)	462
	Radiation-tolerant PLLs	8
Memory	LSRAM 24.5 kb blocks	209
	uSRAM 1.5 kb blocks	210
	Total SRAM Mbits	5.2
	uPROM kb	374
High-Speed Interface	SerDes lanes	24
	PCIe endpoints	2
	DDR SDRAM controllers with ECC	2
	SpaceWire clock and data recovery circuits	16
User I/Os	MSIO (3.3 V)	240
	MSIOD (2.5 V)	300
	DDRIO (2.5 V)	180
	Total user I/Os (Non-SerDes)	720

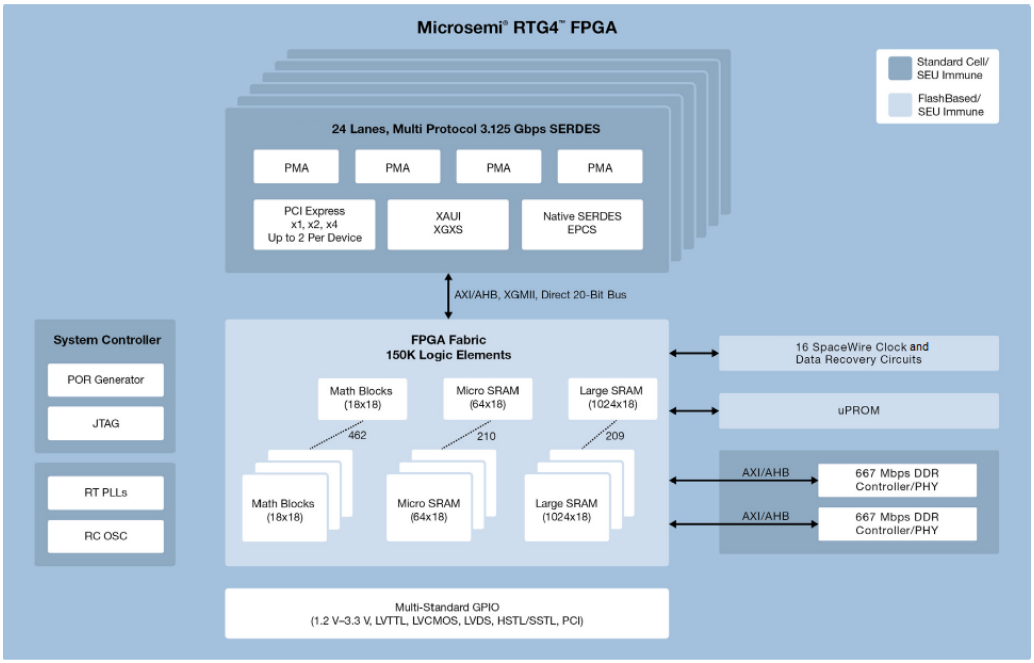
Note:

1. The maximum number of logic elements varies on the basis of the utilization of DSP and memories in the design.

2.2 RTG4 Device Block Diagram

The following figure shows the RTG4 FPGA block diagram.

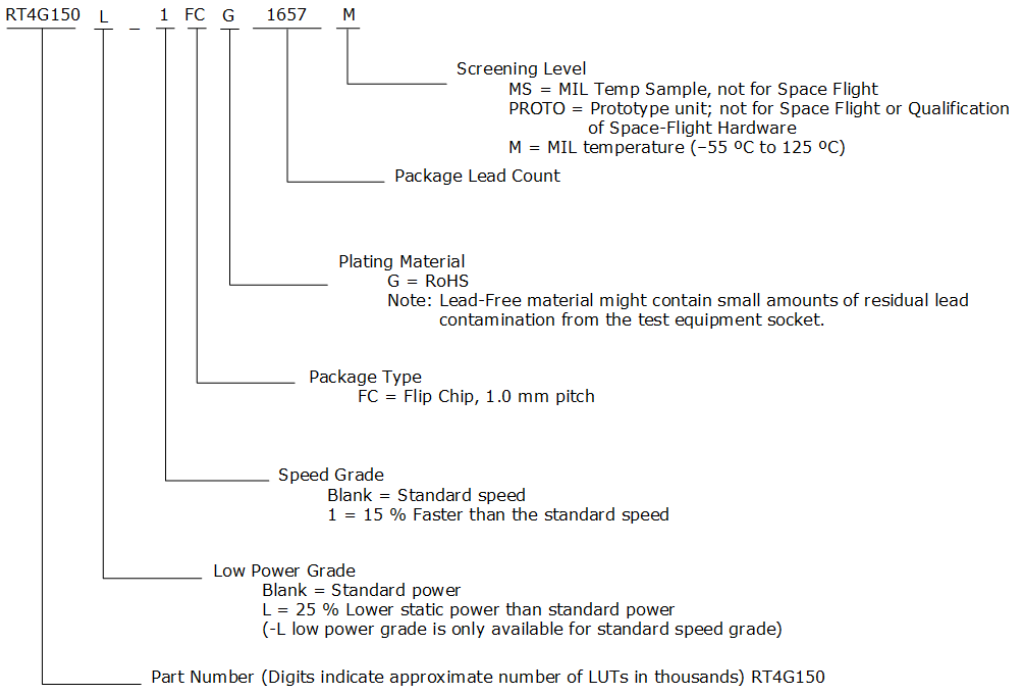
Figure 1 • RTG4 Device Block Diagram



2.3 RTG4 Ordering Information

The following figure shows the ordering codes of RTG4 FPGA in plastic package.

Figure 2 • Ordering Information

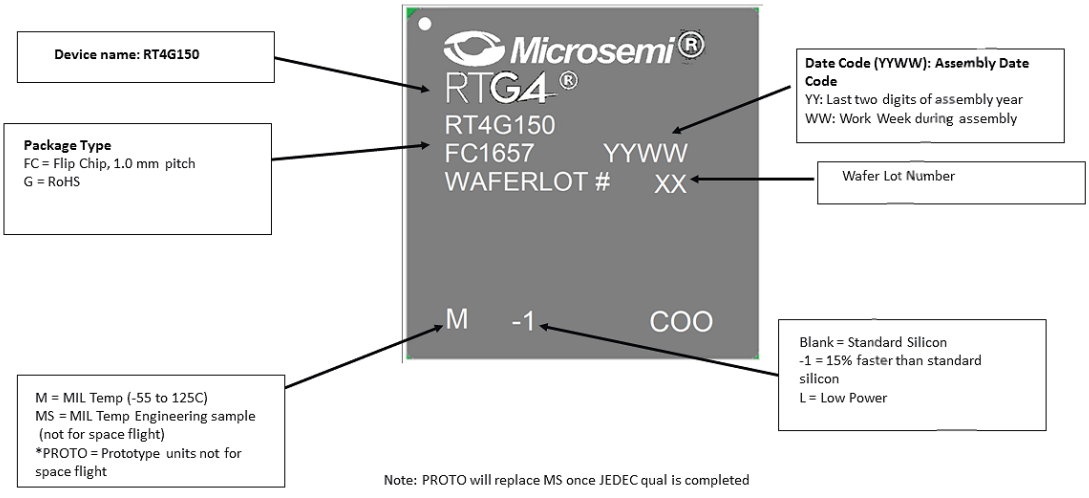


Contact your local Microsemi SoC Products Group representative for device availability.

2.4 Marking Specifications

Microsemi marks the part number on the top of every RTG4 device along with other device specifications, as shown in the following figure.

Figure 3 • RTG4 Device Marking Specifications



3 RTG4 Device Family Overview

RTG4 FPGAs integrate Microsemi's fourth-generation flash-based FPGA fabric and high-performance interfaces, such as SerDes on a single chip, while maintaining the resistance to radiation-induced configuration upsets in harsh radiation environments. For example, space flight, high-altitude aviation, medical electronics, and nuclear power plant control. The RTG4 family offers up to 151,824 registers, which are hardened by design against radiation-induced SEUs.

Each RTG4 logic element includes an LUT4 with fast carry chains providing high-performance FPGA fabric up to 300 MHz. There are multiple embedded memory options and embedded multiply-accumulate blocks for digital signal processing (DSP) up to 300 MHz. A high-speed serial interface provides 3.125 Gbps native SerDes communication, while double data rate DDR2/DDR3/LPDDR memory controllers provide high-speed memory interfaces.

3.1 High-Performance FPGA Fabric

Built on 65 nm process technology, the RTG4 FPGA fabric is composed of the logic module, LSRAM, uSRAM, and mathblocks. The logic module is the basic logic element and supports the following advanced features.

- A fully permutable four-input LUT optimized for lowest power.
- A dedicated carry chain based on carry look-ahead technique.
- A separate SEU-hardened flip-flop that can be used independently from LUT. Each flip-flop has its own synchronous reset. There are up to 206 asynchronous resets that drive RTG4 flip-flops devices.

The four-input LUTs are configured either to implement a four-input combinatorial function or to implement an arithmetic function, where the LUT output is XORed with the carry input to generate the SUM output.

3.1.1 Dual-Port LSRAM

The LSRAM block is targeted for storing large amounts of data for use with various operations. Each LSRAM block stores up to 24,576 bits. It contains port A and port B data ports. The LSRAM block is synchronous for read and write operations. Operations are triggered on the rising edge of the clock. The data output ports of the LSRAM have pipeline registers, which have control signals that are independent of the SRAM's control signals. An optional EDAC is built-in based on single error correction and double error detection. EDAC is enabled to mitigate the impact of SEU in the LSRAM.

3.1.2 Three-Port uSRAM

The uSRAM block is the second type of SRAM block that is embedded in the fabric of the RTG4 devices. The uSRAM block is a three-port SRAM. It has port A and port B for read operations and port C for write operations. The two read ports are independent of each other and perform read operations in both synchronous and asynchronous modes. The write port is always synchronous. The uSRAM block stores up to 1,536 bits. These uSRAM blocks are primarily targeted for building embedded FIFOs to be used by any embedded fabric master. The uSRAM block is also used to store DSP coefficients. Optional built-in EDAC is enabled to mitigate the impact of SEU in the uSRAM.

3.1.3 uPROM Non-Volatile Memory

uPROM is a non-volatile flash memory, which uses the same flash technology as the FPGA configuration cells. uPROM is immune to memory upsets and has a TID performance beyond 100 krad, similar to the FPGA flash configuration cells. RTG4 devices have up to 374 kb of uPROM memory. uPROM can be used for power-on initialization of RAMs and embedded IPs, as well as storage for DSP coefficients. The uPROM has a read performance of 50 MHz.

3.1.4 Mathblocks for DSP Applications

The fundamental building block in any DSP algorithm is the multiply accumulate (MACC) function. The RTG4 FPGA device implements a custom 18-bit × 18-bit MACC (18 × 18 MACC) block for efficient implementation of complex DSP algorithms, such as finite impulse response (FIR) filters, infinite impulse response (IIR) filters, and fast fourier transform (FFT) for filtering and image processing applications.

Each mathblock has the following capabilities.

- Supports 18 × 18 signed multiplications natively (A[17:0] × B[17:0])
- Supports dot product, and the multiplier computes: (A[8:0] × B[17:9] + A[17:9] × B[8:0]) × 29
- Built-in addition, subtraction, and accumulation units to combine multiplication results efficiently

In addition to the basic MACC function, DSP algorithms need small amounts of RAM for coefficients and larger RAMs for data storage. RTG4 uSRAMs are suited to serve the needs of coefficient storage, while the LSRAMs are used for data storage.

3.2 High-Speed Serial Interfaces

This section describes the high-speed interfaces of RTG4 FPGAs.

3.2.1 SerDes Interface

RTG4 has six 3.125 Gbps quad SerDes transceivers, each supporting the following.

- Four SerDes/EPCS lanes (24 total SerDes lanes)
- The native SerDes interface facilitates implementation of SRIO in fabric or a 10 Gigabit media independent interface (SGMII) for a soft Ethernet

3.2.2 PCI Express

PCI Express (PCIe) is a high-speed, packet-based, point-to-point, low pin count, and serial interconnect bus. The RTG4 family has embedded high-speed serial interface blocks. Each SerDes block contains a PCIe system block. The PCIe system is connected to the SerDes block, and following are the main features supported.

- Supports ×1, ×2, and ×4 lane configuration
- Endpoint configuration only
- PCIe Base Specification Revision 2.0 (at Gen1 rate of 2.5 Gbps only)
- 5 Gbps compliant
- Embedded receive (2 KB), transmit (1 KB), and retry (1 KB) buffer dual-port RAM implementation
- Up to 2 KB maximum payload size
- 64-bit AXI or 32-bit/64-bit AHBL Master and Slave interface to the application layer
- 32-bit APB interface to access configuration and status registers of PCIe system
- Up to 3 bit × 64 bit base address registers
- One virtual channel (VC)

3.2.3 XAUI/XGXS Extension

The XAUI/XGXS extension uses four SerDes channels, operating at 3.125 Gbps to allow the user to implement a 10 Gbps (XGMII) Ethernet PHY interface by connecting the XGMII fabric interface through an appropriate soft IP block in the fabric.

3.3 High-Speed Memory Interfaces: DDR2/3 Memory Controllers

RTG4 devices have two fabric DDR (FDDR) subsystems in them. Each subsystem consists of a DDR controller, PHY, and a wrapper. Each FDDR block provides an interface to/from the FPGA fabric.

The following are the main features supported by the FDDR blocks.

- Support for LPDDR, DDR2, and DDR3 memories
- Simplified DDR command interface to standard AMBA AXI/AHB interface
- Up to 667 Mbps (333 MHz double data rate) performance for DDR2 and DDR3
- Up to 266 Mbps (133 MHz double data rate) performance for LPDDR
- Supports different DRAM bus width modes: ×8, ×16, and ×32 (or ×9, ×18, and ×36 with SECDED enabled).
- Supports DRAM burst length of 4 or 8 in full bus-width mode; supports DRAM burst length of 4, 8, or 16 in half bus-width mode
- Supports memory densities up to 4 GB
- Supports a maximum of 8 memory banks
- SECDED enable/disable feature
- Embedded physical interface (PHY)
- Read and write buffers in fully associative CAMs, configurable in powers of 2, up to 64 reads plus 64 writes.
- Support for dynamically changing clock frequency while in self-refresh
- Supports command reordering to optimize memory efficiency
- Supports data reordering, returning critical word first for each command

Each FDDR subsystem has an interface to the DDR memories. This is a multiplexed interface from the FPGA fabric, which is configured as either a single AXI 64-bit bus or two 32-bit AHB-Lite buses. There is also a 16-bit APB configuration bus, which is used to initialize the majority of the internal registers within the FDDR subsystem after reset. This APB configuration bus is mastered by a master in the FPGA fabric.

3.4 Clock Sources: On-Chip Oscillators, PLLs, and CCCs

RTG4 devices have an on-chip 50 MHz RC oscillator, which is available to the user for generating clocks to the on-chip resources and the logic built on the FPGA fabric array. The oscillator is used in conjunction with the integrated user phase-locked loops (PLLs) and CCCs to generate clocks of varying frequency and phase. In addition to being available to the user, this oscillator is used by the system controller and power-on-reset (POR) circuitry.

RTG4 devices have up to eight fabric CCC blocks and a dedicated PLL associated, with each CCC to provide flexible clocking to the FPGA fabric portion of the device. Each of the PLL and oscillator clock sources are radiation hardened to provide glitch free clocks in the system. Any of the 8 PLLs and CCCs can be used to generate fabric clocks from the base fabric clock (CLK_BASE).

3.5 Programming

RTG4 FPGAs support JTAG programming using an external programmer, such as the FlashPro4/5. In-system programming is supported through DirectC software, which enables a microprocessor to program the RTG4 device through the JTAG interface.

Note: RTG4 programming circuitry is not radiation-hardened. Contact Microsemi for the latest data regarding reprogramming in a radiation environment.

3.6 Radiation and Reliability

RTG4 FPGAs are manufactured on a low-power 65 nm process with a substantial reliability heritage.

RTG4 FPGAs are immune to radiation-induced (SEU-induced) changes in configuration, due to the robustness of the flash cells used to connect and configure logic resources and routing tracks.

No background scrubbing or reconfiguration of the FPGA is required to mitigate changes in configuration due to radiation effects. Data errors, due to radiation, are mitigated by hardwired SEU-resistant flip-flops in the logic cells and in the mathblocks. SECDED protection is optional for the embedded SRAM (LSRAM and uSRAM) and the DDR memory controllers. So, if a one-bit error is detected, it is corrected automatically. Errors of more than one-bit are detected only but not corrected. SECDED error signals are brought to the FPGA fabric to allow the user to monitor the status of these protected internal memories.

3.7 RTG4 Development Tools

This section describes the RTG4 development tools of the RTG4 device.

3.7.1 Design Software

Microsemi's Libero® SoC is a comprehensive software toolset to design applications using the RTG4 device. Libero SoC manages the entire design flow from design entry, synthesis and simulation, place-and-route, timing, and power analysis, with an enhanced integration of the embedded design flow. System designers leverage the easy-to-use Libero SoC that includes the following features.

- Synthesis, DSP, and debug support from Synopsys
- Simulation from Mentor Graphics
- Push-button design flow with power analysis and timing analysis
- SmartDebug for access to non-invasive probes within RTG4 devices. For more information about design software, see *Libero SoC*.

3.7.2 Design Hardware

Microsemi’s RTG4 development kit provides designers with an evaluation and development platform for applications, such as data transmission, serial connectivity, bus interface, and high-speed designs using RTG4 devices. The development board features an RT4G150 device, offering 151,824 logic elements in a ceramic package with 1,657 pins. RTG4 ceramic packages are pin-compatible and have the same footprint as the FCG1657 package.

The RTG4 development board includes 2 GB × 1 GB DDR3 and 2 GB of SPI flash memories. The board also has several standard and advanced peripherals, such as PCIe × 4 edge connector, two FMC connectors for using several off-the-shelf daughter cards, USB, Philips inter-integrated circuit (I^2C), gigabit Ethernet port, serial peripheral interface (SPI), and UART. A high precision operational amplifier circuitry on the board helps to measure the core power consumption by the device. There is a FlashPro programmer embedded on the board, allowing programming of the RTG4 FPGA through the JTAG interface.

For more information about kits and boards, see *Dev Kits and Boards*.

3.7.3 IP Cores

Microsemi offers many soft peripherals that can be placed in the FPGA fabric of the device. These include Core1553, CoreJESD204BRX/TX, CoreFIR, CoreFFT, and other DirectCores.

For more information about IP cores, see *IP Cores*.

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