RADIATION CHARACTERISTICS OF FIELD PROGRAMMABLE GATE ARRAY USING COMPLEMENTARY-SONOS CONFIGURATION CELL

J. J. Wang, N. Rezzak, F. Hawley, G. Bakker, J. McCollum, and E. Hamdy
Microchip
San Jose, CA

Abstract

Total ionization dose (TID), single-event upset (SEU) and single-event latch-up (SEL) of a new 28 nm SONOS-based field-programmable gate-array (FPGA) are tested by gamma ray and heavy-ion radiation. Results are evaluated for its applications to space electronics. For TID, the propagation delay of a 4000 inverter chain is tested and passed 300 krad(SiO_2). The test for the worst case of combining TID and long-term retention effects is confirmed by performing retention before TID. For SEU, the Weibull parameters of static-random-access memory (SRAM) and flip-flop are acquired. The lowest SEL threshold occurred in one bank of IO is in excess of 63 MeV-cm^2/mg, when biased at 2.625 V.

Introduction

Right now in the electronics market, PolarFire, using 28 nm SONOS (Silicon Oxide Nitride Oxide Silicon) based technology and manufactured by Microchip FPGA business unit, is the highest performance and lowest power non-volatile and reprogrammable Field Programmable Gate Array (FPGA) [1]. Preliminary testing of total ionizing dose (TID), single event upset (SEU) and single event latch-up (SEL) are performed; results are discussed in the following sections.

Based on existing knowledge, one concern is the total ionizing dose (TID) effects on the long-term retention of the SONOS configuration cells. Although it is manageable in NOR Flash memories [2], using SONOS cell as the data-pass gate in FPGA is much more challenging because of the potential performance degradation. The mechanism is very similar to using NFG (n-type floating gate) in the floating gate technology [3]. Fortunately the same solution in the floating gate case, using a complementary P-channel SONOS (PSONOS) and N-channel SONOS (NSONOS) pair as the control gate [4] to switch on-off of a NMOSFET (N-channel Metal Oxide Silicon Field Effect Transistor) data-pass gate can resolve the issue.

Another TID problem is related to the long-term operation in many space applications. In space, TID induced degradation is added to the effects of long-term storage retention. But logistically it is not practical to perform TID irradiation in the retention testing environment because usually accelerated retention temperature is 150°C or higher that will artificially anneal out TID effects. To approximately mimic reality, two accelerated TID plus retention experiments are performed: one is performing TID testing first, e.g. irradiated to 300krad, and then followed by retention testing on irradiated samples; the other is retention testing first and then TID.

Obviously, as mentioned before, performing TID first then adding accelerated retention at 150°C or higher will artificially anneal out TID effects somewhat. However, it is treated as a control group to compare to the scenario of applying accelerated retention test first and then followed by TID test.

In addition, for the newly-introduced SONOS-based reprogrammable FPGA Polarfire, the first order single event effects (SEE) investigation presented in this paper includes configuration single event upsets (SEUs), SEUs in memories and flip-flops, and also single event latch-up (SEL) in the chip.

TID Effects on Complementary SONOS Cell

Figure 1 shows a SONOS configuration-cell or "SONOS cell" for short. It has a PSONOS on the top and an NSONOS at the bottom to control the switch at "ON" or "OFF" state. The PMOSFET (P-channel MOSFET) and NMOSFET, with gate tied-off to ground and V_{DD}, function as resistors to reduce the gate-to-drain voltage stress that can cause long-term reliability issues.

The construction of the SONOS cell is a small variation of the cell used in previous generation, RTG4 [4]. Its performance will be maintained in TID environment because the data path control, the switch gate, has good TID tolerance due to its thin gate oxide.

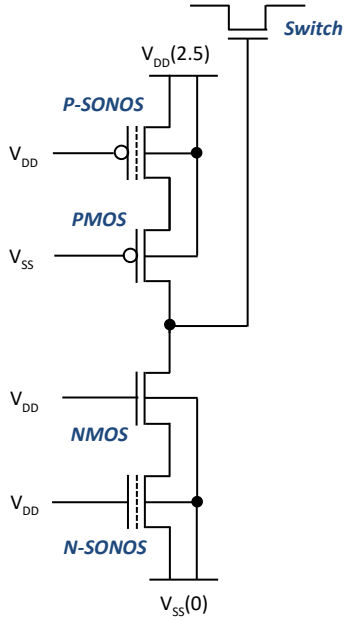

Fig. 1. Schematic of typical C-SONOS cell.

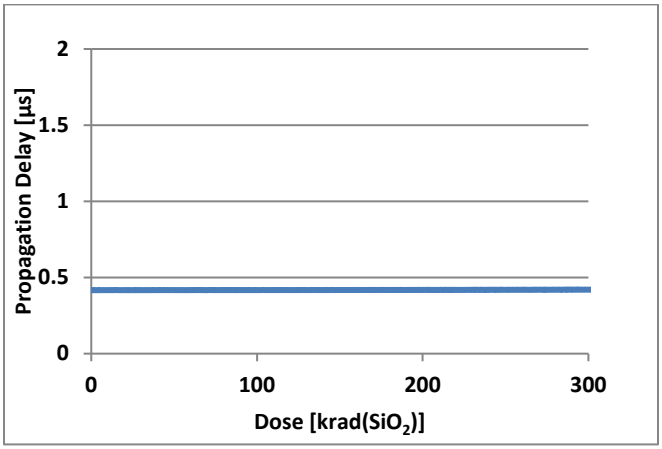

Fig. 2 Propagation delay versus total dose of 4000-inverter chain.

The TID effects on Flash-based FPGA are evaluated by measuring the propagation delay through a long chain of inverters [4]. The experiment used a 4000-inverter chain programmed into a Device-Under-Test (DUT). The result in Figure 2 shows that the degradation is negligible up to 300 krad(SiO_2), proving the expected high TID tolerance of the complementary-SONOS cell.

Retention testing combined with TID testing on Complementary SONOS Cell

The DUT choice is the MPF300. Two combined-effects tests are performed. The first performs retention at 160°C for total 1000 hours, and then adds gamma-ray irradiation total dose testing up to 300 krad(SiO_2). The second applies total dose to 300 krad(SiO_2) and then adds retention at 160°C for total 1000 hours.

The threshold voltage V_T is measured on every SONOS cell, both P-type and N-type, in time steps of 24, 48, 120, 160, 240, 480, and 1000 hours during retention and total dose steps of 100, 200, and 300 krad(SiO_2) during TID.

PSONOS V_T distribution data are plotted in Figure 3 and 4. Note that at each step, measurements are performed twice to make sure that there is no disturb during measurement. Since the degradation is defined by the merging of two states, Figure 3 clearly shows that retention-first shows more severe degradation than the TID-first degradation in Figure 4.

NSONOS V_T distributions in Figure 5 of retention first and in Figure 6 of TID first have less difference in the merging of V_T distribution. However, comparing the horizontal separation between high and low V_T distributions in these Figures, at a particular cell population level the retention-first has narrower separation and therefore more severe degradation.

Figure 3 and 4 shows the results of retention and TID induced V_T shift of PSONOS and NSONOS respectively. As mentioned before each step is measured twice, 24_1 and 24_2 stand for the first and second measurement after 24 hours retention. At every step the data of two measurements overlap, indicating negligible disturbs.

Finally, the overlap of V_T distribution of PSONOS cells is not severe enough to cause functional failures. The operation of the configuration cell depends on both PSONOS and NSONOS. As long as the pair in the same cell, e.g. Figure 1, functions properly, there are no failures.

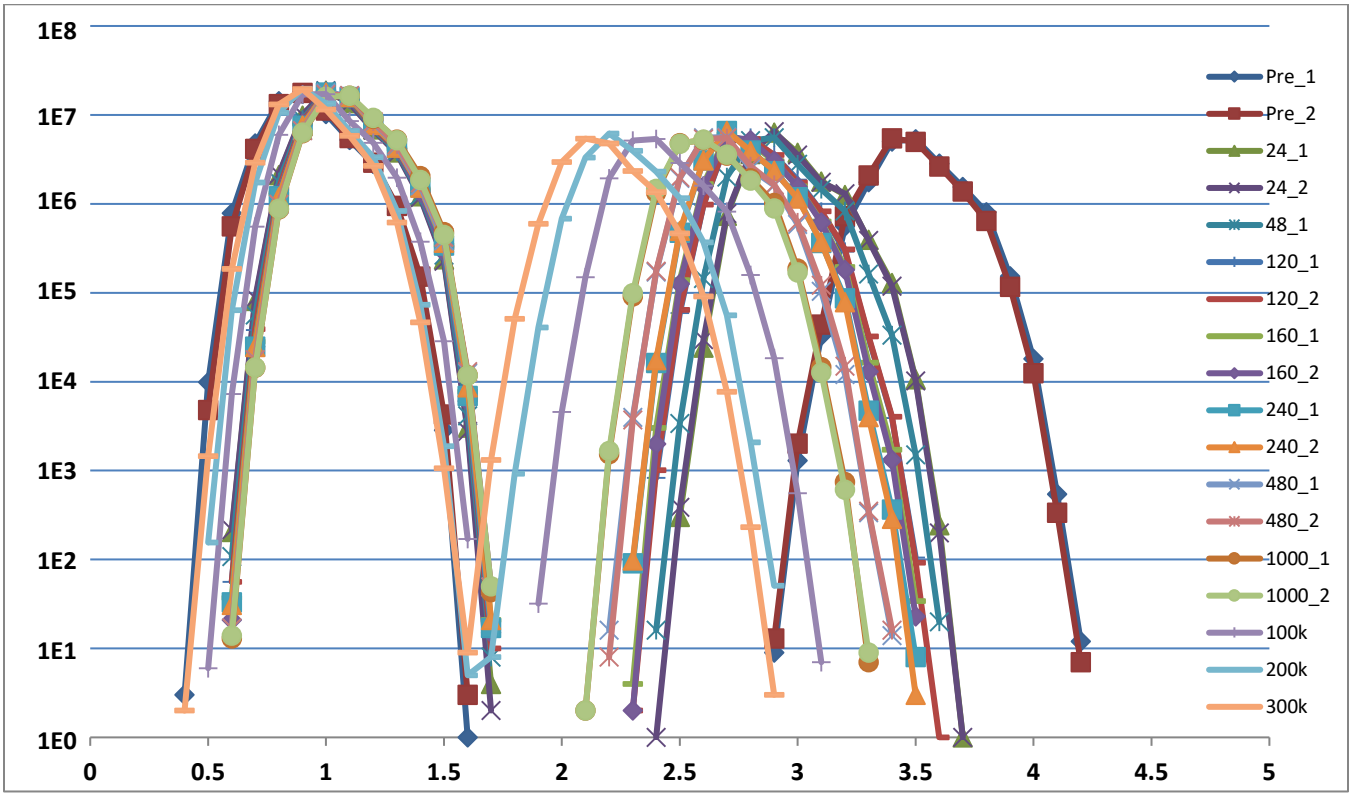

Fig. 3 PSONOS V_T distribution of first retention then TID test: ordinate shows number of cells and abscissa cell V_T (volt).

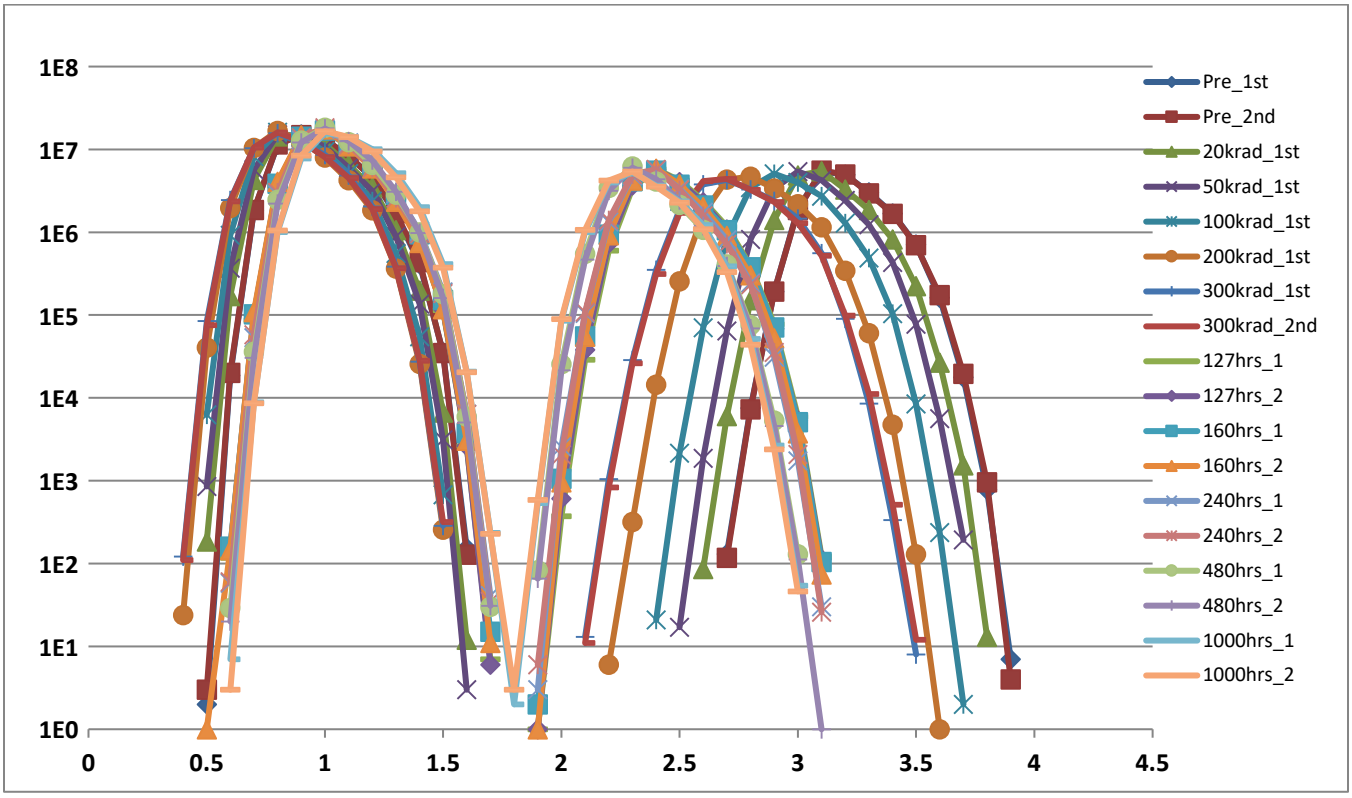

Fig. 4 PSONOS V_T distribution of first TID then retention test: ordinate shows number of cells and abscissa cell V_T (volt).

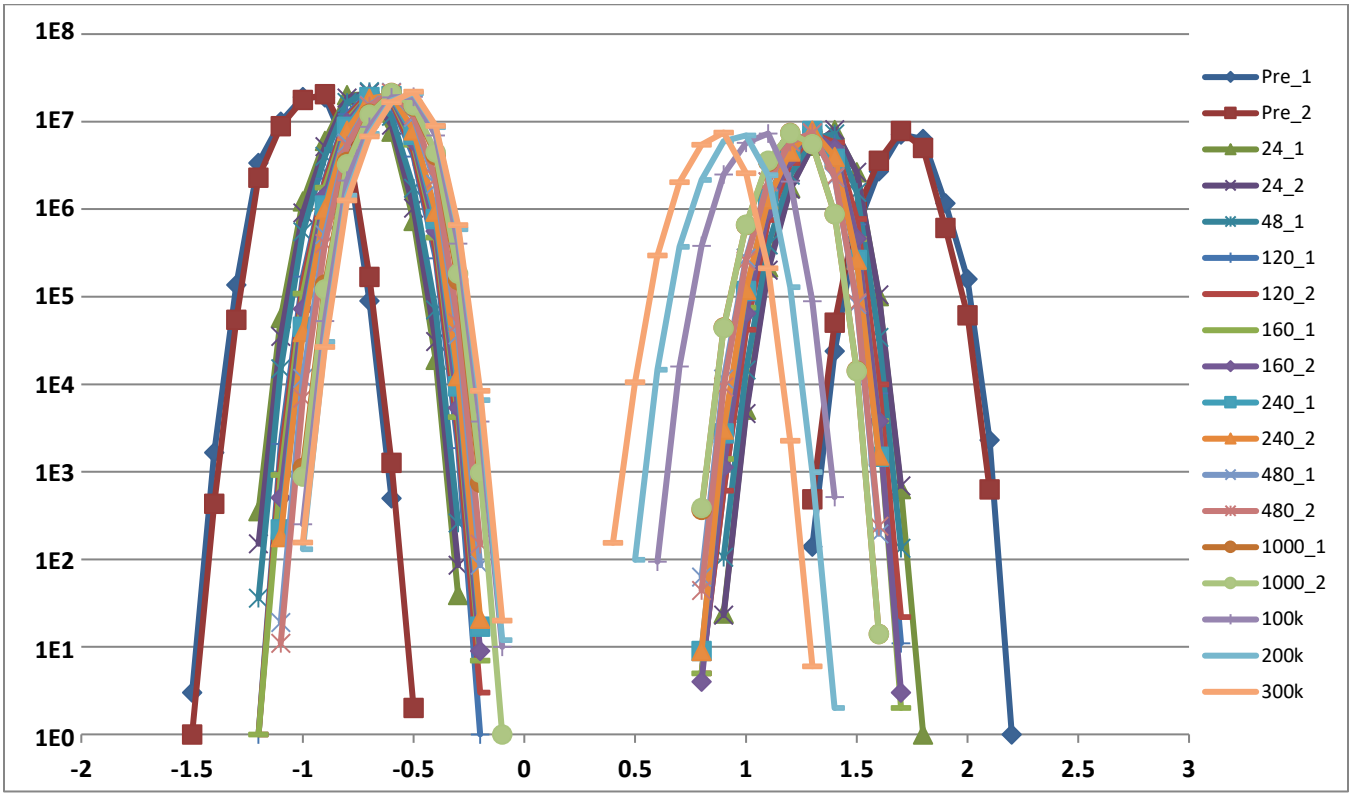

Fig. 5 NSONOS V_T distribution of first retention then TID test: ordinate shows number of cells and abscissa cell V_T (volt).

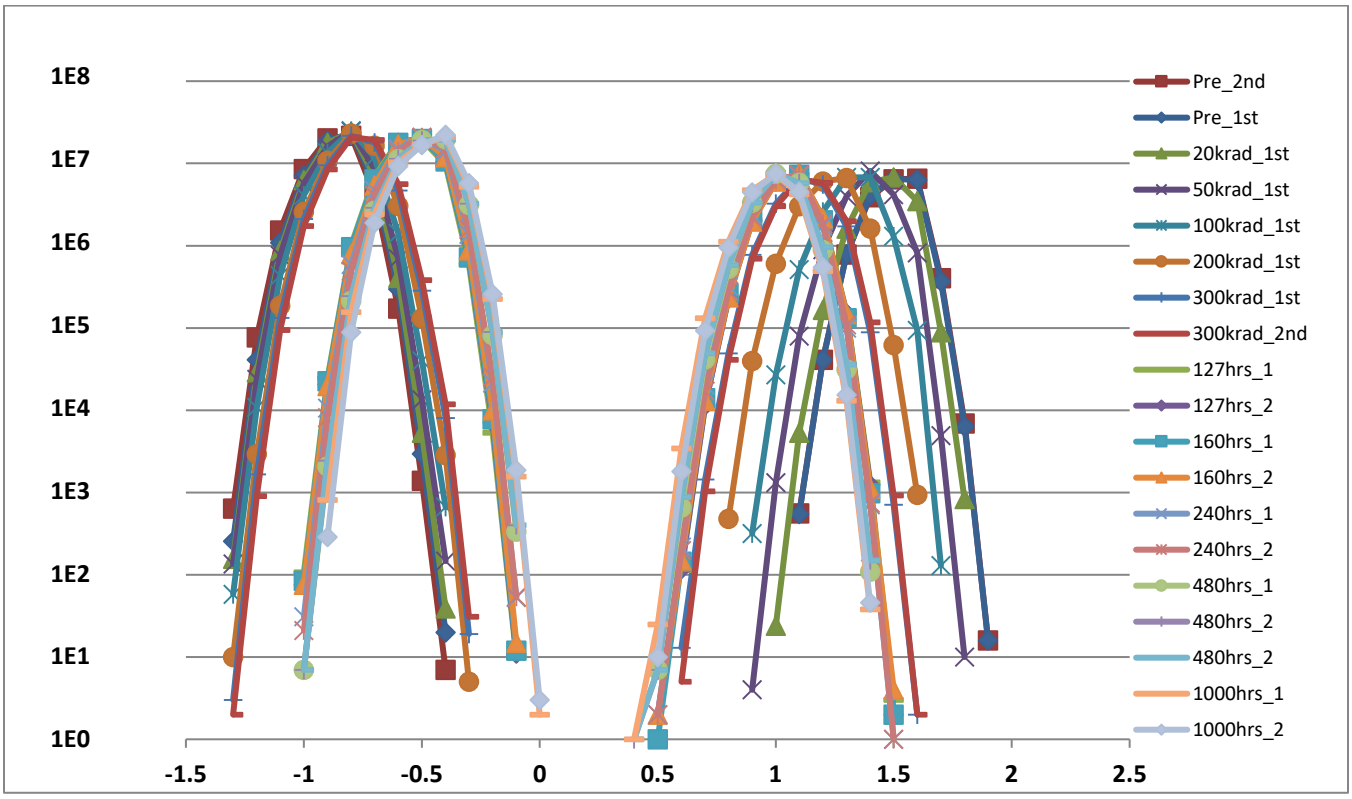

Fig. 6 NSONOS V_T distribution of first TID then retention test: ordinate shows number of cells and abscissa cell V_T (volt).

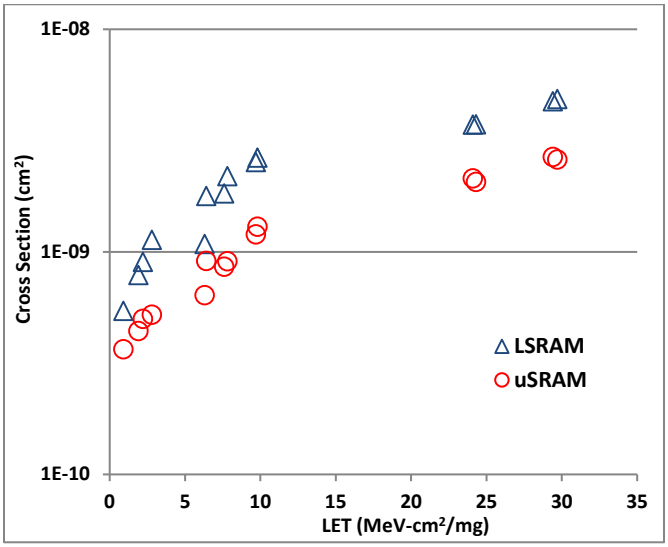

Fig. 7 SEU cross-section versus LET of µSRAM and LSRAM.

Table 1: Weibull Parameters

Circuit	σ (cm²)	LET_{TH} (MeV-cm²/mg)	W (MeV-cm²/mg)	S
µSRAM	3×10^{-9}	0.1	12	1.3
LSRAM	5×10^{-9}	0.1	11	1.3
FF All One	5×10^{-9}	0.5	11	1.3
FF All Zero	4×10^{-9}	0.5	10	1.3
FF CB	7×10^{-8}	0.1	32	1.6
FF CB-Slow	3×10^{-8}	0.1	28	1.5

Preliminary SEE Test Results

SEE testing performed so far includes configuration SEU, SEU of D-type flip-flops (DFF) in the logic fabric, SEU of the µSRAM and LSRAM which are fabric storage resources, and chip level SEL. Testing is performed in the 25 MeV/n heavy-ion beam at TAMU and results are presented in the following sections.

The DUT is MPF300 which features 300,000 Logic Elements, each element comprises a 4-input LUT (Look Up Table) with a DFF. It also has 952 LSRAM blocks each with 20 Kb and 2,772 µSRAM blocks each with 768 bits.

Configuration SEU

Single event effects are studied in a variety of experiments using the heavy-ion beam at TAMU. The presence of configuration upsets would manifest as persistent functional failures in the devices under test. A total fluence in excess of 5.0×10^{-7} ions/cm² is accumulated at LET levels up to 82.1 MeV.cm²/mg. No configuration upsets are detected.

µSRAM and LSRAM SEU

Figure 7 shows the SEU data of µSRAM and LSRAM. Their Weibull parameters are listed in Table 1.

CREME96 is used to compute the orbital error rates in GEO (Geosynchronous Earth Orbit), at solar min and with 100 mils of Al shielding. The orbital error rate for µSRAM is 4.44×10^{-8} upset/bit/day, and for LSRAM it is 9.21×10^{-8} upset/bit/day.

Flip-Flop SEU

Figure 8 shows the heavy-ion SEU data of DFF, with Weibull parameters listed in Table 1. Four different input data patterns are used: All zero, all one, a checkerboard pattern in which data alternates every clock cycle, and a slow checkerboard pattern in which data alternates every second clock cycle. The orbital event rate generated by CREME96 for GEO, solar min and 100 mils of Al is 3.36×10^{-8} upset/bit/day for the all zero data pattern, and 4.07×10^{-8} upset/bit/day for the all one data pattern.

CREME96 generated event rates in GEO, solar min and 100 mils of Al of 2.28×10^{-7} upset/bit/day for the checkerboard data pattern. The checkboard-slow (CB-Slow) data pattern generated an event rate of 1.34×10^{-7} upset/bit/day .

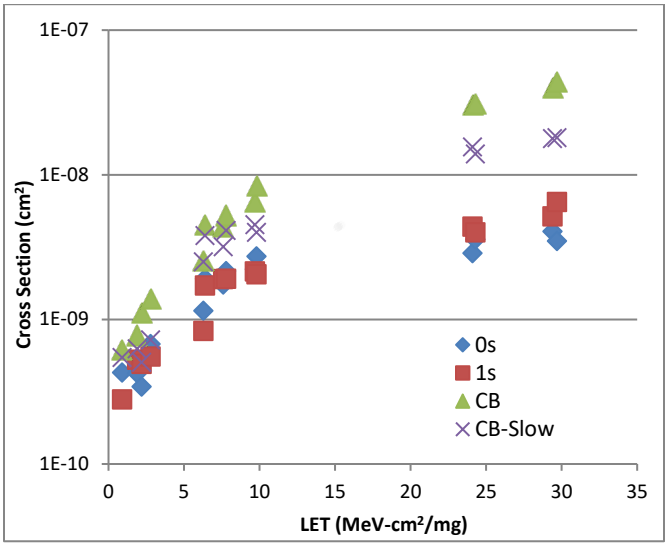

Fig. 8 SEU cross-section versus LET of DFF.

Chip SEL

The SEL sensitivity depends on applied voltage and temperature. Testing is performed with I/Os biased at 3.3V + 5% (3.465V), 2.5V + 5% (2.625V), and 1.8V + 5% (1.89V).

When tested at 100°C with I/Os biased at 3.465V, SEL is detected at LET levels of 48 MeV-cm^2/mg. When tested at 100°C with I/Os biased at 2.625, no LET is detected at LET of 63 MeV-cm^2/mg. SEL is detected at 68.5 MeV-cm^2.mg, therefore the measured LET threshold is between 63 and 68.5 MeV-cm^2/mg. When tested at 100°C with I/Os biased at 1.89V, no SEL is detected in testing, which is performed at LET levels up to 82.1 MeV-cm^2/mg.

Depending on the decoupling capacitance present on the I/O supply, the SEL may or may not be destructive. In testing, with the amount of capacitance in compliance with the guidance in the PolarFire User Guide, the SEL is non-destructive.

Conclusions

The first SONOS-Flash based FPGA has been tested for both TID and SEE. The preliminary data show good TID tolerance. For SEE, the SEL threshold appears high enough to qualify for space applications.

The unique concern of combined TID and data retention issue is investigated by the worst case of performing elevated-temperature retention test first and followed with TID test. Preliminary studies indicate that the TID tolerance doesn't have significant degradation.

References

[1] https://www.microsemi.com/product-directory/fpgas/3854-polarfire-fpgas#documentation

[2] H. Puchner, P. Ruths, V. Prabhakar, I. Kouznetsov, and S. Geha, "Impact of Total Ionizing Dose on the Data Retention of a 65nm SONOS-Based NOR Flash," *IEEE TNS.,* vol. 61, no. 6, 2014, pp. 3005-3009.

[3] J. Wang, N. Rezzak, D. DSilva, C. Huang, S. Varela, V. Nguyen, G. Bakker, J. McCollum, F. Hawley, and E. Esmat, "Radiation Effects in 65nm Flash-Based Field Programmable Gate Array," in *FPGAs and Parallel Architectures for Aerospace Applications*, Switzerland: Springer, 2016, pp. 155-174.

[4] J. Wang, N. Rezzak, D. DSilva, J. Ja, A. Cai, F. Hawley, J. McCollum and E. Esmat, "A Novel 65nm Radiation Tolerant Flash Configuration Cell Used in RTG4 Field Programmable Gate Array," *IEEE TNS,* vol. 62, no. 6, 2015, pp. 3072-3079.

Appendix: SEU Raw Data

LET in MeV-cm^2/mg; Cross-Section in cm^2

LET	FF0	FF1	FF_CB	FF_CB_slow
0.9	4.28571E-10	2.78571E-10	6.14286E-10	5.42857E-10
1.9	4.25E-10	5.25E-10	7.75E-10	6.25E-10
2.2	3.42951E-10	4.91563E-10	1.10888E-09	5.02995E-10
2.8	6.72495E-10	5.52407E-10	1.39303E-09	7.2053E-10
6.3	1.14226E-09	8.30737E-10	2.54413E-09	2.49221E-09
6.4	1.9031E-09	1.71132E-09	4.48483E-09	3.79146E-09
7.6	1.73551E-09	1.89552E-09	4.33263E-09	3.17562E-09
7.8	2.15517E-09	1.90965E-09	5.23789E-09	4.11938E-09
9.7	2.21607E-09	2.14681E-09	6.5097E-09	4.50139E-09
9.8	2.72374E-09	2.0428E-09	8.31712E-09	3.98833E-09
24.1	2.86338E-09	4.36324E-09	3.02018E-08	1.5544E-08
24.3	3.56738E-09	3.99207E-09	3.08041E-08	1.38732E-08
29.4	4.05186E-09	5.15166E-09	3.99398E-08	1.77124E-08
29.7	3.46962E-09	6.47037E-09	4.3886E-08	1.80045E-08
29.8	1.05556E-08	1.16667E-08	0.0000001	3.97222E-08
30.37	7.88177E-09	1.03448E-08	8.02956E-08	4.66749E-08

LET	uSRAM	LSRAM
0.9	3.65E-10	5.44E-10
1.9	4.42E-10	7.86E-10
2.2	5E-10	9.03E-10
2.8	5.22E-10	1.13E-09
6.3	6.39E-10	1.09E-09
6.4	9.12E-10	1.78E-09
7.6	8.58E-10	1.83E-09
7.8	9.08E-10	2.19E-09
9.7	1.2E-09	2.53E-09
9.8	1.3E-09	2.65E-09
24.1	2.14E-09	3.73E-09
24.3	2.06E-09	3.75E-09
29.4	2.67E-09	4.76E-09
29.7	2.6E-09	4.86E-09
29.8	5.95E-09	1.09E-08
30.37	5.36E-09	7.94E-09