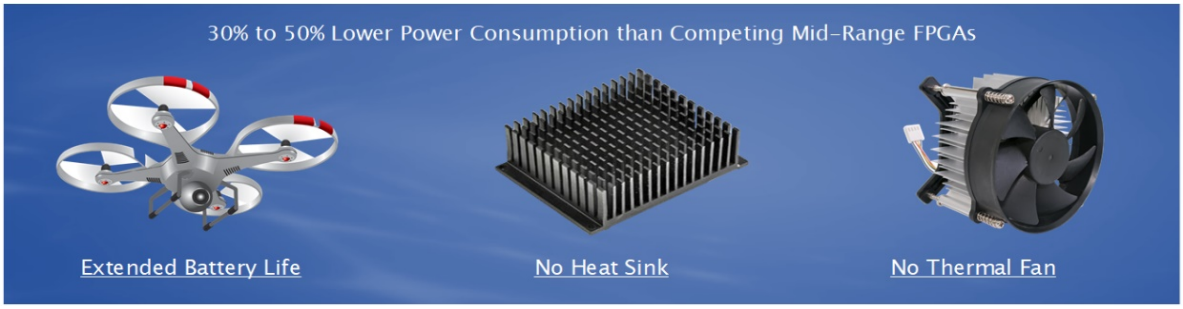
Welcome to Issue 10 of FPGA & SoC TechBytes Newsletter. Since our last issue we've kicked off our Smart Embedded Vision initiative in response to the growing need for solutions that enable compute-intensive, vision-based systems increasingly being integrated by our customers at the network edge. We've also released the latest version of our Libero® SoC Design Suite, which includes production timing and power for all PolarFire® devices. We are also delivering updates to the Renode™ platform for the PolarFire SoC FPGA with the latest release of the SoftConsole software development environment. Please read on for more details, and feel free to pass TechBytes on to your colleagues.

Microchip Launches Smart Embedded Vision Initiative

We launched the Smart Embedded Vision initiative to help you accelerate your designs by providing solutions for designing intelligent machine vision systems with our low-power PolarFire FPGAs. These FPGAs offer 30–50% lower total power over competing Static Random-Access Memory (SRAM)-based mid-range FPGAs. With family members ranging from 100K to 500K Logic Elements (LEs), they provide five to 10 times lower static power, making them ideal for a new range of compute-intensive edge devices, including those deployed in small form-factor, thermally constrained environments.



The Smart Embedded Vision initiative provides a suite of FPGA offerings that includes IP, hardware and tools for low-power, -form-factor machine vision designs across the industrial, medical, broadcast, automotive, aerospace and defense markets. Available through the Libero SoC Design Suite, all IP can be implemented on the PolarFire FPGA Video and Imaging Kit, the evaluation platform for Smart Embedded Vision designs.

Click here to visit the Smart Embedded Vision web pages for details on IP cores supporting Serial Digital Interface (SDI), MIPI, SLVS, HDMI, CoaXPress®, and much more.

Watch the Smart Embedded Vision Webcast

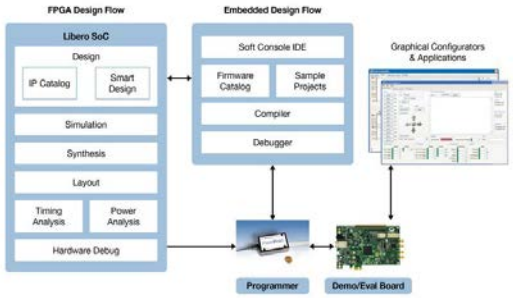
If you'd like to learn more about Smart Embedded Vision, you can watch our webinar with OpenSystems media. Enabling Intelligence at the Edge with Low-Power FPGAs will give you an overview of how low-power FPGA can enable high computing and data throughput for machine vision applications thermally constrained by small form factors. We'll detail requirements for these applications, and how the Microchip PolarFIre solutions give designers
the imaging and AI IP needed to implement their designs. Click here to watch the webcast on demand.

Kick Start Your Designs with PolarFire FPGA Development Kits

PolarFire FPGA development kits are user-friendly evaluation platforms built for quick prototyping, demonstrating specific applications, and analyzing the features and capabilities of the selected family of PolarFire FPGAs. Development is simple with a rich collection of easily accessible demonstration guides, application notes and sample designs. The PolarFire FPGA Video and Imaging Kit offers specific peripherals and components to implement applications that span across Smart Embedded Vision applications such as machine vision, thermal imaging, gaming, video surveillance, robotics, machine learning and Human-Machine Interfaces (HMIs). With onboard DDR4, DDR3, SPI-flash and a wide variety of connectors, the PolarFire FPGA Evaluation Kit is well suited for high-speed transceiver evaluation, 10 Gb Ethernet, JESD204B, CPRI, BMR and more. The PolarFire FPGA Splash Kit provides general-purpose interfaces for evaluation and development of a broad range of generic functions. For more information visit the PolarFire FPGA Development Kits page.

Libero SoC Design Suite v12.2 Release Update

We're delivering production timing and power data for all PolarFire FPGA devices with the release of the Libero SoC Design Suite v12.2. The new release also offers production timing for RTG4 RT4G150 352-CQFP (STD and –1) and RT4G150L 352-CQFP (STD) devices. Runtime reductions include up to 20% for timing for PolarFire devices; 20% in high effort place and route for larger RTG4™, SmartFusion®2 and IGLOO®2 FPGA designs and 20% for simulation. For quality of results, expect an average increase of 5% for PolarFire designs and 8% for large RTG4, SmartFusion2 and IGLOO2 FPGA designs.



This release also introduces a new 'License Selector UI' to show the detailed list of available Libero SoC Design Suite licenses and provides an option to select the required license before invoking the software tool. It also introduces programming and debug support for FlashPro 6 programmer to reduce the programming time to one minute.

Libero SoC USB Dongle License Discontinuation

Mentor Graphics, the vendor of the ModelSim® tool, has discontinued support for the Libero SoC Design Suite USB dongle license. As a result, we are announcing the discontinuation of the USB dongle license for Gold, Platinum, Gold Archival, and Platinum Archival licenses. Users of the Libero SoC Design Suite standalone USB dongle license are not impacted by this discontinuation. For more details, refer to *PDN 19017*.

SoftConsole v6.1 Delivers Renewed Renode Platform

Version 6.1 of the free SoftConsole software for bare-metal and RTOS-based development with soft core and hard CPUs on Microchip's FPGAs is now available. SoftConsole v6.1 delivers the latest Renode embedded development platform for designs targeting the RISC-V based PolarFire SoC architecture. With the new version, we've refined and added PolarFire SoC peripheral models, as well as macros to support bridging from the device's GbE transceivers with the host network. Launching debug is simplified, and Linux® OS users can now use a standard web browser with their Wireshark® network protocol analyzer to monitor the network traffic inside the emulation. The new modularized Renode infrastructure enables you to separate generic and reusable platform scripts, and the toolchain updates improve your productivity. Click here for resources to learn more and download SoftConsole v6.1.

Learn More About the Renode Platform

We've been conducting a series of monthly webinars to help you get started with the PolarFire SoC FPGA, the world's first RISC-V based SoC FPGA, to create fully deterministic, real-time systems alongside the Linux operating system. We introduce you to the free and open Renode development platform from Mi-V partner Antmicro that is available with our SoftConsole software development environment. You will see demo applications, learn how to create projects, and find out how to set up and configure your own systems targeting the new SoC FPGA architecture. Click here to view on-demand sessions and to sign up for upcoming sessions.

Register for the RISC-V Summit

Join us and our Mi-V ecosystem partners for the second annual RISC-V Summit being held at the San Jose Convention Center in San Jose, CA, on December 10–12. Registering for the summit will give you access to in-depth technical content that dives deep into the RISC-V architecture, commercial and open-source implementations, software and silicon, vectors and security, applications and more. You'll also have an opportunity to listen to visionary speakers and check out the exhibition floor where you'll be able to visit Microchip and many other technology leaders driving the RISC-V movement. Click here to lean more and register for the RISC-V Summit.

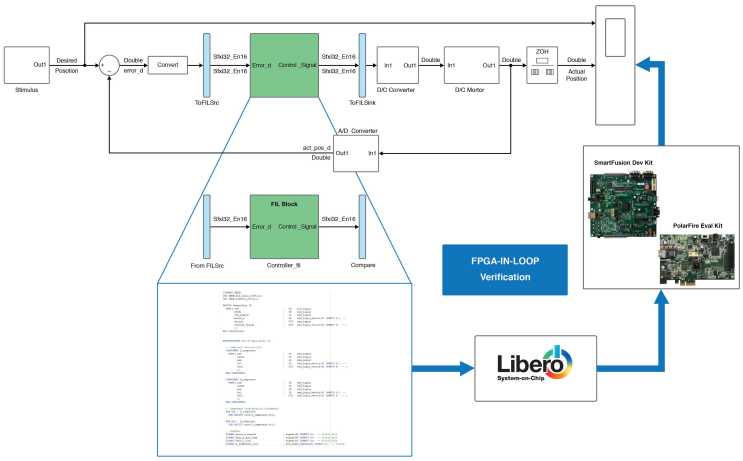
Integrated FPGA-in-the-Loop Workflow with MATLAB® and Simulink® Supports PolarFire, RTG4 and SmartFusion2 FPGA Development Kits

System-level engineers widely use MATLAB and Simulink to develop algorithms targeting FPGAs. Using MathWorks®' HDL Coder™ and HDL Verifier™, engineers can implement their MATLAB and Simulink designs directly onto FPGA boards and connect these boards directly to MATLAB and Simulink system-level test benches. This helps engineers in validating mission-critical systems for aerospace and defense applications.

The new integrated FPGA-in-the-loop (FIL) workflow with MathWorks' HDL Coder and HDL Verifier enables you to automatically generate test benches for Hardware Description Language (HDL) verification, including VHSIC Hardware Description Language (VHDL) and Verilog, providing rapid prototyping and verification of designs.

The new workflow, available in MATLAB's R2019A release, enables you to integrate MathWorks' MATLAB, a multi-paradigm numerical computing environment, and MathWorks' Simulink, a graphical programming environment, with our PolarFire FPGA and SmartFusion2 system-on-chip (SoC) FPGA development boards, which allows the stimulation of designs through FIL verification using the Libero SoC Design Suite.

The FIL verification workflow enables you to analyze the results back in MATLAB and Simulink. Delivering the FIL feature for Microchip boards with MATLAB and Simulink, the collaboration provides a hardware support package and an integrated workflow from algorithms to implementation. Leveraging MathWorks' HDL Verification, enabled by Microchip's Accelerate Ecosystem, makes Microchip's FPGAs ideal for a wide variety of applications within the aerospace market, including motor control and imaging, digital signal processing, communication systems, control systems and payloads.



To learn more, please watch the "Targeting Algorithms to Microsemi FPGAs using MATLAB and Simulink" webinar **here.**

Registration Open for Space Forum 2019

Please plan on joining Microchip for one of our bi-annual Space Forum events, being held in four different locations around the world this fall. Microchip's technical experts and partners will present and showcase their most innovative space-related products, capabilities and system solutions in this one-day technology forum. You will see demonstrations of how the interoperation of our latest products can accelerate your development time. You'll also gain a comprehensive understanding of how Microchip's Sub-QML and COTS-to-RT components help address the challenges of meeting system performance and reliability goals while also saving costs.

This is a must-attend space technology forum for system-level architects, R&D engineers, design and component engineers and other space industry professionals. Feel free to share this information with your space technology colleagues. Registration information will be provided soon. We look forward to seeing you there. (Click on locations to register)

October 24 – Noordwijk, Netherlands
November 13 – Virtual event, web broadcast (North America time zone) November 19 – Bangalore, India
November 21 – Ahmedabad, India

- Archived Webinars and Training -

- Enabling Intelligence at the Edge with Low-Power FPGAs
- Getting Started with the RISC-V Based PolarFire SoC FPGA Webinar Series
- FPGA in the Loop
- Mi-V Embedded Ecosystem
- SoftConsole and Renode from Antmicro
- Libero Design Suite Overview

- Upcoming Events -

- Hong Kong Electronics Fair, Hong Kong, China – October 13–16, 2019 (by appointment)
- Seoul ADEX 2019, Seoul, Korea – October 15–20, 2019
- 32nd Microelectronics Workshop, Tsukuba, Japan – October 23–24, 2019
- Space Forum - Europe, Netherlands - October 24, 2019
- MATLAB Expo, San Jose, CA – November 6, 2019
- Space Forum, US (Virtual) - November 13, 2019
- Space Forum India, Bangalore - November 19, 2019; Ahmedabad - November 21, 2019
- SPS 2019, Nuremberg, Germany – November 26–28, 2019
- RISC-V Summit, San Jose, California - December 9–12, 2019

Microchip Technology Inc.
2355 West Chandler Blvd. Chandler, Arizona,
USA 85224-6199 (480) 792-7200 |
www.microchip.com