



Welcome to Edition 26 of Microchip's Space Brief newsletter. Written for design engineers and design managers, system engineers and system architects, component engineers, radiation effects scientists and program managers in the space industry, Space Brief is a quarterly newsletter in which we aim to bring you the latest news about Microchip's radiation-tolerant and radiation-hardened products. Space Brief provides information about new products, updates on qualification and radiation testing, links to formal customer notifications and news about workshops and conferences at which Microchip will be presenting or exhibiting.

Please forward Space Brief to your colleagues, and let them know they can register to receive their own copy direct to their email inbox by clicking [here](#).

### Take the Libero SoC Survey

We're proud to announce that Libero SoC v12.0 was voted software/tool of the year in the 2019 ASPENCORE World Electronic Achievement Awards. Libero SoC v12.2 is available now with production timing and power support for all PolarFire® FPGAs, as well as production timing support for additional RTG4™ devices. The new version will give you 20% runtime improvement in high effort Place and Route for RTG4™. We also invite you to take our survey to get your feedback on existing features, and what you'd like to see from Libero SoC in the future. Please click [here](#) to take the survey.



### NEW FPGA PRODUCT

#### RT PolarFire® FPGA Helps Solve On-Board Processing Bottleneck Without Exceeding Power Budgets



In order to fulfill the mission requirements of next-generation satellites and space probes, developers of remote sensing systems are designing sensors with higher resolution, faster frame rates and more channels than ever before. However, the ability of communication links to handle the increased sensor data is not keeping pace, leaving remote sensing payload designers to look for solutions that can process data on board their spacecraft in a power-efficient and reliable manner.

Our RT PolarFire® FPGA offers a high-speed processing solution by delivering almost 500,000 logic elements, with each element comprising a D-type flip flop with a 4-input look-up table, nearly 1,500 multiply-accumulate blocks with 18 × 18 multiplication and 48 accumulation bits, 33 Mbits of embedded memory and 24 high-speed transceivers.

The RT PolarFire FPGA will be available in a hermetically sealed ceramic package designed to support qualification to QML class Q and QML class V standards. The intrinsic low power of Microchip's nonvolatile SONOS, reprogrammable configuration cells combined with the power-efficient architecture helps ease the system level cost of integrating systems in FPGAs for space flight, where power is on a limited budget and extreme thermal constraints pose system-level design challenges for developers.

The RT PolarFire FPGA meets the radiation requirements of the vast majority of space-flight systems, with total dose in excess of 100 Krad, absence of configuration upsets, and single event latch-up (SEL) thresholds in excess of 60 MeV-cm<sup>2</sup>/mg when the I/Os are operating at 2.5V, and SEL thresholds in excess of 80 MeV-

cm<sup>2</sup>/mg when the I/Os are operating at 1.8V. Flip flops can be protected with instantiated Triple Module Redundancy (TMR) where necessary using synthesis tools, and embedded SRAM can be protected with EDAC and background scrubbing where needed.

### RT PolarFire FPGA Overcomes SRAM Challenges

Two challenges exist when attempting to solve the signal processing bottleneck with SRAM-based FPGAs. The first relates to radiation effects in the SRAM FPGA configuration memory. The SRAM cells used for configuration of the FPGA are vulnerable to heavy ion and proton radiation in space, and the consequence of a radiation-induced upset can be that the FPGA ceases to function as intended. Mitigation requires complex external circuitry to repair the configuration, and this increases the system cost, mass, complexity and power consumption. The other issue is that SRAM FPGAs consume a lot of power, which creates thermal problems in the spacecraft. The RT PolarFire FPGA provides ample processing throughput while avoiding the pitfalls of SRAM FPGAs.

The reprogrammable SONOS configuration cells in the RT PolarFire FPGA are immune to configuration upsets in radiation and intrinsically consume less power than SRAM cells. Combining SONOS configuration cells with a power-efficient architecture, the RT PolarFire FPGA exhibits 40% to 50% power savings when compared to SRAM FPGAs.



Engineering models of RT PolarFire FPGAs will be available in mid-2020. Design work can begin today, targeting the commercial PolarFire FPGA family. Click [here](#) to access further information on RT PolarFire.

Contact Ken O'Neill, Director of Marketing, Space and Aviation [ken.oneill@microchip.com](mailto:ken.oneill@microchip.com) for more information

## BOARDS AND KITS

### Get Started Now with the PolarFire Evaluation Kit

Because the RT PolarFire FPGA is based on the commercial PolarFire FPGA family, developers can begin working on their designs now using the Libero® SoC Design Suite and the PolarFire Evaluation Kit. The [MPF300-EVAL-KIT](#) provides RT PolarFire FPGA users with an evaluation and development platform for applications such as data transmission, serial connectivity, bus interface and high-speed designs.



The development board features an MPF300 PolarFire FPGA with 300,000 logic elements. A development kit featuring the RT PolarFire FPGA is scheduled to be available in 2020.

Contact Ken O'Neill, Director of Marketing, Space and Aviation [ken.oneill@microchip.com](mailto:ken.oneill@microchip.com) for more information



### High -Performance, Multi-axis Motor Control for Space and Aviation Applications

Microchip's radiation-tolerant FPGAs serve as an ideal platform for the integrated motor control requirements of space and aviation applications. They offer high-performance solutions for high-speed, low latency algorithm processing, strong design security, differential power analysis (DPA) resistance and integration of complementary functions while offering steadfast performance in harsh temperature, pressure, and altitude conditions.

Microchip's motor control solution includes modular algorithmic blocks for field-oriented control (FOC) transformations, PI controller, space vector modulation, core 3 phase PWM, rate limiter, position and speed estimator, encoder interface, and stepper angle generator blocks. Reference designs are available that demonstrate multi-axis motor control solutions on the [Smartfusion2 SoC FPGA](#) and the [RTG4 FPGA](#) and [LX7720 Rad Tolerant Spacecraft Motor Controller](#).



Microchip offers ready demonstrations for [two and six-axis motor control](#), and a [quadcopter drone](#). For more information, visit [Microchip's FPGA based multiaxis Motor Control Solution!](#)

Contact Apurva Peri, Sr. Product Marketing Engineer, FPGA Group.

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### **SAMRH71 Rad-Hard Arm® Cortex®-M7 Based SoC Evaluation Kit Is Available**

The SAMRH71 microcontroller (MCU) is a unique rad-hard processor targeting space applications, derived from the SAMV71Q21 COTS automotive MCU. The SAMRH71 supports SpaceWire, 1553, CAN FD and Ethernet TSN interfaces, and provides high levels of radiation performance:

- Accumulated TID of more than 100 Krad (Si)
- Single event latch-up SEL Latch up immune up to 62 Mev
- No Single-Event Upset (SEU) Linear Energy Transfer (LET) up to 20 MeV.cm<sup>2</sup>/mg, without system mitigation
- Designed for No Single-Event Functional Interrupts (SEFI), which secures all memories' integrity
- Samples of the SAMRH71 MCU are already available in 256-pin ceramic Quad Flat Pack (QFP) packages, and a plastic BGA version is coming soon.

See more details about the SAMRH71 MCU on the Microchip website [here](#):

The SAMRH71 evaluation kit and software development environment are now fully available. The Microchip SAMRH71F20-EK Evaluation Kit is a hardware platform to evaluate the SAMRH71 MCU.

Supported by MPLAB® X Integrated Development Environment (IDE) and MPLAB Harmony embedded software development framework from Microchip, as well as other commercially available development environments, the evaluation kit provides easy access to the rad-hard SAMRH71F20 MCU and its aerospace-specific feature set and explains how to integrate the device in a custom design.

SAMRH71F20-EK Evaluation Kit Contents:

- SAMRH71 Evaluation Board
- USB cable
- Power cable



SAMRH71F20-EK description and content is available on the Microchip website [here](#):

#### **SAMRH71 Evaluation Board Features**

##### **SAMRH71F20C-7GB-E Sample**

##### **On-Board Memories:**

512 Kbytes (8-bit wide) PROM  
256 Mbits (32-bit wide) SDRAM

##### **On-Board Clock Management:**

32.768 kHz crystal  
10 MHz oscillator

##### **Communication Interfaces:**

UART emulation through USB interface  
Ethernet MAC with external IEEE® 802.3az

##### **10BASE-T/100BASE-TX Ethernet RMII PHY (KSZ8061-RND transceiver) and dedicated clock source**

Two CAN transceivers (ATA6563)  
Two SpaceWire connectors  
Two MIL-1553 connectors

##### **Embedded Debug Access:**

JTAG debug connector  
TRACE connector

##### **Extension Capability:**

Five headers compatible with Xplained mezzanine board  
Four connectors with direct access to the processor pins

##### **On-Board End User Interface**

One mechanical reset button  
Three mechanical user push buttons  
Four user LEDs  
One pin for NMIC  
One LCD edge connector

##### **12V Power Supply:**

Jack connector  
LED indicator for 12V power supply

Refer to AN3213: Getting Started with the SAMRH71 Microcontroller for information about hardware and software tools, including a software example for a basis application: Click [here](#).

Ordering part number: SAMRH71F20-EK



Please contact Nicolas Ganry, Product Marketing Manager, Aerospace Marketing at [nicolas.ganry@microchip.com](mailto:nicolas.ganry@microchip.com)

## PRODUCT NEWS

### RTG4 FPGAs Achieve First Flight Heritage

Flight heritage is critical to proving the flight worthiness of new space products and is essential in many space programs' requirements. With the successful launch of the [Mission Extension Vehicle-1 \(MEV-1\)](#) on October 9, 2019, RTG4 FPGAs are on board performing various functions in a single-board computer, a thermal interface unit and a video processing unit on this first-of-its-kind servicing spacecraft. MEV-1's goal is to extend the life of target satellites that have run out of fuel but are otherwise fully functional.

The MEV-1 spacecraft will dock with target satellites to maintain attitude and orbit control of the combined vehicles so that pointing and station-keeping needs are met, allowing the target satellites to continue their mission for several more years. RTG4 FPGAs deliver the density and performance required by a single-board computer and combine high-speed signal processing with special built-in radiation mitigation techniques to keep systems operational in the harsh radiation environments the MEV-1 will navigate.



Source: Northrop Grumman

As an integral component in MEV-1, the RTG4 FPGAs are the first and only QML Class V-qualified FPGAs to achieve flight heritage, elevating the devices' Technology Readiness Level (TRL) to nine. RTG4 FPGAs' first flight heritage adds to existing designations the devices have achieved, including QML Class V, QML Class Q and MIL-STD-883 Class B qualifications.



Contact Minh Nguyen, Sr. Product Marketing Manager, FPGA Group at [Minh.Nguyen@microchip.com](mailto:Minh.Nguyen@microchip.com) for questions and comments.

### Ultra-Stable Oscillators for Latest GPS III Satellites "Vespucci" and "Magellan"

The launch of GPS III Space Vehicle 01 (Vespucci) on December 23, 2018, and Space Vehicle 02 (Magellan) on August 22, 2019, from Cape Canaveral are notable because they each rely on a pair of our 9500B Series Ultra-Stable Oscillators (USOs) as a reference oscillator inside the Harris Space Systems Mission Data Unit (MDU). The MDU is the main command and control center for the navigation mission, distributing precise timing throughout the GPS space vehicle for use by other payloads. The 9500B USO provides short-term stability while an Excelitas Rubidium Atomic Frequency Standard (RAFS) provides long-term stability. The U.S. Air Force will eventually launch up to 32 GPS III satellites.



GPS III Satellite (Source: Lockheed Martin)

GPS has become a critical utility to billions of users worldwide. GPS is essential to the economy and defense but can be vulnerable to accidental or malicious jamming that could jeopardize military missions. GPS III helps address these concerns.

GPS III satellites will provide three times better accuracy and up to eight times improved anti-jamming capabilities, and will boast a 15-year design life, twice as long as some of the current GPS satellites. GPS III's new L1C civil signal will also make it the first GPS satellite to be interoperable with other international Global Navigation Satellite Systems (GNSS).



9500B Master Reference Oscillator

The 9500B Series of ultra-stable oscillators produces a highly stable, low-noise reference frequency output and is built on our strong space flight heritage developed over the past 40 years. Particularly suited to space applications, the 9500B Series delivers the best stability performance available in a commercial product.

#### Key features include:

- 4-100 MHz, 5 MHz standard; Note: contact for alternate frequency requirements
- Short-term stability for  $t = 1-100$  secs  $< 3.0 \times 10^{-13}$

- Space-qualified and radiation rated to >100 K Rad (Si), ELDERS, neutron and SEE hardened
- Power consumption: <3.6W @ 25°C
- Size: 8.95 × 3.87 × 3.27 inches
- Frequency aging <5.0 E-11/day, <1.0 E-8/yr
- Temperature range: -24°C to +60°C

While the Model 9500B provides the best stability performance available in a commercial product, Microchip offers a full range of space-qualified crystal oscillators to meet your requirements. For Low Earth Orbit (LEO) applications, Microchip recently introduced the world's first commercially available radiation-tolerant Chip Scale Atomic Clock (CSAC), providing the accuracy and stability of atomic clock technology while achieving true breakthroughs in reduced size, weight and power consumption.



For more information contact Stewart Hampton, SDA Product Line Manager at [Stewart.Hampton@Microchip.com](mailto:Stewart.Hampton@Microchip.com)

## NEW DOCUMENTATION

### New RTG4 FPGA Documents Posted

A new RTG4 FPGA datasheet Revision 6.0 was published in August 2019. In this revision, some of the key updates include production timing status for RTG4 in CQ352 package, power supply ripple recommendation, complete package thermal resistance and more. The latest datasheet version can be downloaded [here](#).



Application Note AC439: RTG4 FPGAs Board Design and Layout Guidelines and its addendum have recently been updated to include comprehensive information on power-up and power-down requirements for RTG4 FPGA family. The guidelines provided in AC439 expand on the RTG4 FPGA datasheet requirements for power sequences. AC439 Addendum provides different scenarios and their consequences when the power-up or power-down requirements are not followed. [AC439](#) and its [Addendum](#) can be downloaded from Microsemi website.

Contact Minh Nguyen, Sr. Product Marketing Manager, FPGA Group at [Minh.Nguyen@microchip.com](mailto:Minh.Nguyen@microchip.com) for questions and comments.



### Looking for the Correct Clock Oscillator to Drive an RTG4™ FPGA? Check Out App Note AN3216

Microchip application note AN3216 was formally released in September and can be downloaded from the Vectron® Space and Hi-Rel webpage [here](#).

The following Vectron space-qualified clock oscillators have been characterized and are recommended for use with RTG4 FPGA REFCLK receivers:

#### LVDS:

- **DOC203679**, Hybrid Clock Hi-Rel Standard, LVDS Output
- **DOC206903**, Hybrid Clock Hi-Rel Standard, 300 krad Tolerant LVDS Output

#### LVPECL:

- **DOC203810**, Hybrid Clock Hi-Rel Standard, LVPECL Output

#### CMOS:

- **OS-68338**, Hybrid Clock Hi-Rel Standard, CMOS Output
- **DOC206379**, Hybrid Clock Hi-Rel Standard, 300 krad Tolerant CMOS Output
- **DOC204900**, Hybrid Clock Hi-Rel Standard, High Frequency CMOS Output

#### General Recommendations and Summary

1. When an external resistor like the 200Ω termination for differential driving is used, it must be placed as close as possible to the differential receiver input pins. Otherwise, waveform and jitter can greatly be

degraded.

- The RTG4 FPGA's differential receiver must be terminated at the inputs either with an external resistor (100Ω or 200Ω) or with RTG4 FPGA On-Die Termination (ODT) for all clock driver types for best waveform and jitter performance.
- The clock oscillator driver should be placed as close as possible to the input pins of the RTG4 FPGA's receiver, to help reduce interferences and minimize reflection on the transmission line due to possible impedance mismatching.
- It is recommended to use the drivers and interface circuits listed in Table 3.

**\*\*Do not use the RTG4 FPGA's REFCLK Inputs LVDS33 and LVPECL33.**

**TABLE 4: RTG4 FPGA REFCLK Inputs and Clock Driver Matrix**

RTG4™ FPGA		VECTRON® CLOCK DRIVER					
Signal Type	REFCLK Inputs	Clock Type	Vectron Hi-Rel Standard Drawing	Radiation Tolerance (Krad)	Supply Voltage (V)	Max Freq (MHz)	Termination Circuit
Differential	LVDS25_ODT	LVDS	DOC203679	100	3.3	200	Direct interface Figure 1
			DOC206903	300	3.3	200	
	LVDS25_ODT	LVPECL	DOC203810	50 (ELDRS)	3.3	700	Figures 6, 8, and 10
	LVDS25	LVDS	DOC203679	100	3.3	200	200 Ohms Figure 3
			DOC206903	300	3.3	200	
	LVDS33	Do not use					
LVPECL33	Do not use						
Single-Ended	LVC MOS33	CMOS	OS-68338	100	3.3	100	Direct interface Figure 12
			DOC204900	100	3.3	125	
			DOC206379	300	3.3	80	
	LVC MOS25	CMOS	DOC204900	100	2.5	125	Direct interface Figure 12

**Table 4 Notes:** For differential signal application, LVDS25\_ODT (used with LVDS or LVPECL clock driver) or LVDS25 (used with LVDS clock driver and external 200-ohm termination) are the two options for RTGR. The CMOS single-ended signal solution offers the best Total Jitter and Deterministic Jitter performance (See Jitter Measurements Table 5, Table 6 and Table 7), simple direct interface and options to use either the 2.5V or 3.3V supply, but speed is limited to 100 MHz (OS-68338), 80 MHz (DOC206379) and 125 MHz (DOC204900) for the three Vectron CMOS clocks.



For further information, please contact Scott Murphy, Space Product Line Manager, Vectron Oscillator Products at [scott.murphy@microchip.com](mailto:scott.murphy@microchip.com)

**New Radiation-Tolerant FPGA and Space Solutions Brochures**

Microchip has been developing space solutions for almost six decades and has played an important role in a wide variety of space programs globally. The company has a proven track record for innovation, quality and reliability, and continues to build on that legacy with an impressive portfolio of industry-leading new products and technology innovations.

Microchip's high-reliability, low-power spaceflight FPGAs are your best design choice for low Earth orbit, deep space or anything in between. With a history of providing the most reliable, robust, low-power Flash- and antifuse-based FPGAs in the industry, we offer the best combination of features, performance and radiation tolerance. Since our last edition of Space Brief the [Radiation-Tolerant FPGAs brochure](#) and [Space Solutions](#)

Brochure were updated and published on our website. The [Radiation Tolerant FPGAs brochure](#) can be downloaded in the resources tab for all RT FPGA products. Both brochures can also be downloaded on this website:

<https://www.microsemi.com/applications/space#resources>

For questions please contact:

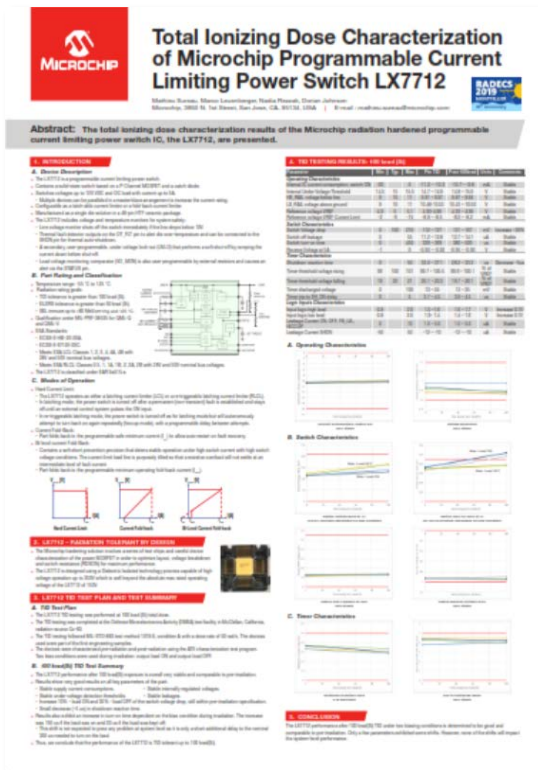
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### LX7712 TID Results Presented at RADECS 2019

Post-TID radiation characterization results on Microchip's new LX7712 Programmable Current Limiting Power Switch were presented at the recent Radiation and Its Effects on Components and Systems (RADECS) conference in Montpellier, France. The post-radiation characterization concluded that the LX7712 performance after 100 Krad (Si) TID under two biasing conditions is determined to be good and comparable to pre-irradiation.



The full report is available on the product webpage at <https://www.microsemi.com/product-directory/radiation-tolerant-devices/5550-lx7712-programmable-current-limiting-power-switch>

The LX7712 is designed for spacecraft applications and can be configured as a latch-able current limiter or a fold-back current limiter. It provides a means to turn on or off a DC load with current up to 5A and includes a solid-state P-channel MOSFET switch and catch diode. Integration allows the temperature of the switch to trigger an optional thermal shutdown.

The device can be programmed with just a few external components, and multiple devices can be paralleled in a master/slave arrangement to increase the current rating. It is packaged in a 48-pin hermetic HTF package.

The LX7712 is currently sampling with flight units available in Q2 2020.



Please contact Dorian Johnson, HiRel Product Line Marketing Manager at [dorian.johnson@microchip.com](mailto:dorian.johnson@microchip.com) for more information.

### MICROCHIP AT RADECS 2019

#### The Microchip Aerospace and Defense Group Team in the Spotlight at RADECS 2019

The RADECS Conference is the annual European scientific and industrial forum where scientists engage on the latest developments about radiation and its effects on components and systems, RADECS 2019 was held from September 16–20 in Montpellier, France. This was first time Microchip attended with a full consolidated aerospace and defense offering that included products from the Microsemi portfolio.

A number of representatives from Microchip were selected to join the organization, including David Truyen from the Aerospace and Defense Group (ADG) in Nantes as chairman, and three reviewers who included Severine Furic and Erwann Berlivet also from the ADG in Nantes and Nadia Rezzak from the FPGA business unit. A total of five posters were presented during the Poster Session and Radiation Effects Data workshop. Also in attendance were Minh Nguyen, Dorian Johnson and Pascale Charpentier, with the support of Philippe Lebarz and Emmanuel Villand from our local sales organization.

The following posters were presented:

**New Approach of Single-Event Latchup Modeling Based on TCAD Simulations and Design of Experiment Analysis - D. Truyen, L. Montagner, Microchip France**

This work presented a predictive SEL modeling based on physical simulations and DOE analysis. The model is built from layout and process inputs and evaluates SEL risk by estimating the LET threshold and holding voltage

**Analysis of Total Dose Effects on a PDSOI n-channel High Voltage Transistor for Analog Applications**

F. Perez, CNES/MICROCHIP/University of Montpellier, France; F. Saigne, IES, University of Montpellier, France; A. Michez, IES, University of Montpellier, France; S. Furic Microchip, France; E. Leduc, Microchip France, F. Malou, CNES, France; J. Boch IES, University of Montpellier, France; A. Touboul IES, University of Montpellier, France; F. Wrobel, IES, University of Montpellier, France

In this paper, TID irradiations have been performed on a PDSOI n-channel high-voltage transistor for analog applications. ECORCE TCAD modeling software is used to qualitatively analyze and model the physical processes at play.

**Total Ionizing Dose Characterization of 28 nm PolarFire SONOS-based FPGA - N. Rezzak, J. Wang, A. Cai, F. Hawley, E. Hamdy, Microchip, USA.**

This paper presents Total Ionizing Dose (TID) results on 28 nm PolarFire SONOS-based FPGA. Gamma and X-ray induced TID effects at the device and product level are presented and discussed.

**SAMV71RT 32-bit Arm Cortex-M7 Microcontroller Total Ionizing Dose and Single Effects Performances**

B. Treuillard, Microchip Technology Nantes, France

The subject is based on a SAMV71RT radiation-tolerant product addressing New Space requirements. This document proposes the description of the device capability against radiation environment. The poster describes TID and Heavy ions results.



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