CN19009A: RTG4 PLL Lock Stability Customer Notification Addendum

December 27, 2019

Summary

CN19009A is an addendum to CN19009 regarding the RTG4 PLL lock stability over temperature issue under investigation. This addendum provides a reminder of the issue description, root cause, PLL loss of lock characterization status, and workarounds status. Microsemi is actively investigating a workaround to completely mitigate the temperature dependence across the full military temperature operating range. The workaround status is described in a subsequent section. Another Customer Notification addendum will be issued when the investigation is concluded.

Description of Change

RTG4 PLLs can experience loss of lock at high temperature after being initialized, via device power-up or PLL reset, at cold temperature. Once loss of lock happens, the PLL lock can be recovered by issuing a reset to the PLL.

The root cause of the PLL loss of lock has been identified. During RTG4 PLL initialization, a VCO gain setting is automatically chosen to ensure optimal operation. When the PLL is initialized at cold temperature, the automatically chosen VCO gain setting does not provide enough margin for the PLL to operate across the full military temperature range (-55°C to 125°C). Rising temperature normally reduces transistor performance, which slows down the VCO to the point where the PLL cannot remain locked. The PLL's VCO performance is similarly affected if the 3.3 V PLL power supply, VDDPLL, decreases after the initial PLL reset.

The RTG4 junction temperature at power-up, or after PLL reset, determines the PLL operating temperature window before the loss of lock occurs. This PLL operating temperature window is defined as the Temperature Rise Window due to the temperature ramping direction explained in the following section on Application Impact. Resetting the PLL at higher temperatures selects a higher VCO gain, allowing the PLL to operate at a higher temperature.

Application Impact

1. Only the following RTG4 PLLs are impacted.
    - Clock Conditioning Circuitry (CCC) PLLs available in the FPGA fabric
    - FDDR PLLs used in the fabric DDR controllers
    - SerDes SPLLs utilized in PCI Express (PCIe) and XAUI modes to synchronize data to the fabric clock rate

      The SerDes PMA PLLs found in each SerDes lane are not impacted. The SerDes PMA PLLs do not use the same VCO gain settings at initialization as the SerDes SPLLs. The SerDes External PCS (EPCS) mode requires that the user implement the serial protocol's PCS logic in the FPGA fabric. The SerDes EPCS mode only uses the SerDes PMA PLLs and thus the SerDes block in EPCS mode is not impacted by this issue.

2. Temperature Ramping Direction

   The PLL loss of lock for the identified root cause only occurs at temperatures higher than the initial PLL reset temperature. There is no temperature-induced loss of lock when operating at temperatures lower than the initial PLL reset temperature.

3. PLL Loss of Lock Characterization Status

   The PLL loss of lock characterization of RTG4 fabric PLLs, FDDR PLLs, and SerDes SPLLs are complete. The characterization accounted for process, voltage, and temperature (PVT) variations, as well as for device aging and total ionizing dose (TID) radiation effects. The characterization and silicon design

analysis showed that the aging effect through 2000-hour life test and the TID effect through 125-Krad irradiation had no impact on the PLL loss of lock results over operating temperature.

The RTG4 fabric CCC no longer supports PLL lock window settings of 500 ppm and 1000 ppm starting with Libero SoC v11.9 SP5 release and Libero SoC v12.3 release. The PLL lock window setting is now validated against the maximum Phase/Frequency Detector (PFD) rate. For more information, see the *Libero SoC v11.9 SP5 release notes* or *Libero SoC v12.3 release notes* and the RTG4 Clocking Resources User Guide (*UG0586*) Lock Window section containing a minimum lock window formula for a given PLL configuration. Existing designs with 500 ppm and 1000 ppm PLL lock window setting will have their design state invalidated to the pre-synthesis state upon opening with Libero SoC v11.9 SP5 or Libero SoC v12.3 and later releases. The log window will print an invalidation message asking the user to update the fabric CCC and regenerate the affected component instances. Consider migrating to the RTG4 fabric CCC configurator with enhanced PLL calibration core as described in the Workaround Status — Option 2A section.

A PLL Temperature Rise Window calculator spreadsheet was published and posted on the *Microsemi* website. *Login* is required to access the calculator. This calculator enables the assessment of an RTG4 design's susceptibility to the PLL loss of lock described in the preceding sections. It is a useful tool to determine the PLL Temperature Rise Window before the loss of lock occurs. Users can employ this Temperature Rise Window information to determine whether a proactive PLL reset is required to maintain design operation throughout the application specific operating temperature range. More information on required actions are provided in the Workaround Status — Option 1B section. Publication of characterization results will be released at the completion of the investigation.

Workaround Status

Microsemi has identified the following workaround options for the PLL loss of lock.

- **Option 1A: Apply PLL Auto-Reset Logic for Fabric PLLs**

  Workaround Description

  This workaround provides auto-reset fabric logic for the RTG4 fabric CCC configurators in Libero SoC v11.9 SP4 software release and later, as well as in Libero v12.2 release and later. The auto-reset logic is enabled by default whenever the PLL is enabled in the CCC, but the user can optionally disable this setting, provided that the causes and design-specific effects of PLL loss of lock have been analyzed/mitigated. When enabled, the Libero SoC software inserts an additional fabric logic circuit to monitor the PLL lock signal and issues a PLL reset, if loss of lock is detected.

  Workaround Use Model

  A PLL reset is not required if the RTG4 device's operating temperature range is within the temperature rise window predicted by the calculator spreadsheet. No design change is required.

  A PLL reset is required if the RTG4 device's operating temperature range exceeds the temperature rise window predicted by the calculator spreadsheet. A design change is required as the fabric CCC configurator needs to be regenerated in Libero SoC v11.9 SP4 and later, as well as in Libero v12.2 and later. The auto-reset logic can be used to regain the lock when fabric PLLs lose the lock because of rising temperature.

  Unrelated to the temperature-induced PLL loss of lock issue described in this CN, the auto-reset logic can also be used to regain the lock when radiation-induced events cause the fabric PLLs to lose lock. See the *RTG4 PLL SEE radiation report* for information on fabric PLLs' performance in heavy ion environment. See the *RTG4 Proton SEE radiation report* for information on fabric PLLs' performance in proton environment.

  Auto-reset Logic Details

  The auto-reset circuit requires a 50 MHz (or slower) free-running clock such as the clock driven from the on-chip RC oscillator. In order to use the internal RC oscillator clock, users must instantiate the RCOSC_50MHZ macro and distribute its output through a GLx of any one CCC and eventually, connect to the exposed CLK_50MHZ input pin of the CCC using the PLL. The CCC connected to RCOSC_50MHZ could even be the same CCC containing the PLL whose reset logic requires the CLK_50MHZ input.

If users do not want to use the on-chip RC oscillator, the CLK_50MHZ input pin of the CCC can be driven by an external free-running oscillator running at 50 MHz or slower.

See the *Libero SoC v11.9 SP4 software release notes* and the RTG4 Clocking Resources User's Guide (*UG0586*) for more information.

- **Option 1B: Use PLL Temperature Rise Window for System Analysis and Apply Proactive PLL resets**

  Workaround Description

  This workaround provides the PLL temperature rise window calculator for fabric PLLs, FDDR PLLs, and SerDes SPLLs. This information can be used while performing a system and operating condition analysis to determine whether a proactive PLL reset is needed across the system's operating temperature range in order to allow the design to operate from a cold start to a higher temperature.

  Workaround Use Model

  A PLL reset is not required if the RTG4 device's operating temperature range is within the temperature rise window predicted by the calculator spreadsheet. No design change is required.

  A PLL reset is required if the RTG4 device's operating temperature range exceeds the temperature rise window predicted by the calculator spreadsheet. A design change may be required. For fabric PLLs, user can still use the auto-reset logic described in Option 1A to reset fabric PLLs as soon as they lose lock. Alternatively, if the temperature rise window is known, users can proactively reset the fabric PLLs, FDDR PLLs, and SerDes SPLLs at certain temperatures before which the PLL is expected to lose lock. Proactive PLL resets can help avoid interruption to system operation.

  Temperature Monitoring Reference Design

  A temperature monitoring reference design is available on the Microsemi website in application note *AC487* and its associated *design files*. This design example configures an external temperature sensor to perform RTG4 junction temperature measurements across the device's internal temperature diode, and then reads the sensor status signals using FPGA fabric logic. By monitoring the RTG4 junction temperature, the system can decide when to issue proactive PLL resets at the desired temperature, given the temperature rise window obtained from the calculator spreadsheet.

- **Option 2: Perform Enhanced PLL Calibration via VCO Speed-up upon PLL Reset Release**

  Workaround Description

  Microsemi is evaluating enhanced PLL calibration cores in Libero SoC software to eliminate the temperature-induced loss of lock issue. The enhanced PLL calibration process performs a VCO speed-up upon PLL reset release to force higher VCO gain selection before applying the intended user-configured divider settings.

  Workaround Use Model

  A design change is required to apply the enhanced PLL calibration cores. When using the enhanced PLL calibration cores, no PLL loss of lock is expected at high temperature after initialization. Hence, no PLL reset is required.

- **Option 2A: Enhanced PLL calibration cores for single (non-triplicated) fabric PLLs, FDDR PLLs, and SerDes SPLLs**
  - Single fabric PLLs

    The enhanced PLL calibration core for the single fabric PLLs is now available in Libero SoC v11.9 SP5 release and Libero SoC v12.3 release. There are two major differences to note when using the Enhanced PLL Calibration core in RTG4 fabric CCC configurator versus the standard fabric CCC configurator.
    - The RTG4 fabric CCC with Enhanced PLL Calibration core applies to both CCCs in a device corner.
    - The core generates additional fabric logic around the CCC instance(s) to perform PLL calibration. See the latest *RTG4 Clocking Resources User Guide* for more information.
  - FDDR PLLs and SerDes SPLLs

Validation of the Enhanced PLL calibration sequence is near completion for FDDR PLL and SerDes SPLL. Microsemi will release the updated FDDR and SerDes configuration cores to generate enhanced CoreABC initialization microcode that applies the PLL calibration sequence during the subsystem initialization. The enhanced PLL calibration cores for FDDR PLLs and SerDes PLLs are expected in the upcoming Libero SoC v12.4 software release. An update will be provided in the next customer notification addendum.

- **Option 2B: Enhanced PLL calibration core for triplicated (TMR) PLLs**

  Validation of the Enhanced PLL calibration sequence is ongoing for TMR PLL operating mode. In the mean time, users can still use TMR PLLs within the supported temperature rise window or with proactive PLL resets as described in Option 1B. Alternatively, a single fabric PLL with the enhanced PLL calibration core can be utilized if it meets a mission's radiation requirements. An update will be provided in the next customer notification addendum.

Proucts Affected

The following table lists the affected products.

Microsemi Part Number	DLA SMD Number
RT4G150-CB1657PROTO	-
RT4G150-CG1657B	5962-1620801QXF
RT4G150-CG1657E	5962-1620805QXF
RT4G150-CG1657V	5962-1620809VXF
RT4G150-CG1657PROTO	-
RT4G150-CQ352E	-
RT4G150-CQ352EV	-
RT4G150-CQ352PROTO	-
RT4G150-LG1657B	5962-1620803QZC
RT4G150-LG1657E	5962-1620807QZC
RT4G150-LG1657V	5962-1620811VZC
RT4G150-LG1657PROTO	-
RT4G150-1CB1657PROTO	-
RT4G150-1CG1657B	5962-1620802QXF
RT4G150-1CG1657E	5962-1620806QXF
RT4G150-1CG1657V	5962-1620810VXF
RT4G150-1CG1657PROTO	-
RT4G150-1CQ352E	-
RT4G150-1CQ352EV	-
RT4G150-1CQ352PROTO	-
RT4G150-1LG1657B	5962-1620804QZC
RT4G150-1LG1657E	5962-1620808QZC
RT4G150-1LG1657V	5962-1620812VZC
RT4G150-1LG1657PROTO	-
RT4G150-CQ325B	5962-1620813QYC
RT4G150-1CQ325B	5962-1620814QYC
RT4G150L-CG1657B	5962-1620815QXF

RT4G150L-LG1657B	5962-1620816QZC
RT4G150L-CQ325B	5962-1620817QYC
RT4G150L-CG1657E	5962-1620818QXF
RT4G150L-LG1657E	5962-1620819QZC
RT4G150L-CG1657V	5962-1620820VXF
RT4G150L-LG1657V	5962-1620821VZC

Contact Information

If you have any questions about this subject, contact Microsemi Technical Support department by using the support portal at *https://soc.microsemi.com/Portal/Default.aspx*.

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