Libero SoC v12.3

Release Notes

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Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision 1.2

Revision 1.2 includes the following changes:

- Updated section 1.2
- Updated section 1.3.2
- Text edits for clarity and consistency

Revision 1.1

Revision 1.1 includes the following changes:

- Updated section 1.1.4
- Updated section 1.3.6 (FlashPro6 support)
- Added known issue in section 4.16.1
- Updated table and footnotes in section 7.2

Revision 1.0

Revision 1.0 was the first publication of this document.

Contents

1 Libero SoC v12.3 Software Release Notes

The Libero® system on chip (SoC) v12.3 unified design suite is Microchip's flagship FPGA software, for designing with Microchip's latest power efficient flash FPGAs, SoC FPGAs, and rad-tolerant FPGAs. The suite integrates industry standard Synopsys Synplify Pro® synthesis and Mentor Graphics ModelSim® simulation with best-in-class constraints management, debug capabilities, and secure production programming support.

Use Libero SoC v12.3 for designing with Microchip's RTG4 Rad-Tolerant FPGAs, SmartFusion®2 and IGLOO® 2® SoC FPGAs, and PolarFire FPGAs.

To design with Microchip's older Flash FPGA families, use Libero SoC v11.9 and subsequent service packs.

To access datasheets, silicon user guides, tutorials, and application notes, visit www.microsemi.com, navigate to the relevant product family page, and click the **Documentation** tab. Development Kits & Boards are listed in the **Design Resources** tab.

Note: Libero SoC v12.3 does not support Classic Constraint Flow. IGLOO2, SmartFusion2 and RTG4 projects using the 'Classic' flow cannot be opened in this release. See Migrating an Existing Project Created with Classic Constraint Flow to Enhanced Constraint Flow for details about how to migrate Classic Constraint Flow projects to the Enhanced Constraint Flow.

1.1 Customer Notification (CN) Support

Libero SoC v12.3 includes changes that address certain important issues.

1.1.1 PolarFire FPGA CCC PLL Feedback Issue

The PLL within the PolarFire Clock Conditioning Circuitry (PF_CCC) includes optional circuity for implementing External or Post-Divider feedback control for designs requiring clock adjustment to compensate for skew. Implementations of the PF_CCC core generated by Libero SoC v12.2 and earlier have shown intermittent behavior between device startups which manifested as the PLL not locking.

PF_CCC v2.2.100, which is part of Libero SoC v12.3 addresses this issue. Consult section 2.1.2 for instructions on migrating a design to use this core version.

For more information, refer to CN19028.

1.1.2 PolarFire FPGA TVS Powerdown

The Powerdown TVS Sensor between conversions feature of the PolarFire (TVS)Temperature-Voltage Sensor is being deprecated from the TVS module.

The Powerdown TVS Sensor between conversions feature has been found to be ineffective for its intended design purpose and will no longer be supported in software.

For more information, refer to CN19029.

1.1.3 PolarFire FPGA TVS Temperature Flags

The temperature flags of the PolarFire FPGA Temperature-Voltage Sensor(TVS) are found to be triggering at wrong values when set by the user in Libero SoC.

The TRIGGER_TEMP_LOW and TEMP_HIGH flags are not correctly handled when the TVS module is generated by Libero SoC TVS configurator.

For more information, refer to CN19030.

1.1.4 PolarFire Quad0/PCIE1

A PolarFire Quad0/PCIE1 use case in Libero SoC is not generated correctly, causing a device functional issue. This issue requires an update to correctly function.

Prior to the Libero SoC v12.3 release, a register field value corresponding to the Libero SoC PCI Express is incorrectly generated in a design using the Quad0 PCIe1 provisioned with PCIE0 disabled and PCIE1 enabled when using x1 or x2 topologies.

The issue manifests in hardware where the programmed PolarFire device will not enter into L0 PCIe link state. This condition will cause a PCIe system to not enumerate the device. This only impacts designs with x1 or x2 PCIe links using PCIE1. x4 PCIe links are not affected.

For more information, refer to CN19031.

1.1.5 RTG4 Enhanced PLL Calibration

Libero SoC v12.3 includes a new RTG4 Fabric CCC configurator core to remove PLL lock stability dependence on the operating junction temperature across the supported RTG4 operating temperature range (CN19009).

New RTG4 Fabric Clock Conditioning Circuit (FCCC v2.1.010) with Enhanced PLL Calibration for non-triplicated PLL

In this release, enhanced PLL calibration is being offered for RTG4 Fabric CCCs operating in the nontriplicated PLL mode. Support for the triplicated Fabric PLL mode will be added in a future release. Similarly, enhanced PLL calibration will be added to an upcoming release of the RTG4 DDR Memory Controller and High-Speed Serial Interface cores that generate register initialization microcode (for use with CoreABC). These upcoming core revisions will add PLL calibration initialization sequences to the DDR FPLL and PCIe/XAUI SPLL.

1.1.6 RTG4 Fabric Clock Conditioning Circuit (FCCC)

The RTG4 Fabric Clock Conditioning Circuit (FCCC v2.0.104) no longer supports PLL Lock window settings of 500 ppm and 1000 ppm. Upon generation, the PLL Lock window setting is validated against the maximum Phase/Frequency Detector (PFD) rate. Refer to the RTG4 Clocking Resources User Guide (UG0586) Lock Window section containing a minimum lock window formula for a given PLL configuration.

Existing designs will have their design state invalidated to the Pre-synthesis state upon opening with Libero SoC v12.3. The log window will print an invalidation message asking the user to update the FCCC and regenerate the affected component instances. Consider migrating to the RTG4 FCCC with Enhanced PLL Calibration core as described in section 2.1.1 below.

1.2 New Device Support

Libero SoC v12.3 includes the following enhancements for PolarFire devices:

- New MIL temperature grade devices (all supporting 1.0V, STD speed grade):
  - MPF200TS
  - MPF300TS (including Production timing and power support)
  - MPF500TS

Libero SoC v12.3 includes the following enhancements for RTG4 devices:

- New 1657 FCG package support for RTG4 devices.
  - RT4G150 1657-FCG (STD and –1)
  - RT4G150L 1657-FCG (STD)

Note that as of this release, the new 1657 FCG package has not been fully qualified, and should not yet be considered a Production package.

1.3 Software Features and Enhancements

1.3.1 Ease of Use Enhancements

Libero SoC v12.3 introduces a few enhancements intended to improve the user experience:

Design Hierarchy Navigation

With this release, users can now search for the required modules, expand or collapse all the modules in the hierarchy, and search for components not yet generated or unknown modules in the Design Hierarchy window.

Constraints Manager

The Constraints Manager now allows users to Discard or Save changes made to constraint file associations to tools preventing accidental invalidation of the design flow.

1.3.2 Tcl Support Enhancements

Libero SoC v12.3 adds the following Tcl support enhancements:

Hierarchical Export of SmartDesign Tcl Description

To enhance design scriptability and reusability, a Tcl fully describing a SmartDesign Component and its child Components can now be exported. Access this new option by right-clicking on any SmartDesign Component in the Design Hierarchy. See section 4.4.

New Tcl Commands in Libero SoC v12.3

get_tool_state: Returns the state of a tool (i.e. whether it has been executed for the current project)

get_tool_options: Returns the configured options/parameters of a tool in the Libero Design Flow.

EXPORTNETLIST: Exports a .v/.vhd netlist file to the active synthesis implementation folder.

Syntax and parameters for the above commands are documented in the Online Help, and in the PolarFire TCL Commands Reference User Guide and Libero SoC TCL Commands Reference User Guide.

1.3.3 Synthesis

SynplifyPro O201809MSP1-1 is the OEM Synthesis tool integrated with Libero SoC v12.3 (no change from the preceding Libero SoC v12.2)

1.3.4 Place and Route

Libero SoC v12.3 includes an average 10% runtime improvement for PolarFire designs.

For PolarFire, the number of half-chip globals that can be automatically assigned by Place and Route has been increased in this release from 24 to 36. Note that only 24 out of the 36 globals may be driven from the FPGA fabric; the remainder must be driven by CCC or hardwired I/Os.

As of this release, the Place and Route log will issue warnings when clock nets are routed using regular routing resources instead of dedicated global resources. It is recommended to use global resources to route clocks. The details of each clock net using regular routing resources also appear in the Warning section of the Global Net Report.

1.3.5 Consolidated Timing Report (Multi Corner)

Libero SoC v12.3 introduces consolidated "multi-corner" timing analysis & violation reports. Multi corner reports reflect the results of static timing analysis using max and min delays across all temperature/voltage/process "corners".

Default Behavior

For projects created using Libero SoC v12.3 or later, when Verify Timing is run, multi corner timing analysis and violation reports (one set of reports for max delay and one for min delay) will be generated by default. Corner-specific reports will not be generated by default.

For projects created with older releases, when Libero SoC v12.3's Verify Timing step is run, in addition to any single-corner timing reports, the new multi-corner timing reports will also be generated.

As with previous releases, use the Configure Options dialog for the Verify Timing tool to modify which single-corner and multi-corner timing reports are generated by the Verify Timing tool.

1.3.6 Programming

FlashPro6 Support

Libero SoC v12.3 continues to enhance support for the next-generation Microchip Flash Programmer, FlashPro6. FlashPro6 offers faster Programming time and faster device debugging actions.

FlashPro6 currently supports the following platforms:

- **Device families**: SmartFusion2, IGLOO2, RTG4, PolarFire
- **Operating systems**: Windows 7, Windows 10, RedHat and CentOS versions 6.6-6.11; 7.2-7.6
- **Software Tools**: Libero, FlashPro Express, SmartDebug

Users of FlashPro6 will see the following speedups in Libero SoC v12.3 (relative to FlashPro5):

- Up to 25% speedup in Programming actions for RTG4 devices
- Up to 50% speedup in Programming actions for PolarFire devices
- Significant speedup in combined Erase, Program and Verify actions for SPI Flash memory devices
- Significant speedup in SmartDebug actions

Refer to the Appendix for details on Programming and Debug time improvements possible with FlashPro6.

SVF Support

The SVF programming file format is now supported in bitstream export for SmartFusion2 and IGLOO2 devices.

DEVICE_INFO Enhancements

With this release, the DEVICE_INFO programming action now reports the following new data for SmartFusion2 and IGLOO2 devices:

- The family name and product name of the device being programmed
- The status of the Cortex-M3 (enabled or disabled)

SmartDebug

The following new SmartDebug features have been added in this release:

- FPGA Hardware Breakpoint (FHB) Auto Instantiation support for Synthesized Verilog Netlist files (files that are imported using Import → "Synthesized Verilog Netlist(*.vm) option in Libero)
- Addition of Project Checksum field to let users know if the design programmed in the device matches the design used for debug

1.4 New Silicon Features and Enhancements

1.4.1 PolarFire Transceiver Solution

Libero SoC v12.3 enhances the PolarFire Transceiver Solution to add a generic Transmit PLL solution for Jitter Attenuation. This can be accessed in the Transmit PLL Configurator, under “Jitter Cleaning Mode” => “Custom Protocol Settings.”

For more information, refer to UG0677: PolarFire FPGA Transceiver User Guide.

In addition, the Transmit PLL now supports the Spread Spectrum mode, which can be enabled using the “SSCG Modulation” radio button in the configurator.

In this release, the PolarFire Transceiver Solution supports an expanded set of CTLE settings. Note that these settings are not yet fully validated, and should not be considered Production.

- For A2 - Short/Medium in CDR, CDR Auto and DFE modes the following RX_CTLE options are available:
    - No_Peak_+9.22dB
    - No_Peak_+4.53dB
    - No_Peak_+1.76dB
    - 5GHz_+3.14dB
- For A1 - Short/Medium in DFE mode the following RX_CTLE options are available:
    - No_Peak_+11.10dB
    - No_Peak_+6.13dB
    - No_Peak_+3.39dB
    - 6GHz_+2.73dB
    - 6GHz_+3.12dB

For details about CTLE settings, refer to AC483: PolarFire FPGA Transceiver Signal Integrity Application Note.

1.4.2 Configuration Reports

PolarFire

Libero SoC v12.3 now generates Register Configuration reports for PCIe, Transceiver, and Transceiver Transmit PLL blocks present in PolarFire designs. Run the ‘Generate Design Initialization Data’ step in the tool flow and open the Reports view to see the reports with configured values for various registers and their addresses corresponding to all the PCIe, Transceiver, and Transceiver Transmit PLL blocks used in the design.

IGLOO2 and SmartFusion2

The Configuration Report now contains new sections to report the configuration of unused hard IP blocks in the device. This facilitates the documentation of these unused IP blocks (e.g. in avionics applications). The following types of unused IP are now reported in the Configuration Report:

- MSS/HPMS
- FDDR
- SERDES
- CCC

The Configuration Report contains the following types of information for unused IPs:

- Programmed configuration (flash-bits) for these physical blocks
- Tie-off values of critical ports such as resets, clocks, and powerdown ports

In addition, the Configuration Report contains a new section that reports whether the system controller suspend mode and the Cortex-M3 are enabled in the design

1.4.3 IGLOO2 and SmartFusion2: Configuration locks for unused IP

Libero SoC v12.3 adds a configuration lock setting capability for unused MSS, FDDR and SERDES hard IP blocks, targeting SmartFusion2 and IGLOO2 devices. Refer to application note AC406: Configuring IGLOO2 and SmartFusion2 Devices for Safety-Critical Applications for instructions on using this capability.

2 Migrating Designs to Libero SoC v12.3

2.1 Notes on Design Migration

2.1.1 RTG4 CCC Updates

Migrating an Existing RTG4 Design from v12.2 or v11.9 SP4 (or older)

Migrating an Existing RTG4 Design to Libero SoC v12.3

With Libero SoC v12.3, users opening existing designs have the choice to continue using the standard RTG4 FCCC core or manually migrating to the RTG4 FCCC with Enhanced PLL Calibration core.

Continuing with the PLL instantiated via the standard RTG4 FCCC core means that the PLL lock stability will be dependent on the operating junction temperature as discussed in CN19009. Users are encouraged to review the CN and confirm the supported temperature rise window for each PLL used in the design via the PLL Temp Rise Window calculator spreadsheet.

Migrating to the PLL instantiated in the RTG4 FCCC core with Enhanced PLL Calibration means that the non-triplicated fabric PLL lock stability is no longer dependent on the operating junction temperature.

Migration from the standard RTG4 FCCC core to the RTG4 FCCC with Enhanced PLL Calibration is recommended in the following scenario:

- The non-triplicated RTG4 Fabric PLL is used in the design and the application must support operation at a junction temperature rise window beyond that predicted by the PLL Temp Rise Window calculator described in CN19009.

Designs using the FCCC without the PLL or with triplicated PLL (internal feedback) do not need to migrate to the Enhanced PLL Calibration core unless the CCC shares the device corner with another fabric CCC that is using the non-triplicated PLL. Designs using the triplicated PLL (via PLL internal feedback) can only use the standard FCCC core in this release. Enhanced calibration for the triplicated PLL is planned for a future release.

Summary of Migration Steps

1. Note the configuration of each CCC instantiated in the existing design. This can be done by either opening the configuration GUI for each CCC and saving screenshots of each tab, or by opening the CCC configuration report for each component instance.
    - Opening Existing CCC GUI: When opening an existing CCC in Libero SoC v12.3, the instance version must first be updated to RTG4 FCCC **v2.0.201** by right-clicking the component in the Design Hierarchy pane and selecting “Replace Component Version”

    Note: PLLs configured to Lock Window settings of 500 ppm or 1000 ppm will have their respective Lock Window setting reset to the 6000 ppm default.

    - Using CCC configuration report: The configuration report is an XML file found in the example path shown below:

      ```
      <libero_prj_folder>/component/work/<ccc_comp_name>/<inst_name>/<ccc_comp_name>_<inst_name>_configuration.xml
      ```

    Note: The XML file can be viewed in a web browser if the rptstyle.xsl file is placed in the same folder as the XML file, before opening the file. The rtpstyle.xsl can be found in the Libero project folder path below:

    ```
    <libero_prj_folder>/designer/<top_level_inst_name>/rptstyle.xsl
    ```

2. Note the location and CCC number for each CCC instantiated in the existing design and group them by device corner (NW, NE, SW, or SE) and CCC number (0 or 1). This information is found in the Global Net Report available after running the Place and Route design flow step. Refer to the CCC Input Connections table for the CCC Location column to identify the die corner (NW, NE, SW, or SE) and CCC number (0, or 1). For example, a CCC Location can be listed as CCC-SE1 for CCC #1 in the Southeast corner.
    - The Global Net Report can be viewed in the Libero Reports tab under the Place and Route report list or by opening the file directly in a web browser from the default file location within the project folder. The file name format follows the convention: `<top_level_inst_name>_glb_net_report.xml` and it can be found in the project folder path `<libero_prj_folder>/designer/<top_level_inst_name>/`.
3. Delete all existing CCC instances that are being migrated to the CCC with Enhanced PLL Calibration, even those not using the PLL, if they share the device corner location with a PLL that *is* being migrated.
4. Configure a new instance of RTG4 FCCC with Enhanced PLL Calibration **v2.1.010** for each pair of CCCs being migrated.
    - Use the CCC configurations noted in step 1 above for each CCC location per device corner, ensuring that respective settings are mapped to the correct CCC tab in the configuration GUI for CCC_0 and CCC_1.
    - Refer to the RTG4 FCCC with Enhanced PLL Calibration Configurator User Guide for information about using the configurator GUI.
    - Refer to UG0586: RTG4 Clocking Resources User Guide *revision 8 or newer* for information about the CCC / PLL settings and use models, including Lock Window settings and Auto-Reset logic.
5. Open the Constraints Manager from the Design Flow tab, and click **Derive Constraints** in the Timing tab to generate the required clock and false-path constraints for the CCC/PLL instances.
6. Integrate the new CCC component into the design hierarchy by replacing the module instantiations and connections to the standard FCCC with an instantiation of the new FCCC with Enhanced PLL Calibration containing ports for CCC_0 and CCC_1 on the same component instance.

Migrating an Existing RTG4 Design from v11.9 SP5

If your Libero SoC v11.9 SP5 design has already been migrated to use the RTG4 FCCC v2.0.201 or RTG4 FCCC with Enhanced Calibration v2.1.010, your design will not be invalidated. However, if these cores need to be regenerated for any reason, the latest version from the Catalog must be used. Follow steps 1-5 in Section 2.1.3 below.

2.1.2 PolarFire CCC Updates

PolarFire CCC v2.2.100 (compatible with Libero SoC v12.3) fixes an important meta-stability issue in External and Post-Divider Feedback soft logic. If your pre-v12.3 project contains a PolarFire CCC configured to use External or Post-Divider Feedback modes, upon opening it with Libero SoC v12.3, it will be invalidated to Pre-Generate state. If this occurs,

1. Download the latest version of the core into your vault.
2. Upgrade each configured core in your design to the latest version (2.2.100) by right-clicking the core component in the Design Hierarchy and selecting 'Replace Component Version…'.
3. Regenerate the design.
4. Rerun the Derive Constraints step.
5. Rerun the tool flow.

Note: Custom flow (VM import) users must regenerate the CCC that was used to synthesize the VM if the CCC was using the external/post-div feedback. The design must then be resynthesized.

2.1.3 Core Upgrade

If a Libero SoC v12.3 project contains the following cores, and the cores have been generated, they do not need to be upgraded upon migrating the project to Libero SoC v12.3. However, if the core needs to be generated again for any reason (for example, a change in parameters), the latest version from the Catalog must be downloaded and used.

- PolarFire CCC[1]
- PolarFire Transmit PLL
- PolarFire I/O
- PolarFire Initialization Monitors
- RTG4 Fabric CCC
- RTG4 Fabric CCC with Enhanced PLL Calibration

For the above cores, if you want to change their configuration, you must do the following:

1. Download the latest version of the core into your vault.
2. Upgrade each configured core in your design to the latest version by right-clicking on the core component in the design hierarchy and selecting 'Replace Component Version'.
3. Regenerate the design.
4. Rerun the Derive Constraints step.
5. Rerun the tool flow.

[1]Note: The PolarFire CCC v2.1.104 core can be regenerated with Libero SoC v12.3, without upgrading to the latest PolarFire CCC core. However, if External or Post-Divider Feedback modes are used, generation of the core will fail. Microchip recommends upgrading all cores components to the latest available version.

2.2 PolarFire Core Updates

Libero SoC v12.3 includes the following PolarFire core updates from Libero SoC v12.2.

Display Name	Libero SoC v12.3 version	Changes for Libero SoC v12.3
PolarFire Clock Conditioning Circuitry (CCC)	2.2.100	Fixed Post-divider and external feedback modes meta stability issue. Refer to section 1.1.1 for details.
PolarFire I/O	1.0.104	No functional changes
PolarFire Initialization Monitors	2.0.104	Added I/O recalibration capability (CALIB_START signal)
PolarFire Transmit PLL	2.0.200	Added Spread Spectrum support Added Custom Protocol settings for jitter attenuation use models

2.3 RTG4 New Cores

Libero SoC v12.3 includes the following RTG4 core updates from Libero SoC v12.2.

Core	Version	Description
RTG4 FCCC with Enhanced PLL Calibration	2.1.010	New core. See section 1.1.2
RTG4 Clock Conditioning Circuit (CCC)	2.0.201	See section 1.1.3

RTG4 CCC APB Interface	1.1.109	Resolve hold violations
RTG4 DDR Memory Controller	2.0.100	No functional changes
RTG4 High Speed Serial Interface (PCIe, EPCS & XAUI)	2.0.100	No functional changes
RTG4 High Speed Serial Interface (EPCS & XAUI)	2.0.100	No functional changes

3 Resolved Issues

The following table lists the customer-reported SARs resolved Libero SoC v12.3. Resolution of previously reported "Known Issues and Limitations" is also noted in this table.

3.1 List of Resolved Issues

Case Number	Description
493642-2601274887	Mismatch in the hardwired net from IOPAD_IN:Y to GBM:An between post-layout simulation and SmartTime reports
493642-2666904321, 493642-2675947969	PF_FCCC: CCC_0_PLL_EXT_FEEDBACK_MODE_RTL logic issue
493642-2671325505	PF_XCVR: PolarFire PCIe1 UIC
493642-2658293185	A_WEN[1] behavior when data width is less than 11
493642-2655141910	Messaging during logic assignments in the region
493642-2654021376	CCC GPDs reset after lock when driven by non-PLL output sources
493642-2610293482	IBIS software export: SmartFusion2/IGLOO2: SERDES and differential clock re-biasing issue
493642-2643676150	SmartFusion2/IGLOO2: Clock constraint not analyzed
493642-2650986625	Clock Group constraints not honored by SmartTime
493642-2633658184	PF_INIT_MONITOR: Calib_start needs to be addes in PF_Initialization _monitor IP
493642-2636978831, 493642-2637115919, 493642-2673908851	CCC producing output clocks and asserting lock when no input clock is present
493642-2634547986	Libero SoC SDF File Generation in v12.1
493642-2619692584, 493642-2669481953, 493642-2671343751	Unable to generate the firmware for soft cores in SmartDesign-based projects
493642-2545154827	ODT - Series Pin Mapping model missing from exported RTG4 IBIS file
493642-2592752842	IGLOO2 EDN file created using Libero v11.8SP1 fails in Libero SoC v12.1
493642-2608338001	RTG4: BVALID does not behave as expected during FDDR simulation
493642-2573858783	Libero SoC v12.0 does not include new SmartDesign features
493642-2574818193, 493642-2590831388, 493642-2596337143, 493642-2659811742	Unsigned driver actelsvc.sys in FlashPro v11.9 installation
493642-2558949322	Additional information on "SPI Clock divider value"
493642-2549800616	FlashPro6: SPI-SLAVE PROGRAMMING: Support for SPI-Slave programing in FlashPro software
493642-2526041901, 493642-2569622715	Change of path for linked files does not affect the SmartDesign
493642-2526431054	Linked file instantiated in SmartDesign does not get updated when the HDL is edited
493642-2523725687	Help options to update for SmartTime: online help points to old options for PolarFire
493642-2505664212	XCVR window shows illegal routing assignments with red arrow - needs error message
493642-1826645965, 493642-1825092298, 493642-1980430671, 493642-1986322124, 493642-2005176595,	Feature: SVF file support for SmartFusion2 and IGLOO2 devices

493642-2141382953, 493642-2356766859, 493642-2392075854, 493642-2461809942, 493642-2513380594	
493642-2610293482	SmartFusion2/IGLOO2: SERDES and differential clock re-biasing issue
493642-2679326818	Import_component Tcl command is not listed as supported Tcl for PolarFire
493642-2673109884	HDL_LANGUAGE: DH: CRASH: Libero crash when importing packages and building Design Hierarchy
	PROGRAM, VERIFY, ERASE, AUTHENTICATE actions should read device certificate and report family and device

4 Known Issues and Limitations

4.1 Catalog Cores

4.1.1 Core Generation Language

In Libero SoC v12.3, the PolarFire cores listed in section 2.2 generate only Verilog files, regardless of the preferred HDL language selected in the Libero project.

VHDL users desiring to simulate designs containing affected cores must use mixed-language simulation (available with ModelSim ME Pro, which is bundled with this release, and requires a Gold, Platinum, or Eval license).

4.1.2 Linux: Core generation fails in batch mode when the DISPLAY variable is not set

The following Direct Cores cannot be generated in Libero in batch mode via Tcl when the DISPLAY variable is not set on a Linux machine:

- CoreAXI4SRAM
- CoreCIC
- CoreCordic
- CoreABC
- CoreEDAC
- CoreDDS
- CoreFIFO
- CoreFFT
- CoreFIR_PF
- CoreRSDEC
- CoreRSENC

4.1.3 Core version upgrade

When upgrading the core version for components created for PolarFire System Builder cores from an older version to the latest, it is required that both the core versions are downloaded to the vault. Core version upgrade fails otherwise.

4.1.4 New cores are available pop-up message

New cores are available pop-up appears on opening a project. The pop-up should be ignored if the cores are not present in the catalog.

4.2 Project Manager

The Generation of Licensed Cores Core APB3 and Core ABC will fail if done through Remote Desktop.

4.3 Design Hierarchy

4.3.1 HDL language duplicate modules

- Opening an existing project does not show Design Hierarchy correctly when the design has duplicates between a core module and an HDL module.

Workaround: Build the Design Hierarchy after opening the project.

- If a design has duplicates between the elaborated modules of the core and a normal HDL module, they are not shown as duplicate modules in the Design Hierarchy.
- If two different VHDL files have same signature (same inputs, outputs, and architecture), they are not detected as duplicate modules in the Design Hierarchy.

4.3.2 Multiple definitions error message for RTG4FCCC and RTG4FCCCECALIB

When RTG4FCCC and RTG4FCCCECALIB are used in same design, multiple definitions error message is reported in the log window. This will not stop the user design flow.

Error: The CCCAPB module is defined in multiple files. Duplicate modules are not supported.

User can select any one of the ccc_comps.v files, as they have the same content.

4.4 Tcl Support Limitations

Parameters for SgCore and System Builder components are not documented. To configure such cores using Tcl, do the following:

1. Use the GUI to configure the core as desired.
2. Export the core configuration Tcl description by selecting the “Export Component Description(Tcl)” action on the right-click menu of the component in the Design Hierarchy.
3. Use the exported Tcl command to create the configured core in a regular Tcl script.

Note: The following set of cores cannot be configured using Tcl; the Export Component Description (Tcl) option is thus not supported:

- SmartFusion2/IGLOO2 MSS/HPMS component
- SmartFusion2/IGLOO2 System Builder component
- RTG4 DDR memory controller with initialization (RTG4FDDRC_INIT)
- RTG4 High Speed Serial Interface 2 – EPCS and XAUI – with Initialization (NPSS_SERDES_IF_INIT)
- RTG4 High Speed Serial Interface 1 – EPCS and XAUI – with Initialization (PCIE_SERDES_IF_INIT)

4.5 SmartDesign

4.5.1 Modify Memory Map feature should not be used

The Modify Memory Map action used to connect peripherals to buses in the SmartDesign canvas should not be used in the Libero SoC v12.3 release. If used, Libero may crash or produce an incorrect/incomplete memory map. Connect peripherals to bus slave positions manually, as per the desired memory map.

4.5.2 Export Component Description (Tcl)

In some cases, when the Export Component Description (Tcl) command is executed on a SmartDesign, pin groups created by Libero are converted to Tcl and the exported Tcl script errors out when executed.

Workaround:

1. Delete the converted line(s) that have create_pin_group commands that are failing from the exported file.
2. Delete the created SmartDesign.
3. Re-execute the Tcl script.

4.6 Synthesis

4.6.1 MPF500T/TS/TL/TLS: encrypted blocks are limited to one top level module

To avoid Synthesis failures for Libero projects targeting the MPF500T device, ensure that each encrypted block in the design has exactly one top module. This issue also affects designs containing the Cortex-M1 IP core.

4.6.2 SynplifyPro mapping of sequential shift to uSRAM does not support initial values

PolarFire devices do not support initial values on registers for Sequential-shift constructs mapped to uSRAMs. If an initial value is specified for a register in RTL, Synplify will ignore the value and issue a warning.

4.6.3 SynplifyPro version checking returns an error message on RHEL/CentOS 7.4

Checking the SynplifyPro version with the following command returns an error message:

```
synplify_pro -version -batch
```

```
Error creating '"Internal Error: unsupported format used in message: ' Error creating '"Internal Error: unsupported format used in message: ' N-2017.09M-SP1-1
```

Note: In Libero SoC v12.3, the dialog box where a Synthesis profile is added will display the same error message.

This error message can be safely ignored. These operating systems are supported by Libero SoC v12.3.

4.6.4 Standalone Synthesis Flow

Libero SoC v12.3 users can synthesize their design outside the Libero SoC software by using Synopsys SynplifyPro directly. When using this flow, the following additional steps are necessary to successfully synthesize and implement a design:

- For Windows, ensure that the <install location>/Designer/data/aPA5M/polarfire_syn_comps.v is added as a source file to the SynplifyPro project. This file contains module declarations with timing information for PolarFire primitives not known to Synopsys.
- For Linux, ensure that the <install location>/Libero/data/aPA5M/polarfire_syn_comps.v is added as a source file to the SynplifyPro project. This file contains module declarations with timing information for PolarFire primitives not known to Synopsys.
- Many configured cores generate timing constraints. You must ensure that these constraint files are passed to synthesis for optimal results. These constraint files must also be imported into Libero along with the synthesis gate level netlist to get optimal place and route and timing analysis results. Core-generated constraint files must be modified so that constraints are expressed using the proper hierarchical name of the configured cores in the top-level design.

4.7 Place and Route

4.7.1 Min-Delay violations

There could be min-delay violations remaining in the slow process/low voltage corners in the design, even after running Repair min-delay violations.

4.8 I/O Editor

4.8.1 DRC validation

The DRC check in the I/O Editor does not validate all the constraints set in the tool. You must run Place and Route to validate these constraints.

4.8.2 XCVR SI Parameters in Placement View

In the I/O Editor XCVR View, clicking on a placed XCVR lane in the Placement view does not show any Signal Integrity parameters corresponding to that lane in the Signal Integrity view.

Workaround: Click on the XCVR lane instance in the schematic view to select the lane and view the parameters corresponding to that lane in the Signal Integrity view.

4.9 Netlist Viewer

Opening two or more views (for example, Hierarchical RTL View and Flattened Post-Compile View) in Netlist Viewer may result in a crash due to memory usage. Avoid opening multiple views for large designs.

4.10 PolarFire Block Flow

Libero SoC v12.3 supports Block Flow. The limitation is that only Fabric components (LUT, SLE, RAM, MATH) may be instantiated in a Block. All other components (CCC, DDR, and so forth) must be part of the top-level design and cannot be instantiated in Blocks.

4.11 IBIS Models

For all PolarFire MPF300T/TS/TL/TLS -FCG1152 devices, SSN Analyzer simulated data deviates from the Silicon measured data. This deviation can be between 20%-60%.

4.12 Initialize RAM at Power-up

- Unable to open memory file error in Fabric RAMs tab

  If the “Initialize RAM at Power-up” option is selected without specifying the memory file, the Fabric RAMs tab in the Configure Design Initialization Data and Memories and the Memory Initialization tools will error out as “Unable to open memory file.”

  Workaround:

  If you intend to initialize the memory file with zero’s (and therefore did not specify memory file option in the configurator), you must edit the corresponding client and select the initialization option “Content Filled with 0s” in the Fabric RAMs tab.

  If you intend to specify a memory file, you must select the “Content from file” option and specify a memory file.

4.13 Post-layout simulation is not supported for PolarFire

Post-layout simulation is not supported for PolarFire devices in the Libero SoC v12.3 release.

4.14 PolarFire Silicon Support Limitations

4.14.1 PLL

- Bypass option on output clocks is not available in this release.
- PLL External feedback mode limitations:
- The PLL Lock does not assert in Post Synthesis Simulation.

4.14.2 PCIe

- During BFM simulation of the PCIe AXI interface (master or slave), the simulator may print warning messages about AHB signals, such as “HRESP”. The warning messages can be ignored.
- Some collapsible UI settings in the PF_PCIE configurator GUI are not clearly visible when invoked on laptop screens.

  Workaround: Collapse all settings except the one you want to view or configure.

4.14.3 PF_CCC

- For some cores, not all rules are validated for parameters when using Tcl configuration. As described earlier in this document, users should always use the UI first to configure, export the Tcl description and reuse as is.
- When the PolarFire CCC is configured in DLL or PLL-DLL cascaded mode, the DLL reference frequency must be greater or equal to 133 MHz. When opening a design using the custom flow, this rule is not enforced. Users should make sure that they have generated a CCC configuration that does not violate this requirement. CCC generated with Libero SoC v12.1 or later meet this requirement.
- In some PF_CCC external feedback configurations, post-synthesis simulation might fail with the lock not going high. Pre-synthesis simulation will still work fine in these cases.

4.14.4 PF_TVS

- POWERDOWN checkbox in TVS IP is not working. This feature will be removed in upcoming releases. For more information, refer to CN19029.

4.14.5 PF_UPROM

- When UPROM is configured with invalid values such as incorrect path to mem file, mismatch in number of words specified and the number of words in mem file, etc via Tcl, the generate_component Tcl command does not fail. This issue will be fixed in upcoming releases.

4.14.6 PF_SPI

- PF_SPI Macro does not support SPI-Slave mode. It supports SPI-Master mode only. The SS_OE and CLK_OE ports should always be tied high.

4.14.7 Transceiver Reference Clock

- Enabling on-die-termination and external VREF on the Transceiver Interface Reference Clock I/O is not supported in the I/O editor. However, these options can be set in the I/O PDC file.

  Refer to UG0715: PDC Commands User Guide (PolarFire) for more information.

- The connection from the Transceiver Interface Reference Clock I/O to the South-East PLL for all the reference clocks associated with Transceiver Interface Quad 0,2 and 4 lanes is not available in the software. Place and Route will fail if this connection is attempted.

4.14.8 Transceiver Interface

- Post-synthesis simulations are not supported for the Transceiver Interface.

4.14.9 I/O's: SSTL15 On-Die Termination values are incorrectly programmed

For MPF300XT/TES/TSES devices, when the ODT value for an SSTL15 I/O is selected as 20 Ohm or 30 Ohm, an incorrect setting is programmed

Workaround: Do not use 20 or 30 Ohm on-die termination values for the affected devices.

4.14.10 IOD Receive Interface Data rate issue

In the PF_IOD_RX configurator, duplicate Data rate DRC check messages appear for the presets RX_DDRX_B_G_FA_HSIO, RX_DDRX_B_G_DYN_HSIO and RX_DDRX_B_R_DYN_HSIO. Ignore the second DRC message. The correct Data rates for the presets are 700, 1600 and 500, respectively.

4.14.11 ERM is not available for MPF300XT or ES devices

The XCVR_ERM core must not be used with the MPF300XT or MPF300T/TS_ES devices. This restriction is not currently enforced by the Libero software.

4.15 PolarFire XCVR sourced fabric clocks and jitter compensation

The PolarFire XCVR can source three different clocks into the fabric, TX_CLK, RX_CLK, and the REFCLK (FAB_REF_CLK). These clocks will contain high frequency jitter that is not reported by Libero in the timing report and SmartTime. It is recommended that users add clock uncertainty constraints to these clocks in their design.

The following is a list of recommended values for clock uncertainty per clock, resource, and speed-grade.

- FAB_REF_CLK on Global: 275ps for STD, 200ps for –1
- FAB_REF_CLK on Regional: Not supported
- TX_CLK_G on Global: 300ps for STD, 225ps for –1
- TX_CLK_R on Regional: 225ps for STD, 150ps for –1
- RX_CLK_G on Global: 325ps for STD, 250ps for –1
- RX_CLK_R on Regional: 250ps for STD, 175ps for –1

Below is an example clock uncertainty constraint. This constraint would be added to the user's timing SDC file.

```
# TX_CLK and RX_CLK on Regionals
set_clock_uncertainty -setup 0.150 [ get_pins { PF_XCVR_ERM_LANE2/I_XCVR/LANE0/TX_CLK_R } ]
set_clock_uncertainty -setup 0.175 [ get_pins { PF_XCVR_ERM_LANE2/I_XCVR/LANE0/RX_CLK_R } ]

# TX_CLK and RX_CLK on Globals
set_clock_uncertainty -setup 0.300 [ get_pins { PF_XCVR_ERM_LANE2/I_XCVR/LANE0/TX_CLK_G } ]
set_clock_uncertainty -setup 0.325 [ get_pins { PF_XCVR_ERM_LANE2/I_XCVR/LANE0/RX_CLK_G } ]

# FAB_REF_CLK on Global
set_clock_uncertainty -setup 0.275 [get_clocks PF_DDR4_C0_0/CCC_0/pll_inst_0/OUT1]
```

These constraints will be automatically added to the derived constraints from the Constraints Manager in a future release of Libero.

4.16 Programming

4.16.1 Libero Programming

- Updating the security or sNVM with a security-only bitstream or sNVM-only bitstream on a device that has the Fabric programmed will disable the Fabric.

  If the Fabric has been disabled, you must reprogram the Fabric to enable it.

  Workaround:

  a. sNVM only bitstreams: Field-update bitstream files should always program the Fabric with sNVM.
  b. Security only bitstreams: Security-only bitstream should be used on a blank device only.

- When a device is programmed with a blank Silicon Signature field, it will not get erased.

  Workaround:

  a. Specify a Silicon Signature that is not blank and program the device to change the value.
  b. Perform the Erase program action to erase it.

- A SPI file that contains a Silicon Signature setting (set in Configure Programming Options) cannot be imported as a SPI bitstream file for a Recovery/Golden client (in the SPI Flash configurator).

  Workaround: Use Libero SoC v12.0 software.

- If the USERCODE that is part of the security segment is unspecified and the security is not programmed, the previous value of USERCODE will be retained.
- FlashPro Express does not support SPI-Flash only programming in a JTAG chain with SmartFusion2/IGLOO2 and PolarFire devices.
- Serialization is not working for SmartFusion2 and IGLOO2 in Libero SoC v12.3.
  Serialization of the eNVM client is not working for Libero SoC v12.3.

  Workaround: Use Libero SoC v11.9.

- The action device_info shows programming file type as SVF instead of PPD when job-ppd is used.
- Programming is not supported for the RTG4150L device.

4.16.2 SPI Flash Programming

This release includes the following limitations:

- Supports only the following Micron SPI Flash memory devices:
  - Using FlashPro5: MT25QL01G only
  - Using FlashPro6: All members of N25Q and MT25Q device families.

  Note: For support Flash memory devices from other vendors and device families using FlashPro6, contact Microchip Technical Support.

- This tool erases the SPI Flash prior to programming. It is recommended to program the SPI Flash with Programming and Debug Tools v12.3 prior to programming other data on the SPI Flash using non-Libero programming solutions.
- Partial update of the SPI Flash is currently not supported.
- It is not recommended to have huge gaps between clients in the SPI Flash, since gaps are currently programmed with 1’s and will increase programming times.

See the appendix for programming tables.

4.16.3 sNVM write fails due to ROM client created by previous design

In the scenario where a PolarFire device is first programmed with a design with an sNVM client, and then reprogrammed with a (different) design without an sNVM client, upon completion of programming with the second design, the sNVM client will not be erased. In such a case, if there are sNVM pages that are locked, writes to those pages will fail.

There is no programming action to erase the sNVM completely.

Workaround: Create a dummy sNVM client (filled with 0's) in the second design.

4.16.4 FlashPro will error out, if an existing PDB is modified to disable the fabric

If an existing PDB file is modified to disable the fabric and programmed only with eNVM, FlashPro will error out.

4.16.5 Verify during PROGRAM action fails for design with custom user security

For Libero SoC v12.0 and above, PolarFire designs having Custom user security options, enabling DO_VERIFY optional procedure in PROGRAM action and executing PROGRAM action in Libero (via Run PROGRAM action) will fail with "Invalid/Corrupted encryption key".

Workaround:
Run standalone VERIFY action after PROGRAM separately if needed.

4.17 SmartDebug

4.17.1 General SmartDebug Limitations

- Initializing RAM blocks with random values in the Design Initialization Data and Memory tool will result in SmartDebug displaying incorrect values for zeroed memory blocks.
- The logical view cannot be reconstructed for:
  - LSRAM/uSRAM for port widths of x1 inferred through RTL.
  - LSRAM/uSRAM configurations when a single net of an output bus is used and others are unused (i.e. A_DOUT[0]/B_DOUT[0] for DPSRAM/uSRAM and RD[0] for TPSRAM). In this scenario, the memories can be read/write using physical view.
  - LSRAM/uSRAM configurations inferred using CoreAHBLtoAXI (Verilog flow), CoreFIFO (Verilog and VHDL flow).
  - HDL modules inferring RAM blocks that are instantiated in SmartDesign.
  - TPSRAM with ECC enabled.

  Workaround: There are no workarounds for the issues above currently.

4.17.2 PolarFire Transceiver Support Limitations

- Plot Eye introduces a burst of errors in data traffic on Transceiver Interface lanes when started for lanes configured in CDR mode. This will be fixed in an upcoming Libero SoC PolarFire release.

  Workaround: Enable Eye Monitor using the Power On Eye Monitor option before starting the traffic. This will power on the DFE and EM receivers in CDR mode and no spurious errors will be seen during eye plot.

- The Custom DFE solution (using the Optimize DFE option in the Eye Monitor tab) does not work when the transceiver is configured in 8B10B PCS-PMA mode and the receiver is DFE.

  Workaround: Perform the following steps to obtain the expected eye output:

a. Assert PCS RX RESET
b. Optimize DFE
c. Plot Eye
d. De-Assert PCS RX RESET

- The SmartBERT IP does not work when lanes are configured at 250Mbps data rate.
- SmartBERT IP PRBS tests take more time to start/stop/inject error on RHEL 7.x and Cent OS 7.x platforms as compared to RHEL 6.x and Windows OS. This issue is seen only with PRBS patterns from the SmartBERT IP. This will be fixed in an upcoming Libero SoC PolarFire release.
- During the Static Pattern Transmit operation, the Receiver PLL (RX PLL) does not lock to the max run length pattern when looped back from TX to RX.
- SmartBERT IP PRBS tests do not work when the first Transceiver lane uses an internal pattern (PRBS from XCVR PMA) and the following lane uses a SmartBERT pattern (PRBS from SmartBERT IP).
- The Power ON eye monitor Tcl command (eye_monitor_power) does not work correctly in Programming and Debug Tools v12.3. The Receive PLL does not lock to the incoming data after this Tcl command is run. This will be fixed in an upcoming Libero SoC PolarFire release.

Workaround: There are no workarounds for the above issues.

- Designs using PCIe1 controller:
  - RXPLL lock status is not shown in the Configuration Report UI of Debug XCVR. This will be fixed in an upcoming Libero SoC PolarFire release.
  - Signal Integrity parameters are shown in the Configuration Report UI of Debug XCVR. This will be fixed in an upcoming Libero SoC PolarFire release.
- Designs using Dual PCIe i.e. PCIe0 and PCIe1:
  - PCIe debug is not supported for designs using dual PCIe controllers. This will be fixed in an upcoming Libero SoC PolarFire release.

4.17.3 PolarFire Signal Integrity Support Limitations

- The RX Polarity Signal Integrity parameter (Polarity P/N reversal) has no effect when a PDC file is imported using the Import option in SmartDebug. This flow works without errors in GUI mode. This will be fixed in an upcoming Libero SoC PolarFire release.

4.17.4 PolarFire FPGA Hardware Breakpoint (FHB) Limitations

- Soft Reset behavior is not consistent when the DUT is clocked at frequencies less than 160MHz. In such cases, the device may not respond to a Soft Reset operation initiated from the FHB UI. A potential workaround is to do the following:
  a. Halt the DUT via Live Probe.
  b. Initiate a Soft Reset operation using the FHB UI.
  c. Halt the DUT again via Live Probe.

4.17.5 SmartFusion2/IGLOO2 FPGA Hardware Breakpoint (FHB) Limitations

- Live Probe channel assignment using a static signal (connected to GND) halts the DUT. If this occurs, initiate the Soft Reset operation using the FHB UI to restart the DUT.

4.17.6 RTG4 FPGA Hardware Breakpoint (FHB) Limitations

- Synthesis fails when FHB auto instantiation is enabled on designs containing FCCC modules using instantiation flow (i.e. FCCC modules instantiated in RTL files).
- Live Probe channel assignment using a static signal (connected to GND) halts the DUT. If this occurs, initiate the Soft Reset operation using the FHB UI to restart the DUT.

- Halting a clock domain driven by a CCC will also halt all four clock domains belonging to the CCCs in the design. This is a silicon limitation.
- FHB is not supported for cascaded CCCs (CCCs that rely on other CCC outputs to source the reference/feedback clocks). FHB is auto instantiated, but the PLAY/HALT/STEP operations do not work.

4.17.7 RTG4 LSRAM Data corruption

- LSRAM Data corruption is seen on doing a read to LSRAM configured in 512x36 mode through SmartDebug on the active address location.

4.17.8 Standalone SmartDebug Limitations

- Microchip devices present in a chain along with non-Microchip devices cannot be debugged using standalone SmartDebug. In addition, the ID code of Microchip devices cannot be read in this scenario.

  Workaround: Use SmartDebug through Libero to perform these operations.
- Programming fails for all device families when a standalone SmartDebug project is created using the "Construct Chain Automatically" option, and a DDC file is imported in the Programming Connectivity and Interface dialog.

  Workaround:

  a. Close and reopen the Programming Connectivity and Interface UI after importing the DDC file contents in Programming Connectivity and Interface, and then click **Run Program Action**.

  (or)

  b. Create a project by importing the DDC file (without Auto-construct).
- If TCK frequency is set in the Programmer Settings in Standalone SmartDebug, it is not reflected in the SmartDebug operations for SmartFusion2, IGLOO2, RTG4 and PolarFire devices.

  Workaround: Set TCK frequency; program the device and then use SmartDebug features to debug. This will be fixed in an upcoming Libero SoC PolarFire release.
- Standalone SmartDebug User Guide fails when invoked from the UI.

  Workaround: There is no workaround for this; it will be fixed in an upcoming Libero SoC PolarFire release.
- FlashPro6 programmer will not be detected during SmartDebug project creation when SmartDebug is invoked for the first time after the installation of Program and Debug software.

  Workaround: Exit the SmartDebug instance, invoke a new instance of SmartDebug, and project creation will be successful.
- In Standalone SmartDebug, for designs containing security settings, program action (for a device that was already programmed with security settings) and erase action done in Programming Connectivity and Interface result in failure.

  Workaround: Use FlashPro Express or SmartDebug through Libero to Erase/Program the device for designs containing security settings. This will be fixed in an upcoming Libero SoC PolarFire release.
- Read eNVM in Standalone SmartDebug fails when security settings are enabled on the design.

  Workaround: Use SmartDebug through Libero to read eNVM when security settings are enabled on the device. This will be fixed in an upcoming Libero SoC PolarFire release.
- Project Checksum warning message gets retained after programming the device when debug project is created using import DDC option.

  Workaround: Close and reopen the debug project to clear the warning message.

  This will be fixed in an upcoming Libero SoC PolarFire release.

4.18 PolarFire Power Estimator

A PolarFire device with no IOs that is kept active using 1.8V supply draws current roughly in the range of 10mA@25C, which is not reported by the power tools.

4.19 Secure Production Programming Solution

4.19.1 Job Manager may crash during the Import Job Status operation

Running the Import Job Status operation may cause Job Manager to crash. This may happen for designs where the User ECC Key mode is enabled, targeting SmartFusion2 or IGLOO2 M2S/M2GL060, 090, or 150 devices.

4.19.2 Job Manager crashes when opening an existing Job Manager project from v11.9

Job Manager v12.3 does not support Job Manager project files created with releases prior to v12.0.

4.19.3 Job Manager does not support PolarFire DAT export

PolarFire DAT file bitstream export from Job Manager is not supported in Libero SoC v12.3.

4.19.4 SmartFusion2/IGLOO2: eNVM update protection with FlashLock is no longer supported

Due to a silicon limitation, eNVM update protection with FlashLock has been defeatured. If a JDC file generated with a pre-v12.0 version of Libero SoC had the eNVM set to be protected by passkey, it must be regenerated with Libero SoC v12.3 without eNVM FlashLock Protection enabled. eNVM update protection continues to be provided by User Encryption Keys (UEK1, UEK2 or UEK3).

4.19.5 ERASE Action failure for FlashPro Express Job

If a HSM FlashPro Express job has tickets for PROGRAM and ERASE actions, without a ticket for the VERIFY action, the ERASE action will fail. To successfully run the ERASE action, ensure that a ticket for the VERIFY action is included.

4.19.6 Job Manager init_bitstream Tcl command limitation

On Windows, when you run non-HSM flow using Job Manager on PC, if the "enable_passkey_export" option in init_bitstream Tcl command is not specified, the exported bitstream files may include passkeys.

Workaround: You must explicitly set the "enable_passkey_export" option to either TRUE or FALSE in the init_bitstream Tcl command to export the correct bitstream files.

4.20 Identify Debugger

4.20.1 Identify Instrumentor may hang on some Windows 10 machines

When the Identify Instrumentor is opened in Integrated mode on certain machines, the tool opens, but, upon interaction, it freezes. This is an isolated issue and happens in rare Windows 10 OS configurations.

Workaround: Use the Standalone Identify Instrumentor.

4.20.2 Identify Debugger is not supported with FlashPro6 Hardware

The Identify Debugger packaged with Libero SoC v12.3 does not support the new FlashPro6 programming hardware. Support will be added in a future release of Identify, to be released standalone on the Microsemi website.

4.21 Simulation stuck with Aldec Simulators

~~PCIe~~ BFM simulation gets stuck after one write-read BFM command while using PF_SRAM_AHBL_AXI core in Active HDL and Riviera Pro Aldec simulators.

Workaround: If you are using Aldec Simulators, you must manually change the generated CoreAXI4SRAM_MAINCTRL.v file as shown below.

At line number #373.
Comment/remove below lines in starting of always block.

```
//wr_req_gnt = 1'b0;
//rd_req_gnt = 1'b0;
```

And explicitly set for each state:
In REQ_IDLE_ST state:

```
wr_req_gnt = 1’b0; rd_req_gnt = 1’b0;
```

In REQ_WR_ST state:
wr_req_gnt = 1’b1; rd_req_gnt = 1’b0;

In REQ_RD_ST state:
wr_req_gnt = 1’b0; rd_req_gnt = 1’b1;

In default state:
wr_req_gnt = 1’b0; rd_req_gnt = 1’b0;

4.22 Installation and System Limitations

4.22.1 FlashPro6 driver re-installation reports error message

Customers with FlashPro6 drivers previously installed on their system may see the following message at the end of the installation:

```
“The installation of Program Debug Tool v12.3 is finished, but some errors
occurred during the install. Please see the installation log for details.”
```

Resolution: Uninstall existing FlashPro6 drivers and restart the system before installing Libero SoC v12.3. If the software is already installed, ignore the above message if installation logs do not report any errors.

4.22.2 Libero does not run on 8TB File Systems

Libero is currently only supported for partitions 2TB or smaller. If either the Libero install or the Libero project is located on a partition that is larger than 2TB, file access errors or tool crashes may occur. Support for larger partitions is expected to be added in an upcoming release.

4.22.3 4K and 8K screens are not supported

4K and 8K screens are not supported in the Libero SoC v12.3 release.

4.22.4 Installation on Local Drive Only

This release is intended for installation only on a local drive. The Installer might report permission rights problems if the release is installed across a networked drive.

4.22.5 Visual C++ Redistributable Installation Error

On some machines, the installer may display a message stating:

> "The installation of Microsoft Visual C++ Redistributable Package (x86) appears to have failed. Do you want to continue the installation?"

The above error message is benign. If it is seen, click Yes and Libero SoC v12.3 will be installed successfully.

4.22.6 Installation on Windows 7

During Libero SoC v12.3 installation on Windows 7 machines, you may see pop-up warning messages about shortcuts toward the end of installation process.

These messages can be safely ignored. Click OK to close the pop-up windows and the installation will proceed and complete as expected. All Windows shortcuts will appear correctly.

4.22.7 Installation fails when there is insufficient space

- In Libero SoC v12.3, the web installer quits without any user notification or error message when there is insufficient space for the installation. In addition, the estimated space for the installation is incorrect – it reads as approximately 236MB required. Ensure that there is at least 20GB free space on the target hard drive before invoking the installer.

  The DVD installer will also not proceed if there is insufficient space.
- Linux installer fails the first time as IATEMPDIR is not set.

4.22.8 Windows Standalone Installer: Spaces in Extraction Path

During installation of the standalone (DVD) version, the folder to which the zip file is extracted must not contain spaces. If spaces are present, invocation of the installer will fail with the error *"Windows cannot find '<truncated path to extracted folder>'. Make sure you typed the name correctly, and then try again"*. Rename and/or move the extracted folder to one without spaces (in the entire path).

4.22.9 Linux Package Note

- In Libero SoC v12.3, the script bin/check_linux_req/check_linux_req.sh incorrectly reports that the Linux package xz.i686 is required for RHEL/CentOS 7.x. Package xz.i686 is not required. The correct required packages are xz-libs.x86_64 and xz-libs.i686.
- If the installer does not come up in graphical mode, additional X window system libraries might be required. For RHEL/CentOS, the following system packages are recommended:

  ```
  $ sudo yum install -y libXau libX11 libXi libxcb libXext libXtst libXrender
  ```

4.22.10 Antivirus Software Interaction

Many antivirus and HIPS (Host-based Intrusion Prevention System) tools will flag executables and prevent them from running. To eliminate this problem, users must modify their security setting by adding exceptions for specific executables. This is configured in the antivirus tool. Contact the tool provider for assistance.

Many users are running Libero SoC PolarFire successfully with no modification to their antivirus software. Microchip is aware of issues for some antivirus tool settings that occur when using Symantec, McAfee, Avira, Sophos, and Avast tools. The combination of operating system, antivirus tool version, and security settings all contribute to the end result. Depending on the environment, the operation of Libero SoC v12.3, ModelSim ME and/or Synplify Pro ME may or may not be affected.

All public releases of Libero software are tested with several antivirus tools before they are released to ensure that they are not infected. In addition, the Microchip software development and testing environment is also protected by antivirus tools and other security measures.

4.23 RTG4CCCECALIB generation fails when only local clock outputs are used

Generation of the RTG4CCCECALIB configurator fails when only local clock outputs are used.

Workaround:

To use local clocks Y[0..3], select the GL associated with Y[0..3] which has lower frequency

5 System Requirements

The Libero SoC v12.3 release has the following system requirements:

- 64-bit OS
  - Windows 7, or Windows 10 OS
  - RHEL 6.6-6.11, RHEL 7.2-7.6, CentOS 6.6-6.11, and CentOS 7.2-7.6
- A minimum of 16 GB RAM

Note: Setup instructions for using Libero SoC v12.3 on Red Hat Enterprise Linux OS or CentOS are available here. As noted in that document, installation now includes running a shell script (bin/check_linux_req.sh) to confirm the presence of all required runtime packages.

6 Download Libero SoC v12.3 Software

The following are available for download:

- Libero SoC v12.3 for Linux
- Libero SoC v12.3 for Windows
- Mega Vault (Linux)
- Mega Vault (Windows)

Note: Installation requires administrative privileges.

After successful installation, clicking **Help-> About Libero** will show Version: 12.800.0.16

7 Appendix: Sample Programming and SmartDebug Times Using FlashPro5/FlashPro6

The tables in this appendix show sample programming times and SmartDebug runtimes using FlashPro5 and FlashPro6 programmers.

7.1 Microchip FPGA Array Programming

The following table shows sample PPD programming times of the FPGA Array.

Devices[1]	PPD Programming Time[2] (mm:ss)		
	FlashPro5	FlashPro6	
	TCK=4MHz USB 2.0	TCK=4MHz USB 2.0/3.0	TCK=20MHz[3] USB 2.0/3.0
M2S/A2GL 050	2min 9sec	2min 10sec	2min 2sec
M2S/A2GL 150	4min 21sec	4min 19sec	3min 54sec
RTG4	2min 10sec	1min 56sec[4]	1min 33sec[4]
MPF100	39sec	28sec	23sec
MPF200	1min 3sec	43sec	28sec
MPF300	1min 33sec	1min 4sec	43sec
MPF500	1min 57sec	1min 34sec	1min

[1] FlashPro6 supports JTAG programming for all SmartFusion2, IGLOO2, RTG4 and PolarFire devices.
[2] To benefit from the improved programming time using FlashPro6, use the PPD file format for SmartFusion2, IGLOO2 and PolarFire devices.
[3] To ensure successful programming at 20MHz TCK, appropriate steps need to be taken to ensure signal integrity of the JTAG signals.
[4] New and improved programming time for RTG4 starting with Libero SoC/FlashPro Express v12.3 and later.

7.2 SPI Flash Programming

The following table shows sample SPI Flash (10MB) Programming time using the PolarFire Splash Kit.

(N25Q00AA13GSF40G / MT25QL01GBBB8ESF-0SIT TR)[1] 10MByte data	SPI Flash Programming Time				
	FlashPro5		FlashPro6[2]		
	TCK = 4MHZ	TCK = 15MHz[3]	TCK = 4MHZ	TCK = 15MHz[3]	TCK = 20MHz[3]
	USB 2.0	USB 2.0	USB 2.0/3.0	USB 2.0/3.0	USB 2.0/3.0
Erase and Program SPI Flash[4]	8min 15sec	4min 58sec	14min 53sec	5min 45sec	4min 54sec
Verify SPI Flash	1hr 57min 38sec	1hr 50min 45sec	16min 33sec	7min 53sec	7min 04sec
Read SPI Flash	2hrs 02min 43sec	1hr 55min 30sec	16min 12sec	7min 36sec	6min 47sec
Erase SPI Flash	18sec	18sec	1min 52sec	1min 50sec	1min 50sec

NOTES:

[1]SPI Flash programming has been tested on N25Q00AA and MT25QL01G/MT25QU01G devices only. Contact technical support for other SPI-Flash device support needs.

[2]FlashPro6 has longer erase and programming times for SPI Flash devices, when compared to FlashPro5. However, readback and verification times are significantly shorter. As a result, the total combined Erase, Program and Verify time is significantly lower compared to FlashPro5. Programming time for FlashPro6 will be improved in future releases.

[3]To successfully program the device at a high TCK frequency, appropriate steps must be taken to ensure signal integrity of the JTAG signals.

[4]SPI Flash programming time may vary from device to device even though the part number is the same. This is due to die to die variation.

7.3 SmartDebug Runtime Samples

The following table shows sample runtimes of some SmartDebug key functions.

SmartDebug Function Runtimes		
SmartDebug Operations	**FlashPro5**	**FlashPro6[1]**
	TCK = 4MHZ	**TCK = 4MHZ**
	USB 2.0	**USB 2.0/3.0**
Active Probe Read (13,000 probe points)	28 sec	1 sec
Active Probe Write (13,000 probe points)	35 sec	6 sec
Logical View Read of LSRAM (340 LSRAM Blocks)	20 min	<5 min
Logical View Read to USRAM (32 USRAM Blocks)	1 sec	1 sec
FHB - Waveform dump to VCD file (160 probe points; 1,000 cycles)	7 min	25 sec

NOTES:

[1]FlashPro6 SmartDebug runtime is applicable for SmartDebug v12.3 and later only.