# UG0902
# User Guide
# PolarFire SoC FPGA Packaging and Pin Descriptions

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# Contents

1 PolarFire SoC FPGA Packaging and Pin Descriptions . . . . . . . . . . . . . . . . . . . . . . . . 6
1.1 Packaging Overview . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 6
1.2 Bank Locations . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 6
1.3 Packaging Pin Assignment . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 8
1.4 Pin Descriptions . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 8
1.4.1 User I/O . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 8
1.4.2 MSS I/Os . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 9
1.4.3 Supply Pins . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 11
1.4.4 Memory Interface . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 12
1.4.5 DDR Interface . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 12
1.4.6 Clocking Pins . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 13
1.4.7 Dedicated I/O Bank Pins . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 13
1.4.8 XCVR Interface . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 15
1.5 Package Pin-outs . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 15
1.6 Mechanical Drawings . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 16
1.7 Package Material Information . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 18
1.8 Thermal Specifications . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 19
1.9 Package Marking . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 19
1.10 Packing and Shipping . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 19
1.11 Thermal Management . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 19
1.11.1 System Level Heat Sink Solutions . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 20
1.12 Thermal Interface Material . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 20
1.12.1 Heat Sink Attachments . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 20
1.13 Heat Sink Guidelines for Bare-die Flip-Chip Packages . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 21
1.14 Heat Sink Removal Procedure . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 21
1.15 Recommended PCB Design Rules for BGA Packages . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 22
1.16 Moisture Sensitive Level . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 23

2 Revision History . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 24
2.1 Revision 1.0 . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 24

# Figures


Figure 1 PolarFire SoC MPFS250T-FCG1152 I/O Bank Locations . . . . . 6
Figure 2 PolarFire SoC MPFS250T-FCVG 484 I/O Bank Locations . . . . . 7
Figure 3 MSS I/O Block Diagram . . . . . 10
Figure 4 MPFS250T-FCG1152 Package Top-View and Side-View . . . . . 16
Figure 5 MPFS250T-FCG1152 Package Bottom-View . . . . . 17
Figure 6 MPFS250T-FCVG484 Package Top-View and Side-View . . . . . 17
Figure 7 MPFS250T-FCVG484 Package Bottom-View . . . . . 18
Figure 8 Heat Spreader with Thermal Interface Material . . . . . 19
Figure 9 Cross Section of Bare-die Flip-chip BGA . . . . . 21
Figure 10 Recommended Application of Heat Sink . . . . . 21
Figure 11 Ball and Via Dimensions . . . . . 22

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# Tables


Table 1 Organization of I/O Banks . . . . . 7
Table 2 Serial Transceiver Channels . . . . . 8
Table 3 Supported I/O Features . . . . . 9
Table 4 Supply Pins . . . . . 11
Table 5 Packaging Decoupling Capacitors . . . . . 12
Table 6 Package De-capacitor Part Number and ESR Values . . . . . 12
Table 7 JTAG Pins . . . . . 13
Table 8 Device Reset Pins . . . . . 13
Table 9 SPI Interface Pins . . . . . 13
Table 10 Special Pins . . . . . 14
Table 11 XCVR Interface Pins . . . . . 15
Table 12 PolarFire SoC FPGAs Package Information . . . . . 18
Table 13 PolarFire SoC Ball Grid Array RoHS Packages . . . . . 18
Table 14 PolarFire SoC Ball Grid Array Leaded Packages . . . . . 19
Table 15 Standard Device Counts per Tray and Carton . . . . . 19
Table 16 Recommended PCB Design Rules . . . . . 22
Table 17 Moisture Sensitive Levels . . . . . 23

# 1 PolarFire SoC FPGA Packaging and Pin Descriptions

This guide provides pin and packaging information (such as bank assignments and mechanical information) for PolarFire® SoC FPGAs.

PolarFire SoC FPGAs feature a flexible I/O structure that supports a range of mixed voltages (1.1 V, 1.2 V, 1.35 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V) through bank selection. The HSIO and GPIO are configured as differential I/Os or two single-ended I/Os. For more information about HSIO, GPIO, and supported I/O standards, see *PolarFire SoC FPGA User I/O User Guide* (Yet to be published).

## 1.1 Packaging Overview

PolarFire SoC FPGAs are available in multiple packages. Each package (device variant) has various I/O banks to allow the flexibility of using different I/O standards. HSIO and GPIO banks have a maximum supply voltage of 1.8 V and 3.3 V, respectively.

The following table lists the PolarFire SoC FPGA variants, with user I/O and XCVR lanes, in Pb-free packages.

Table to be added.

## 1.2 Bank Locations

PolarFire SoC FPGA I/O are grouped based on I/O voltage standards and I/O capabilities. Each I/O bank has dedicated I/O supplies and ground voltages. Because of these dedicated supplies, only I/O with compatible standards are assigned to the same I/O voltage bank.

The following illustrations show the bank locations for the MPFS250Tdevice with available package combinations.

***Figure 1 •*** **PolarFire SoC MPFS250T-FCG1152 I/O Bank Locations**

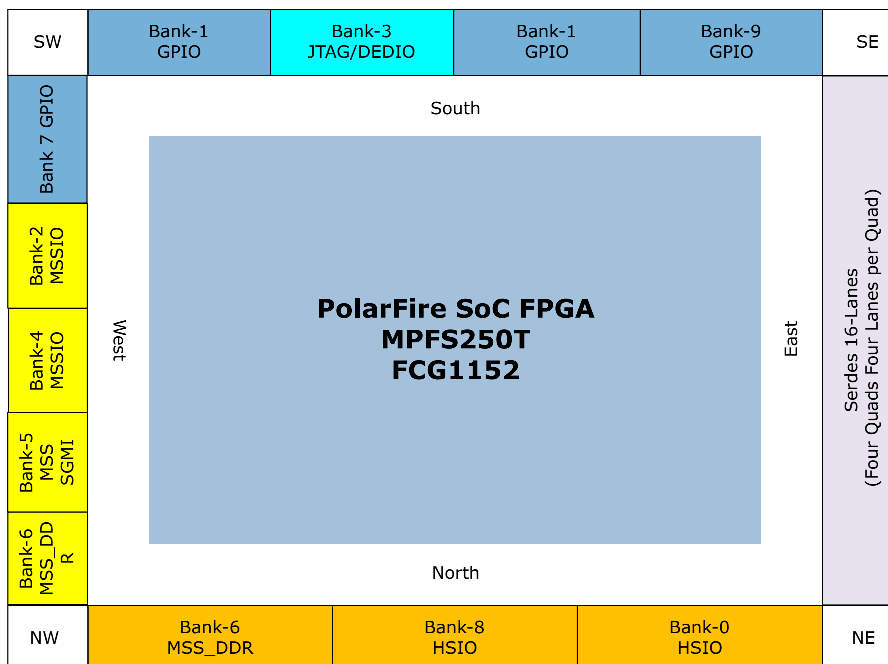
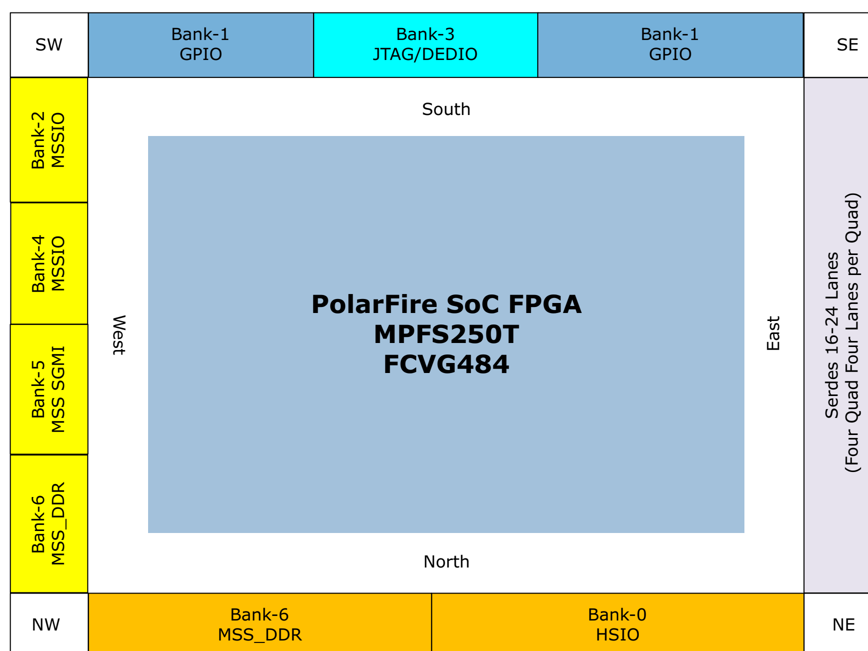


*Figure 2 •* **PolarFire SoC MPFS250T-FCVG 484 I/O Bank Locations**




The following table lists the organization of the I/O banks in PolarFire SoC MPFS250T device in FCG1152 and FCVG484 packages. Each XCVR supports four lanes in every package. In all the packages, PCIe is supported only in XCVR0.

*Table 1 •* **Organization of I/O Banks**

| Bank Number | FCG1152 | FCVG484 |
|---|---|---|
| | MPFS250T | MPFS250T |
| Bank 0 | HSIO | HSIO |
| Bank 1 | GPIO | GPIO |
| Bank 2 | MSSIO | MSSIO |
| Bank 3 | JTAG/<br>FIXED I/O | JTAG/<br>FIXED I/O |
| Bank 4 | MSSIO | MSSIO |
| Bank 5 | MSS-SGMII | MSS-SGMII |
| Bank 6 | MSS-DDR | MSS-DDR |
| Bank 7 | HSIO | |
| Bank 8 | HSIO | |
| Bank 9 | GPIO | |
| XCVR 0 | Yes | Yes |
| XCVR 1 | Yes | |
| XCVR 2 | Yes | |
| XCVR 3 | Yes | |

Each I/O bank supports multiple DDR lanes. If CDR/SGMII interface is connected to the I/O bank, the Tx and Rx signal must be within the same DDR Lane. Only one CDR/SGMII is allowed per DDR lane. For

more information about DDR lanes for each package in *PolarFire SoC Packaging Pin Assignment Table* (PPAT).

The following table lists the XCVR channels for PolarFire SoC device/package.

***Table 2 •*** **Serial Transceiver Channels**

| Device | FCG1152 | FCVG484 |
|---|---|---|
| **MPFS250T** | 16 | 4 |

## 1.3 Packaging Pin Assignment

*PolarFire SoC Packaging Pin Assignment Table* (PPAT) contains information about recommended DDR pin-outs, PCI Express capability for XCVR-0, DDR Lane information for IO CDR, and generic IOD interface pin placement.

## 1.4 Pin Descriptions

PolarFire SoC devices have user I/O (GPIO/HSIO) pins, dedicated I/O bank pins, memory interface, XCVR interface, clocking pins, and supply pins.

### 1.4.1 User I/O

PolarFire SoC FPGA I/Os are paired up to meet the differential I/O standards and grouped into lanes of 12 buffers with a lane controller for memory interfaces. For more information about the memory controller, see *PolarFire SoC FPGA DDR Memory Controller User Guide* (yet to be published).

There are two types of I/O buffers—HSIO and GPIO. HSIO is optimized for 1.2 Gbps (DDR4) operation with operating supplies between 1.1 V and 1.8 V. GPIO buffers support a wider range of I/O interfaces with speeds of up to 1066 Mbps when using single-ended standards and 1.25 Gbps when using differential standards, and operating supplies ranging from 1.2 V to 3.3 V. GPIO supports multiple standards, including 3.3 V with an integrated Clock Data Recovery (CDR) to high-speed serial interfaces such as 1GbE.

Each PolarFire SoC FPGA user I/O uses a IOxyBz naming convention, where:

- **IO** = the type of I/O.
- **x** = the I/O pair number in bank z.
- **y** = P (positive) or N (negative). In single-ended mode, the I/O pair operates as two separate I/O—P and N. Differential mode is implemented with a fixed I/O pair and cannot be split with an adjacent I/O.
- **B** = bank (see note in Supported I/O Features, page 9).
- **z** = bank number.

GPIOxyBz and HSIOxyBz are bi-directional user I/O pins that are capable of differential signaling.

#### 1.4.1.1 Supported I/O Features

The following table lists the I/O features supported on HSIO and GPIO.

***Table 3 •*** **Supported I/O Features**

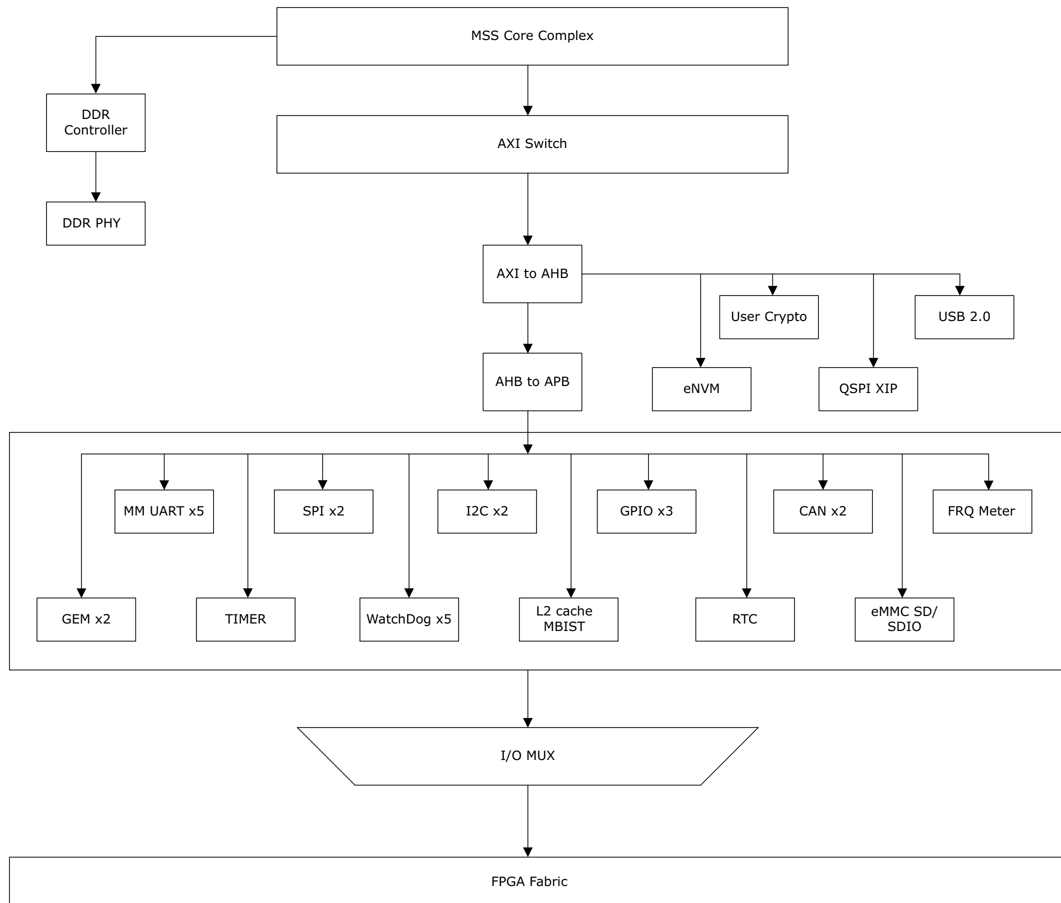
| I/O Feature | HSIO | GPIO | Additional Information |
|---|---|---|---|
| Programmable on/off clamp | | Yes | |
| Hot-plug | | Yes | |
| Cold sparing | Yes | Yes | |
| True differential output driver | | Yes | |
| Programmable on/off 100 Ω differential termination | | Yes | |
| PVT-compensated output drive | Yes | Yes | |
| Programmable slew control | | Yes | |
| PVT compensated slew control | Yes | | |
| Programmable input hysteresis | Yes | Yes | |
| Mobile Industry Processor Interface (MIPI) (input) | | Yes | High-speed and low-power. |
| MIPI (output) | | Yes | High-speed. |

**Note:** Bank 5 VDDI power pins are connected to Bank 4 VDDI power pins within package substrates for pin migration compatibility.

### 1.4.2 MSS I/Os

The PolarFire SoC family offers the industry's first RISC-V based SoC FPGAs. The PolarFire SoC family combines a powerful 64-bit 5x core RISC-V Microprocessor Sub-System (MSS) with the FPGA fabric in a single device. Packed with this powerful combination, PolarFire SoC devices offer the scalable features of FPGAs and high-performance of ASICs. Only the FPGA fabric resources vary and the MSS remains the same across PolarFire SoC device variants, making these devices ideal for many applications.

***Figure 3 •*** **MSS I/O Block Diagram**




There are 38 MSS I/Os which can be configured using the Libero SoC software to interface with various peripherals. Refer (add link) for the pin out information for the MSS pins. The pin out provided multiple options on where the MSS peripherals may be connected. All the interfaces are configured using the software.

- CAN Controller (x2)
- I2C (x2)
- MMUART (x5)
- SPI (x2)
- Quad SPI with XIP
- Gigabit Ethernet MAC (GEM x2)
- eMMC SD/SDIO
- Universal Serial Bus OTG Controller (USB)
- DDR Controller
- GPIO

## 1.4.3 Supply Pins

The following table lists multiple power supply pins required for proper device operation. For more information on power sequence, see *UG0901: PolarFire SoC FPGA Board Design Guidelines User Guide*.

**Table 4 • Supply Pins**

| Name | Description | Operating Voltage | Unused Condition |
|---|---|---|---|
| XCVR_VREF[1] | Voltage reference for transceiver. | 0.9 V/1.25 V | Connect to VSS through a 10 KΩ resistor. |
| VDD_XCVR_CLK[2] | Power for transceiver reference clock input buffers. | 2.5 V/3.3 V | 2.5 V/3.3 V or connect to VSS through a 10 KΩ resistor, see *PolarFire SoC FPGA Transceiver User Guide* (yet to be published). |
| VDDA25 | Transceiver PLL power | 2.5 V | 2.5 V or connect to VSS through 10k resistor. |
| VDDA | Power for transceiver Tx and Rx lanes 0, 1, 2, 3. | 1.0 V/1.05 V | 1.0 V/1.05 V or connect to VSS through 10k resistor. |
| VSS | Core digital ground. | NA | Must connect to the ground. |
| VDD | Device core digital supply. | 1.0 V/1.05 V | Must connect to the core supply. |
| VDDIx (JTAG Bank)[2] | Supply for I/O circuits in a bank. | 1.8 V/2.5 V/3.3 V | 1.8 V/2.5 V/3.3 V |
| VDDIx (GPIO Banks) | Supply for I/O circuits in a bank. | 1.2 V/1.5 V/1.8 V/2.5 V/3.3 V | 1.2 V/1.5 V/1.8 V/2.5 V/3.3V or connect to VSS through a 10 KΩ resistor. |
| VDDIx (MSSIO Banks) | Supply for MSS I/O circuits in a bank. | 1.2 V/1.5 V/1.8 V/2.5V/3.3V | 1.2 V/1.5 V/1.8 V/2.5V/3.3V or connect to VSS through a 10 KΩ resistor. |
| VDDIx (MSS SGMII Banks) | Supply for MSS SGMII circuits in a bank. | 2.5V/3.3V | 2.5V/3.3V or connect to VSS through a 10 KΩ resistor |
| VDDIx (MSS DDR Bank) | Supply for MSS DDR circuits in a bank. | 1.2V/1.5 V/1.8 V | 1.2V/1.5 V/1.8 V or connect to VSS through a 10 KΩ resistor |

1. SSTL25 (stub series terminated logic) I/O standard for 1.25 V VREF, SSTL18 I/O standard for 0.9 V, and HSUL18 I/O standard for 0.9 V.
2. The VDDIx (JTAG bank) and VDD_XCVR_CLK operating voltage should not be more than 2.5 V. Future releases would support an operating voltage, ranging from 2.5 V to 3.3 V.

### 1.4.3.1 Packaging Decoupling Capacitors

PolarFire SoC 0.8 mm and 1.0 mm pitch packages contain decoupling capacitors to support high-speed I/O operation.

Small, low-profile CSP packages (0.5 mm ball pitch, 16 mm × 16 mm and smaller) do not have package decoupling capacitors.

The following table lists the packaging decoupling capacitors contained in non-CSP packages.

***Table 5 •*** **Packaging Decoupling Capacitors**

| Power Supply | 0.8 mm Pitch | | 1 mm Pitch | |
|---|---|---|---|---|
| | Number of Capacitors | Value | Caps available | Value |
| VDDI0 | | | 1 | 1 µF/4 V |
| VDDI1 | | | 1 | 1 µF/4 V |
| VDDI2 | | | TBD | |
| VDDI4 | | | TBD | |
| VDDI5 | | | TBD | |
| VDDI6 | | | 1 | 1 µF/4 V |
| VDDI7[1] | | | 1 | 1 µF/4 V |
| VDDI8[1] | | | 1 | 1 µF/4 V |
| VDDI9[1] | | | 1 | 1 µF/4 V |
| VDD18 | | | 1 | 1 µF/4 V |
| VDDA | 2 | 4.7nF /6.3 V<br>1.0nF/16.0 V | 4 | 4.7nF/6.3 V<br>2.2 nF/6.3 V<br>1.5 nF/6.3 V<br>1.0 nF/16.0 V |
| VDD25 | | | 1 | 1 µF/4 V |

1. 0.8 mm pitch PolarFire SoC packages do not support VDDI7, VDDI8, and VDDI9.

***Table 6 •*** **Package De-capacitor Part Number and ESR Values**

| Capacitance Value | Part numbers | Package | ESR (Ω) |
|---|---|---|---|
| 4.7 nF | GRM033R70J472KA01 | 0201 | 0.09724812 |
| 2.2 nF | GRM033R70J222KA01 | 0201 | 0.16111 |
| 1.5 nF | GRM033R70J152KA01 | 0201 | 0.194915396 |
| 1 nF | CGA1A2X7R1C102K030BA | 0201 | 0.2444 |
| 1 µF | LLR185C70G105ME01L | 0306 | 0.005475757 |
| 1 µF | LLL185C70J105ME14K | 0306 | 0.005009904 |
| 2.2 µF | W2L14C225MAT1A | 0508 | 0.003964 |

## 1.4.4 Memory Interface

Valid locations for DDR memory interfaces are shown in *PolarFire SoC Packaging Pin Assignment Table*. By using Libero SoC, all individual DDR interface pins are identified from the DDR macro. For more information on the memory interface, see *PolarFire SoC FPGA DDR Memory Controller User Guide* (Yet to be published).

## 1.4.5 DDR Interface

The DDR subsystems are hardened ASIC blocks for interfacing the LPDDR3, DDR3, and DDR4 memories. It supports 16-, 32-, and 64-bit data bus width modes with ECC support. The DDRIO uses fixed impedance calibration for different drive strengths. These values are programmed using Libero SoC software for the selected I/O standard. The values are fed to the pull-up or pull-down reference network

to match the impedance with an external resistor. For more information on DDR signals, see *PolarFire SoC FPGA DDR Memory Controller User Guide* (yet to be published).

### 1.4.6 Clocking Pins

CCC blocks, located at each corner of the PolarFire SoC FPGAs, contain two PLLs and two DLLs that provide flexible on-chip and off-chip clock management and synthesis capabilities. CCCs are labeled according to their locations in the core. For example, the CCC located in the northeast corner is labeled as CCC_NE. For more information on clocking pins, see *PolarFire SoC FPGA Clocking Resources User Guide* (yet to be published).

Preferred clock inputs (CLKIN) are located on three sides of the device, with eight preferred clock inputs on the west side, twelve on the north side, and either 12 or 16 inputs on the south side, depending on the package. The following table lists the clocking pin names and descriptions. See Table 4, page 11 for more information on CCC pin voltage.

### 1.4.7 Dedicated I/O Bank Pins

JTAG, SPI, and DEVRST_N signals share the same bank 3 supply and are not directly available to the fabric. SPI I/O are, however, dynamically switched over to be used by the fabric whenever the PolarFire SoC controller is not using them. Dedicated I/O bank supplies must be powered up higher than their operational threshold and enabled before the PolarFire SoC controller negates the main power-on reset to the FPGA fabric. The following tables list the JTAG, SPI, and DEVRST_N pin names and descriptions. Libero configures unused user I/O as input buffer disabled, output buffer tri-stated with weak pull-up.

***Table 7 •*** **JTAG Pins**

| Name | Direction | Weak Pull-up | Description | Unused Condition |
|---|---|---|---|---|
| TMS | Input | 15 KΩ to VJTAG | JTAG Test Mode Select (TMS). | DNC |
| TDI | Input | 15 KΩ to VJTAG | JTAG data input pin. In ATPG/test mode, when using a 4-bit TDI bus, this I/O is used as TDI[0]. | DNC |
| TDO | Output | | JTAG data out. | DNC |
| TCK | Input | | JTAG clock. | Must connect to VSS through 10 KΩ resistor. |
| TRSTB | Input | 15 KΩ to VJTAG | JTAG reset (asserted low). | Must connect to VDDI3 through 1 KΩ resistor per pin, not to be shared with any other pins. |

***Table 8 •*** **Device Reset Pins**

| Name | Direction | Weak Pull-up | Description | Unused Condition |
|---|---|---|---|---|
| DEVRST_N | Input | 22 KΩ | Device reset (asserted low). | Must connect to VDDI3 through a 1 KΩ resistor per pin, not to be shared with any other pins. |

***Table 9 •*** **SPI Interface Pins**

| Name | Direction | Description | Unused Condition |
|---|---|---|---|
| SCK | Bi-directional | SPI clock. | Must connect to VSS through 10 KΩ resistor. |
| SS | Bi-directional | SPI slave select. | Must connect to VSS through 10 KΩ resistor. |
| SDI | Input | SDI input for the shared SPI interface. | Must connect to VDDI3 through 10 KΩ resistor. |
| SDO | Output | SDO output for the shared SPI interface. | DNC |

***Table 9 •*** **SPI Interface Pins *(continued)***

| Name | Direction | Description | Unused Condition |
|---|---|---|---|
| SPI_EN | Input | Pulled up or down through a resistor or driven dynamically from an external source to enable or tri-state the SPI I/O. | Must connect to VSS through 10 KΩ resistor. |
| IO_CFG_INTF | Input | Pulled up or down through a resistor or driven dynamically from an external source to indicate whether the shared SPI interface is a master or a slave. Dedicated to the system controller.<br>0: SPI slave interface<br>1: SPI master interface | Must connect to VSS through 10 KΩ resistor. |

***Table 10 •*** **Special Pins**

| Name | Direction | Description | Unused Condition |
|---|---|---|---|
| NC | – | No connect pin. This pin indicates that it is not connected within the circuitry. NC pins can be driven by any voltage or can be left floating with no effect on the operation of the device. | – |
| DNC | – | Do not connect pin. DNC pins must not be connected to any signals on the PCB, and they must be left unconnected. | – |
| LPRB_A | Output | Specifies an internal signal for probing (oscilloscope-like feature). The two live probe I/O cells function as either of the following:<br>– Live probe<br>– User I/O (HSIO) | Libero-defined DNC. |
| LPRB_B | Output | | Libero-defined DNC. |
| FF_EXIT_N | Input | RESERVED | – |
| Shield Signal | Output | Shield signal is required for each DDR data byte signal. It must be driven with maximum drive strength to improve the signal integrity. | Only when DDR controller is in use. |

### 1.4.8 XCVR Interface

The transceiver I/O available in the PolarFire SoC devices are dedicated for high-speed serial communication protocols. Libero Defined DNC pins are pulled up internally when not used in the Libero design.

*Table 11 •* **XCVR Interface Pins**

| Name | Direction | Description | Unused Condition |
|---|---|---|---|
| XCVR_xy_REFCLK_P<br>XCVR_xy_REFCLK_N | Input | Differential serial reference clock<br>xy - location<br>x - transceiver number (0, 1, 2, 3)<br>y - lane number (0, 1, 2, 3) | DNC. |
| XCVR_x_TXy_P<br>XCVR_x_TXy_N | Output | Differential serial transmit pins.<br>x - transceiver number (0, 1, 2, 3)<br>y - lane number (0, 1, 2, 3) | Libero-defined DNC. |
| XCVR_x_RXy_P<br>XCVR_x_RXy_N | Input | Differential serial receive pins.<br>x - transceiver number (0, 1, 2, 3)<br>y - lane number (0, 1, 2, 3) | Libero-defined DNC, see *PolarFire SoC FPGA Transceiver User Guide* (yet to be published) |

## 1.5 Package Pin-outs

For more information about the pin-outs, see *PolarFire SoC Packaging Pin Assignment Table*.

## 1.6 Mechanical Drawings

The following illustrations show the top, bottom, and side views and dimensions for the PolarFire SoC FPGAs.

*Figure 4 •* **MPFS250T-FCG1152 Package Top-View and Side-View**

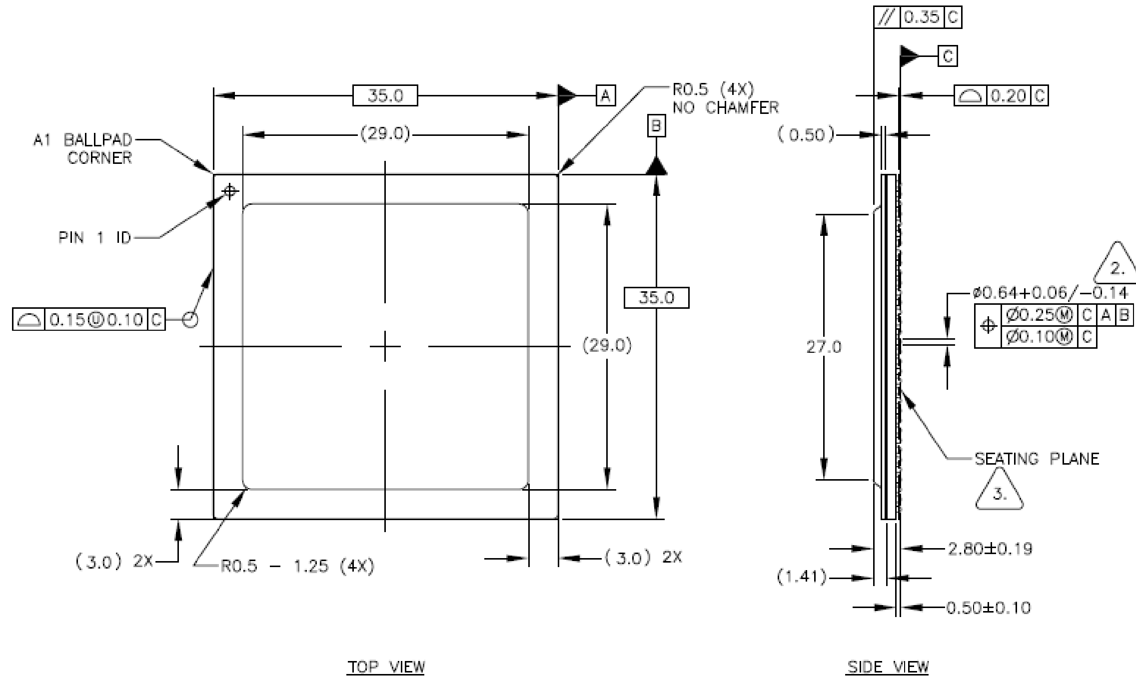


***Figure 5 •*** **MPFS250T-FCG1152 Package Bottom-View**

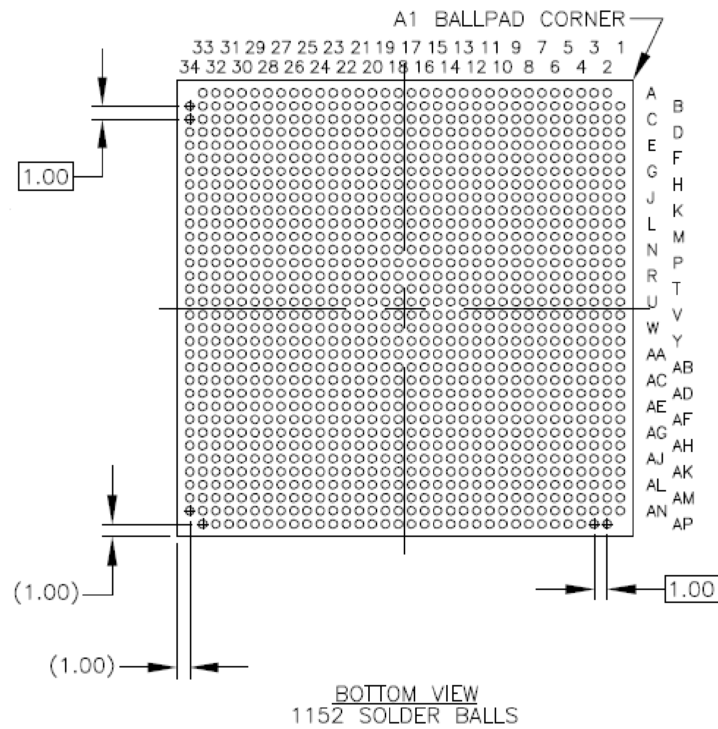



***Figure 6 •*** **MPFS250T-FCVG484 Package Top-View and Side-View**

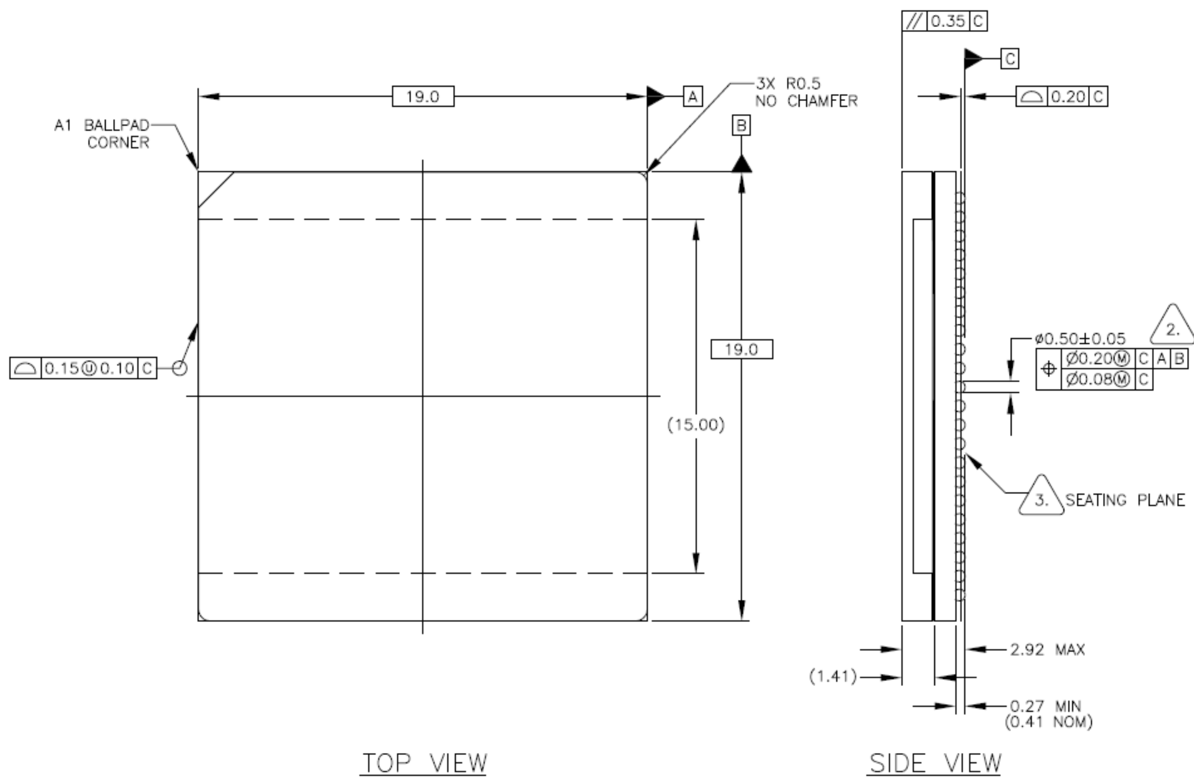
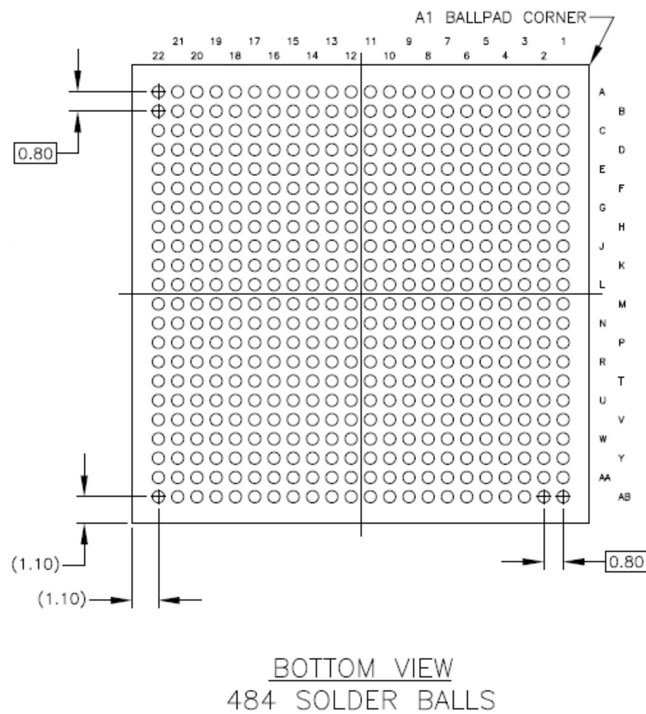


***Figure 7 •*** **MPFS250T-FCVG484 Package Bottom-View**




The following table lists the PolarFire SoC FPGAs Package description and specification.

***Table 12 •*** **PolarFire SoC FPGAs Package Information**

| Package | Description | Package Specifications | | | |
|---|---|---|---|---|---|
| | | **Package type** | **Pitch (mm)** | **Size (mm)** | **Maximum I/Os** |
| FCG1152 | Flip-chip with lid | BGA | 1 | 35 × 35 | 512 |
| FCVG484 | Flip-chip with lid | BGA | 0.8 | 19 × 19 | 284 |

## 1.7 Package Material Information

The following table lists the PolarFire SoC ball grid array RoHS packages.

***Table 13 •*** **PolarFire SoC Ball Grid Array RoHS Packages**

| Package Balls | FCG1152 | FCVG484 |
|---|---|---|
| Package Pitch | 1 mm | 0.8 mm |
| Substrate Material | Epoxy Glass | Epoxy Glass |
| Solder Ball Composition RoHS | SAC305 | SAC305 |
| Solder Bump Material | Sn98.2/Ag1.8 | Sn98.2/Ag1.8 |

All flip-chip BGA packages—FCG1152 and FCVG484—are vented.

***Table 14 •*** **PolarFire SoC Ball Grid Array Leaded Packages**

| Flip-chip Packages | Ball Pad Diameter (mm) | Ball Pad Opening (mm) | Vent Dimension (mm) | Vented Package |
|---|---|---|---|---|
| MPFS250T - FCG1152 (with heat spreader) | TBD | TBD | TBD | TBD |
| MPFS250T - FCVG484 (Bare Die) | TBD | TBD | TBD | TBD |

## 1.8 Thermal Specifications

To be updated.

## 1.9 Package Marking

To be updated.

## 1.10 Packing and Shipping

The PolarFire SoC series devices are packed in trays, which are used to pack most of the Microsemi surface-mount devices. Trays provide excellent protection from mechanical damage. In addition, they are manufactured using the anti-static material to provide limited protection against ESD damage.

***Table 15 •*** **Standard Device Counts per Tray and Carton**

| Package | Maximum Number of Devices Per Tray | Maximum Number Trays Per Stack | Maximum Number of Units per Inner Carton |
|---|---|---|---|
| FCG1152 | TBD | TBD | TBD |
| FCVG484 | TBD | TBD | TBD |

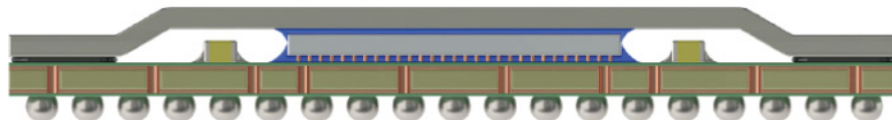
## 1.11 Thermal Management

Microsemi PolarFire SoC FPGAs are offered in lidded flip-chip BGA (FCBGA) format. Lidded FCBGA features a controlled bond-line thermal interface material (TIM) thickness that reduces the thermal resistance (Theta-JC) between the junction and the externally applied thermal solution. The lid or heat spreader also spreads the heat away from the die to the package perimeter and to the printed circuit board.

Optimized package electrical performance with multiple power and ground planes to take care of signal return paths, and dense core via under the die to improve power delivery adds benefit in dissipating heat through the bottom of the package and to the board.

PolarFire SoC FPGAs in FCVG484 are also available in bare die FCBGA. Bare die flip-chip BGA produces the lowest possible thermal resistance (Theta-JC) between the junction and any externally applied thermal solution.

***Figure 8 •*** **Heat Spreader with Thermal Interface Material**



### 1.11.1 System Level Heat Sink Solutions

The use of external heat sinks, component placement in the PCB, and air flow in the system depends on the physical and mechanical limitations of the system. A system level thermal design engineer must understand these limitations and device capabilities to effectively manage the complete thermal strategy.

## 1.12 Thermal Interface Material

When using external heat sinks, a suitable thermal interface material must be considered to effectively transfer the heat from the component to the heat sink, and eventually to the environment.

For bare-die flip-chip BGAs, the surface of the silicon contacts the heat sink. For lidded flip-chip BGAs, the lid contacts the heat sink. The surface size of the bare-die flip-chip BGA and lidded flip-chip BGAs are different. Microsemi recommends a different type of thermal material for long-term use with each type of flip-chip BGAs package.

For lidded flip-chip BGAs, the lid contacts the external heat sink while bare die flip-chip BGAs, the surface of the silicon contacts the external heat sink. The surface areas of lidded flip-chip BGAs and bare die flip-chip BGAs are different. The system level thermal design engineer must choose the appropriate TIM to be used.

Thermal interface material is required because the surfaces of both the PolarFire SoC package and heat sinks base are not smooth. The surface roughness reduces the effective contact area between the package and the heat sinks base. The insulating air gaps created by voids between contacting surfaces are too large. The thermal interface materials fill these gaps and allow an effective conductive transfer of heat from the package to the external heat sink.

The selection of the appropriate thermal interface material is critical to ensure the lowest thermal contact resistance. One must consider the thermal conductivity of the TIM—the flatness of the surface contact areas, the applied pressure on the thermal interface material and the total thermal contact area. In addition to thermal performance, TIMs are selected based on the ease of use in assembly and long term reliability.

### 1.12.1 Heat Sink Attachments

There are six main methods for heat sink attachment. The following table lists their advantages and disadvantages.

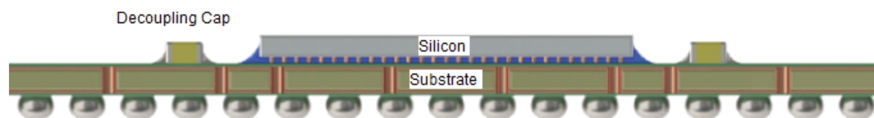
- Thermal tape
- Thermally conductive adhesive
- Wire form Z-clips
- Plastic clip-ons
- Threaded stand-offs (PEMs) and compression springs
- Push-pins and compression springs
- Thermal compound (also called as thermal gel, thermal grease, thermal paste, heat-sink paste or heat-sink compound)

## 1.13 Heat Sink Guidelines for Bare-die Flip-Chip Packages

Heat sinks can be attached to the package in multiple ways. For heat to dissipate effectively, the advantages and disadvantages of each heat sink attachment method must be considered. Factors influencing the selection of the heat sink attachment method include the package type, contact area of the heat source, and the heat sink type.

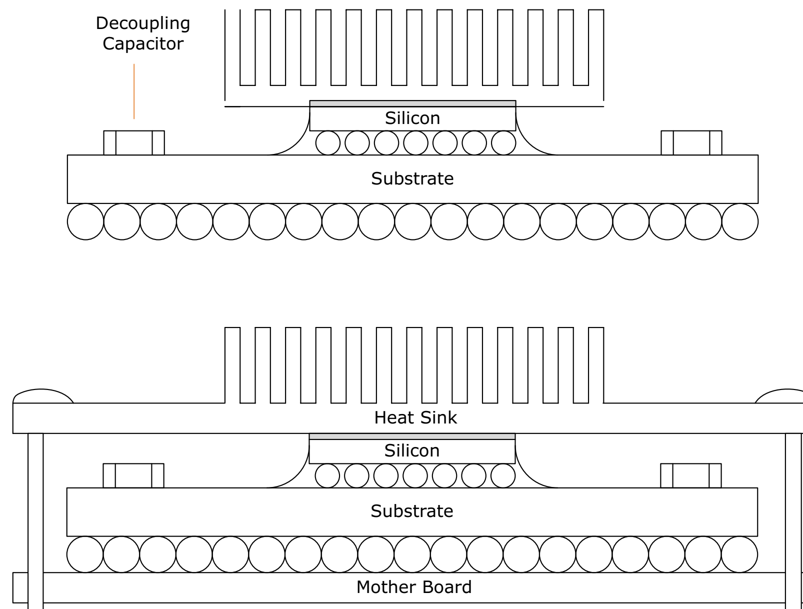
When designing heat sink attachments for bare-die flip-chip BGA packages, the height of the die higher than the substrate and also the height of decoupling capacitors must be considered. This is to prevent electrical shorting between the heat sink (metal) and the decoupling capacitors. When attaching the heat sink to the bare-die flip-chip BGA, ensure that the TIM thickness and the force applied during heat sink placement are even.

***Figure 9 •*** **Cross Section of Bare-die Flip-chip BGA**




Care must be taken while attaching a heat sink to the bare-die package after the component is placed onto the PCBs.

***Figure 10 •*** **Recommended Application of Heat Sink**




## 1.14 Heat Sink Removal Procedure

The heat spreader on the package provides mechanical protection for the die and serves as the primary heat dissipation path. It is attached with an epoxy adhesive to provide the necessary adhesion strength to hold the package together. For an application in which an external heat sink subjects the lid adhesion joint to continuous tension or shear, extra support might be required.

Also, if the removal of an attached external heat sink subjects the joint to tension, torque, or shear, care should be exercised to ensure that the lid itself does not come off. In such cases, it has been found useful to use a small metal blade or metal wire to break the lid to heat sink joint from the corners and carefully pry the heat sink off. The initial cut should reach far in enough so that the blade has leverage to exert upward pressure against the heat sink. Contact the heat sink and heat sink adhesive manufacturer for more specific recommendations on heat sink removal.

# 1.15 Recommended PCB Design Rules for BGA Packages

Microsemi provides the diameter of a land pad on the package side. This information is required before the start of the board layout so the board pads can be designed to match the component-side land geometry. The typical values of these land pads are shown in the following figure and summarized in Table 16, page 22. For Microsemi BGA packages, Non-Solder Mask Defined (NSMD) pads on the board are suggested to allow a clearance between the land metal (diameter) and the solder mask opening (diameter) as shown in the following figure.

The space between the NSMD pad and the solder mask; the actual signal trace widths and via dimensions depend on the capability of the PCB vendor. The cost of the PCB is higher when the line width and spaces are smaller.

***Figure 11 •*** **Ball and Via Dimensions**

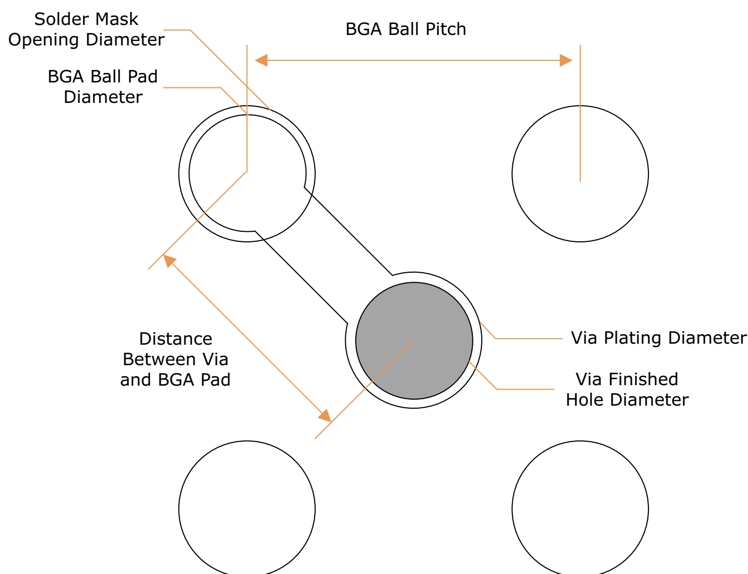



***Table 16 •*** **Recommended PCB Design Rules**

| Design Rule for Packages | 0.8 mm Pitch | 1.0 mm Pitch |
|---|---|---|
| | FCVG | FCG |
| BGA Ball Pad diameter | 0.4 mm | 0.51 mm |
| Solder mask opening diameter | 0.43 mm | 0.54 mm |
| BGA Ball pitch | 0.8 mm (31.5 mils) | 1.00 mm (39.37 mils) |
| Line width between via and solder land | 0.13 mm | 0.15 mm |
| Distance between via and solder land | 0.56 mm | 0.7 mm |
| Via Finished hole diameter | 0.33 mm | 0.33 mm |
| Via Plating diameter | 0.48 mm | 0.48 mm |

**Note:** For more information about package fanout, see *PolarFire SoC FPGA Package Fanout Application Note* (yet to be published).

## 1.16 Moisture Sensitive Level

The following table lists Microsemi PolarFire SoC packages Moisture Sensitive Levels (MSL). For information about solder re-flow guidelines for Sn/Pb and Pb-free, see *https://www.microsemi.com/company/quality/soldering-profiles*

***Table 17 •*** **Moisture Sensitive Levels**

| Package | MSL |
|---|---|
| FCG1152 | 4 |
| FCVG484 | 4 |

# 2 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the current publication.

## 2.1 Revision 1.0

The first publication of the document.