PolarFire® SoC FPGA Packaging and Pin Descriptions

Introduction

This guide provides pin and packaging information (such as bank assignments and mechanical information) for PolarFire SoC FPGAs.

PolarFire SoC FPGAs feature a flexible I/O structure that supports a range of mixed voltages (1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V) through bank selection. The HSIO and GPIO are configured as differential I/Os or two single-ended I/Os. For more information about HSIO, GPIO, and supported I/O standards, see UG0916: PolarFire SoC FPGA IO User Guide.

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1. Packaging Overview

PolarFire SoC FPGAs are available in multiple packages. Each package (device variant) has various I/O banks with the flexibility of using different I/O standards. HSIO and GPIO banks have a maximum supply voltage of 1.8 V and 3.3 V respectively.

The following table lists the PolarFire SoC FPGA variants, with user I/O and XCVR lanes, in Pb-free packages.

Table 1-1. Organization of I/O Banks

Bank Number	FCG1152	FCG1152	FCVG784	FCSG536	FCVG484	FCVG484	FCVG484
	MPFS460T	MPFS250T	MPFS250T	MPFS250T	MPFS250T	MPFS160T	MPFS095TS
Bank 0	HSIO	HSIO	HSIO	HSIO	HSIO	HSIO	HSIO
Bank 1	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO
Bank 2	MSSIO	MSSIO	MSSIO	MSSIO	MSSIO	MSSIO	MSSIO
Bank 3	JTAG/ FIXED I/O	JTAG/ FIXED I/O	JTAG/ FIXED I/O	JTAG/ FIXED I/O	JTAG/ FIXED I/O	JTAG/ FIXED I/O	JTAG/ FIXED I/O
Bank 4	MSSIO	MSSIO	MSSIO	MSSIO	MSSIO	MSSIO	MSSIO
Bank 5	MSS-SGMII	MSS-SGMII	MSS-SGMII	MSS-SGMII	MSS-SGMII	MSS-SGMII	MSS-SGMII
Bank 6	MSS-DDR	MSS-DDR	MSS-DDR	MSS-DDR	MSS-DDR	MSS-DDR	MSS-DDR
Bank 7	GPIO	GPIO	GPIO	GPIO	—	—	—
Bank 8	HSIO	HSIO	HSIO	—	—	—	—
Bank 9	GPIO	GPIO	GPIO	—	—	—	—
XCVR 0	Yes	Yes	Yes	Yes	Yes	Yes	Yes
XCVR 1	Yes	Yes	Yes	—	—	—	—
XCVR 2	Yes	Yes	—	—	—	—	—
XCVR 3	Yes	Yes	—	—	—	—	—
XCVR 4	Yes	—	—	—	—	—	—

1.1 Bank Locations

PolarFire SoC FPGA I/O are grouped based on I/O voltage standards and I/O capabilities. Each I/O bank has dedicated I/O supplies and ground voltages. Due to these dedicated supplies, only I/O with compatible standards are assigned to the same I/O voltage bank.

The following illustrations show the bank locations for the MPFS460T, MPFS250T, MPFS160T, and MPFS095T devices with available package combinations.

Figure 1-1. PolarFire SoC FPGA MPFS460T-FCG1152 I/O Bank Locations

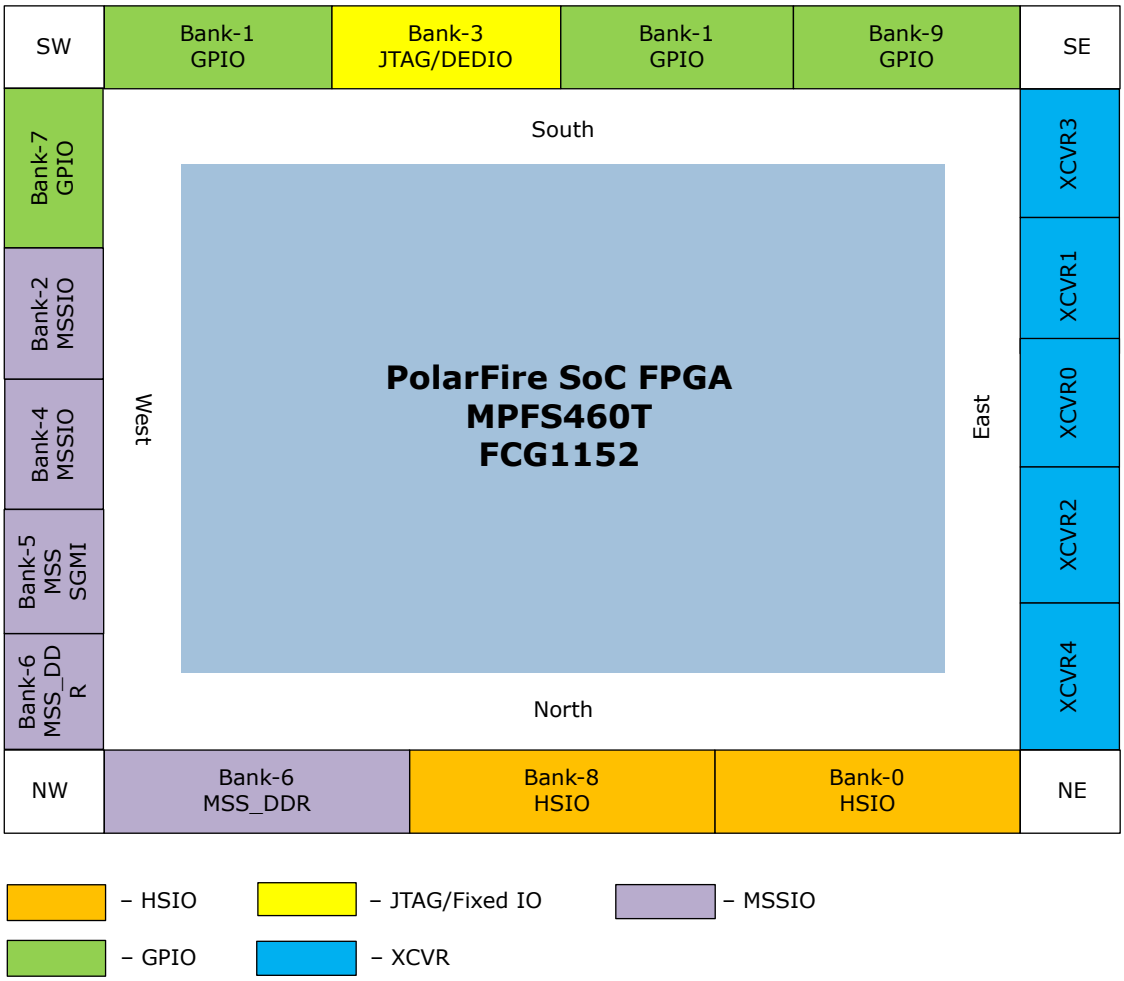


Figure 1-2. PolarFire SoC FPGA MPFS250T-FCG1152 I/O Bank Locations

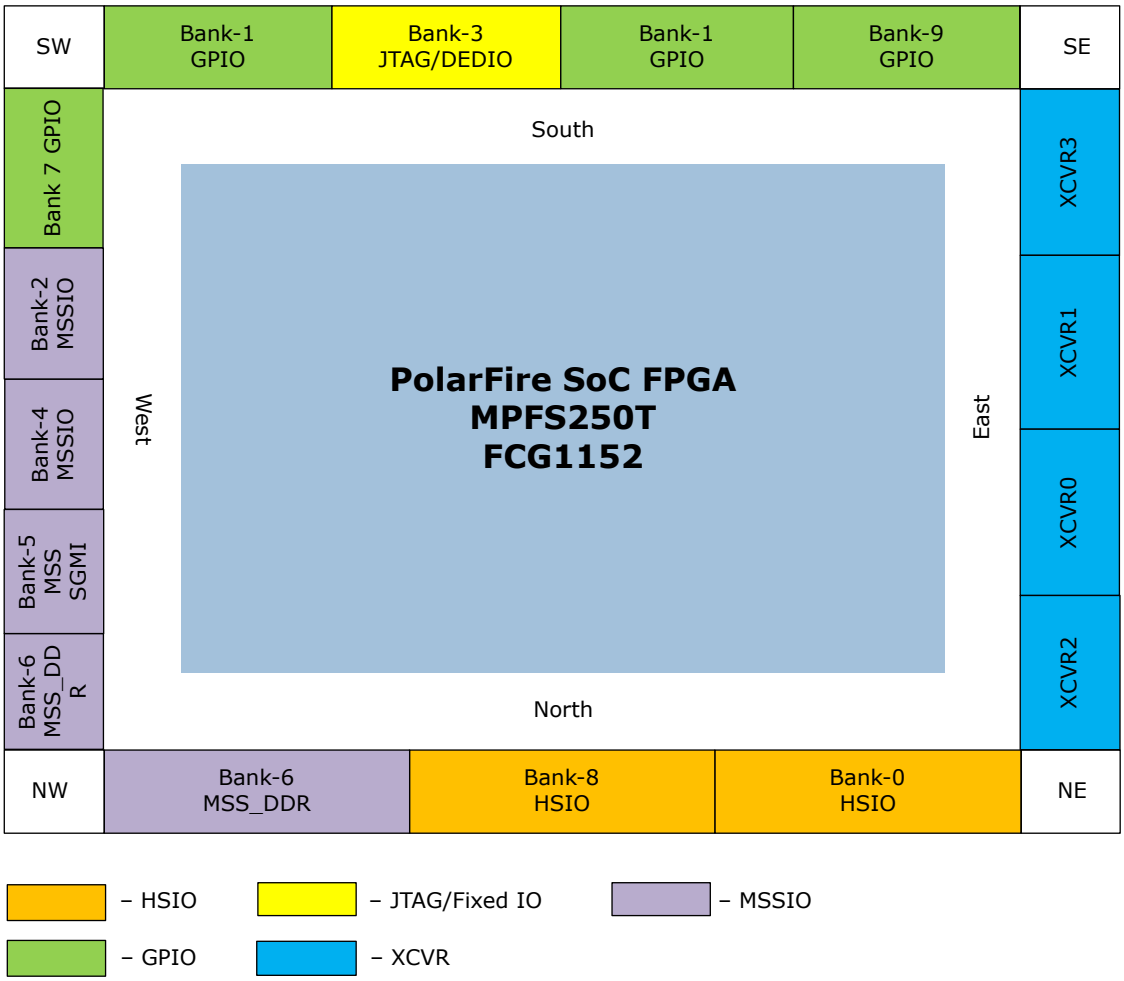


Figure 1-3. PolarFire SoC FPGA MPFS250T-FCVG784 I/O Bank Locations

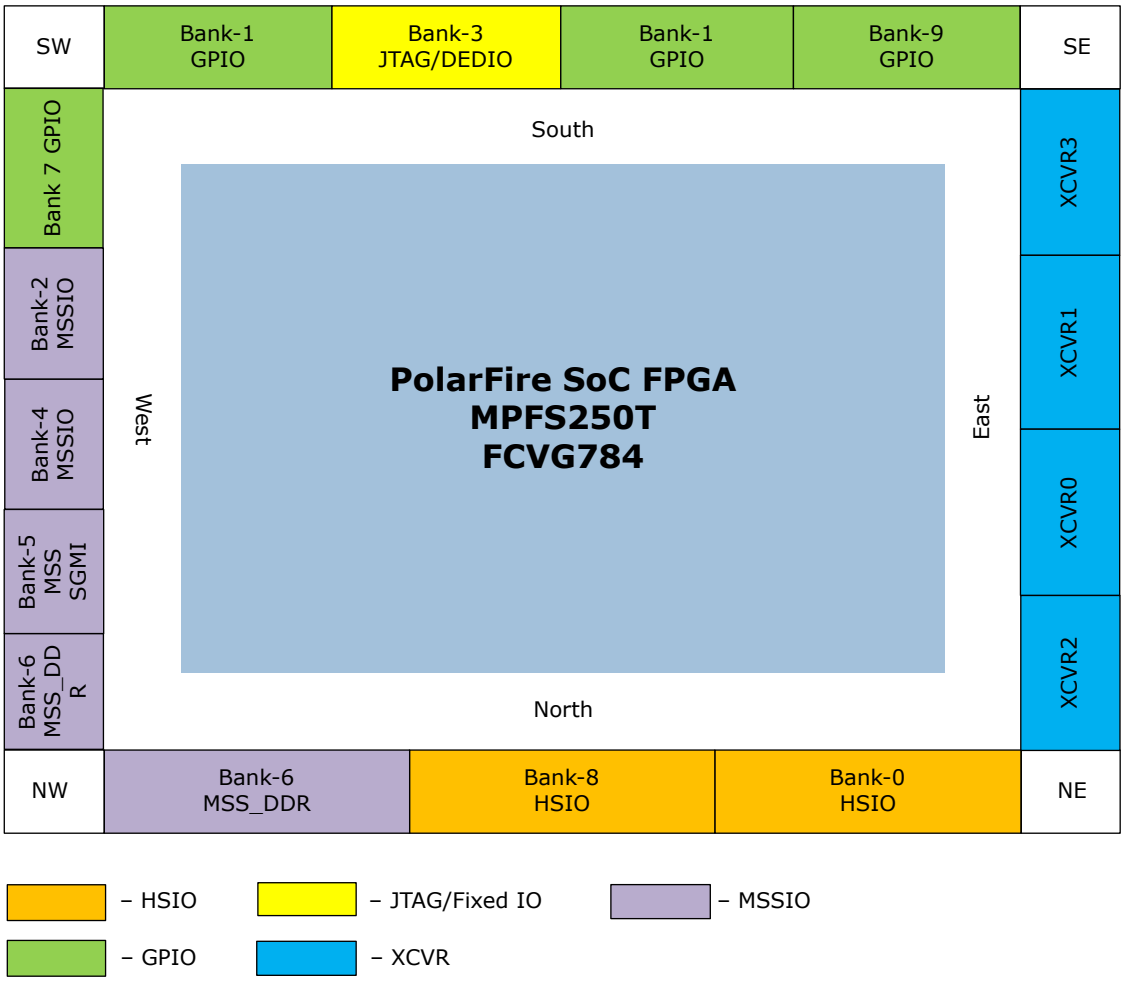
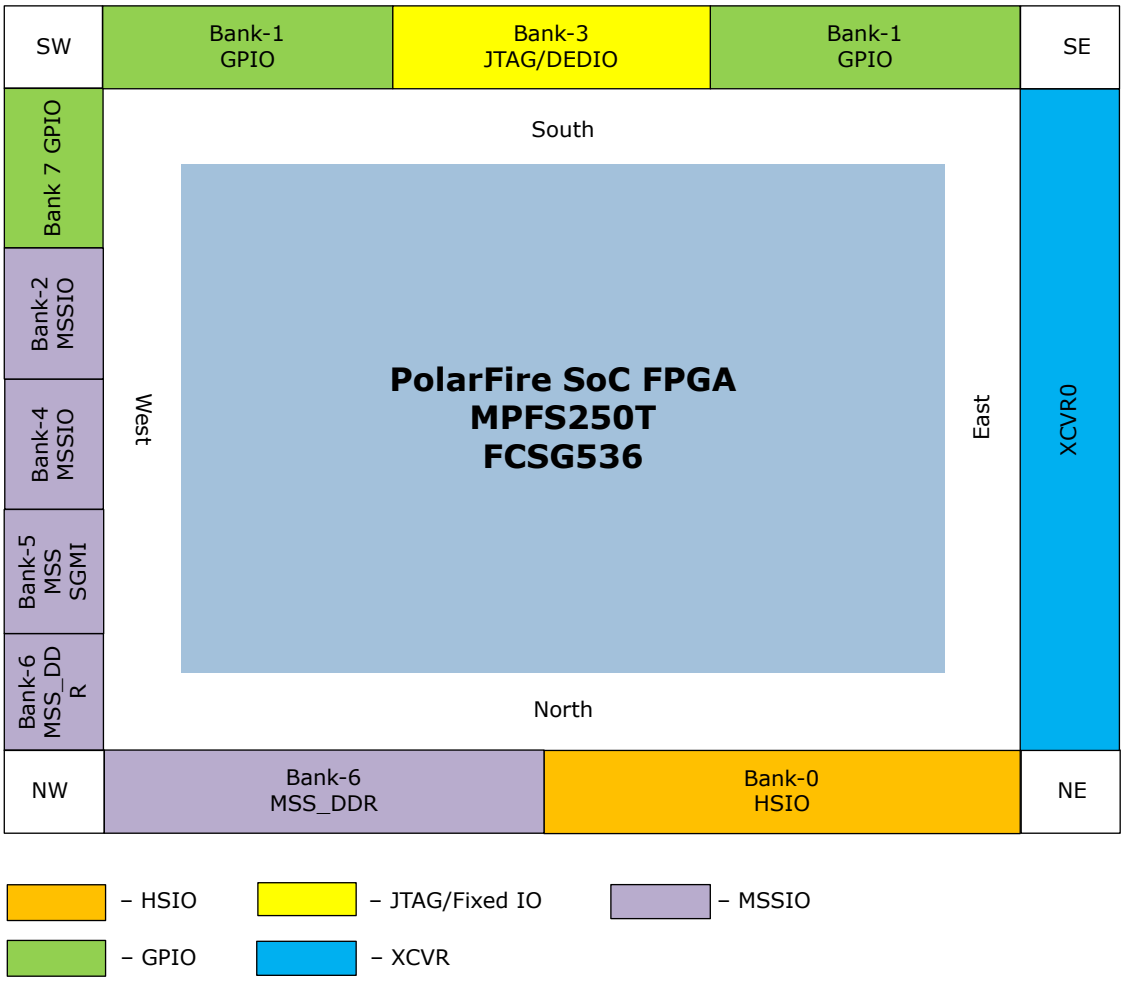
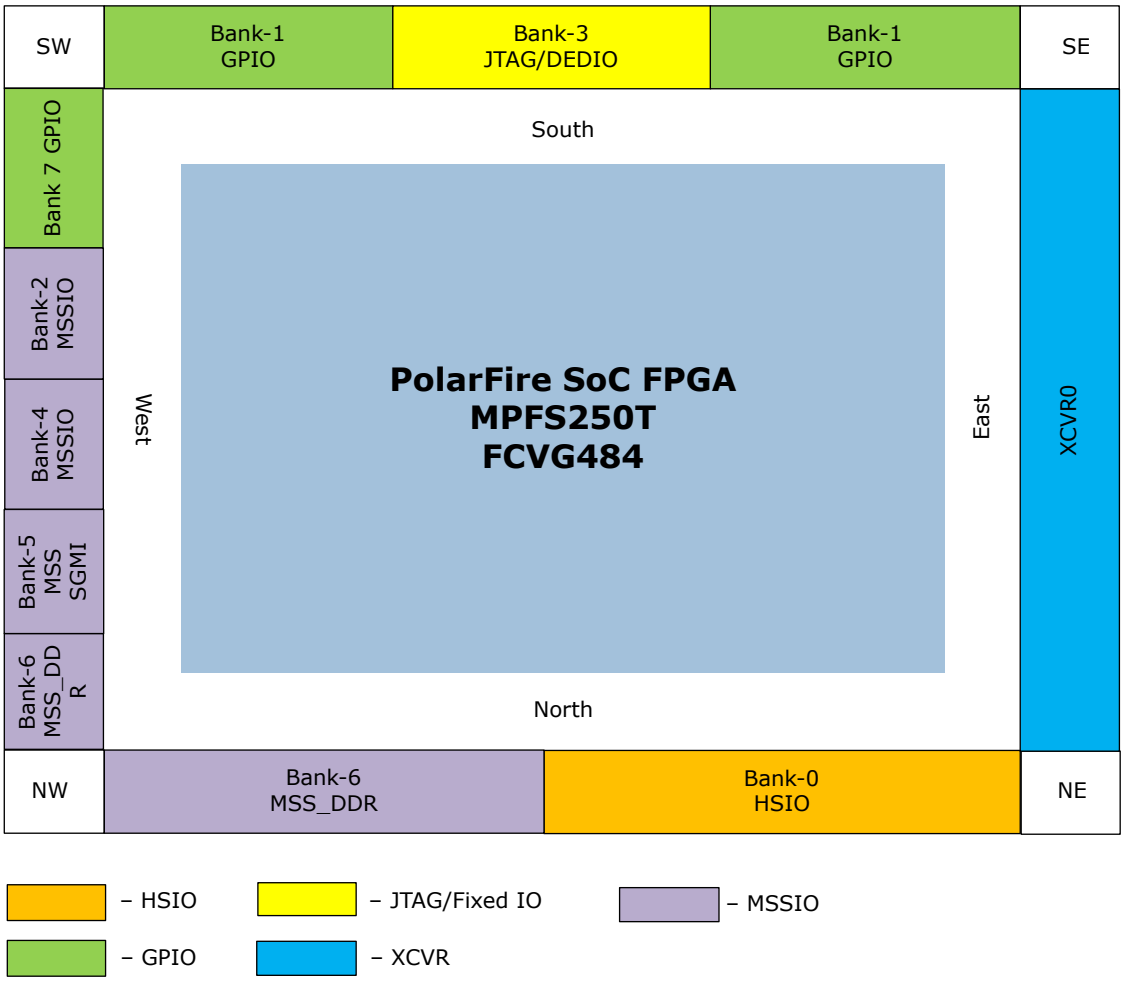


Figure 1-4. PolarFire SoC FPGA MPFS250T-FCSG536 I/O Bank Locations



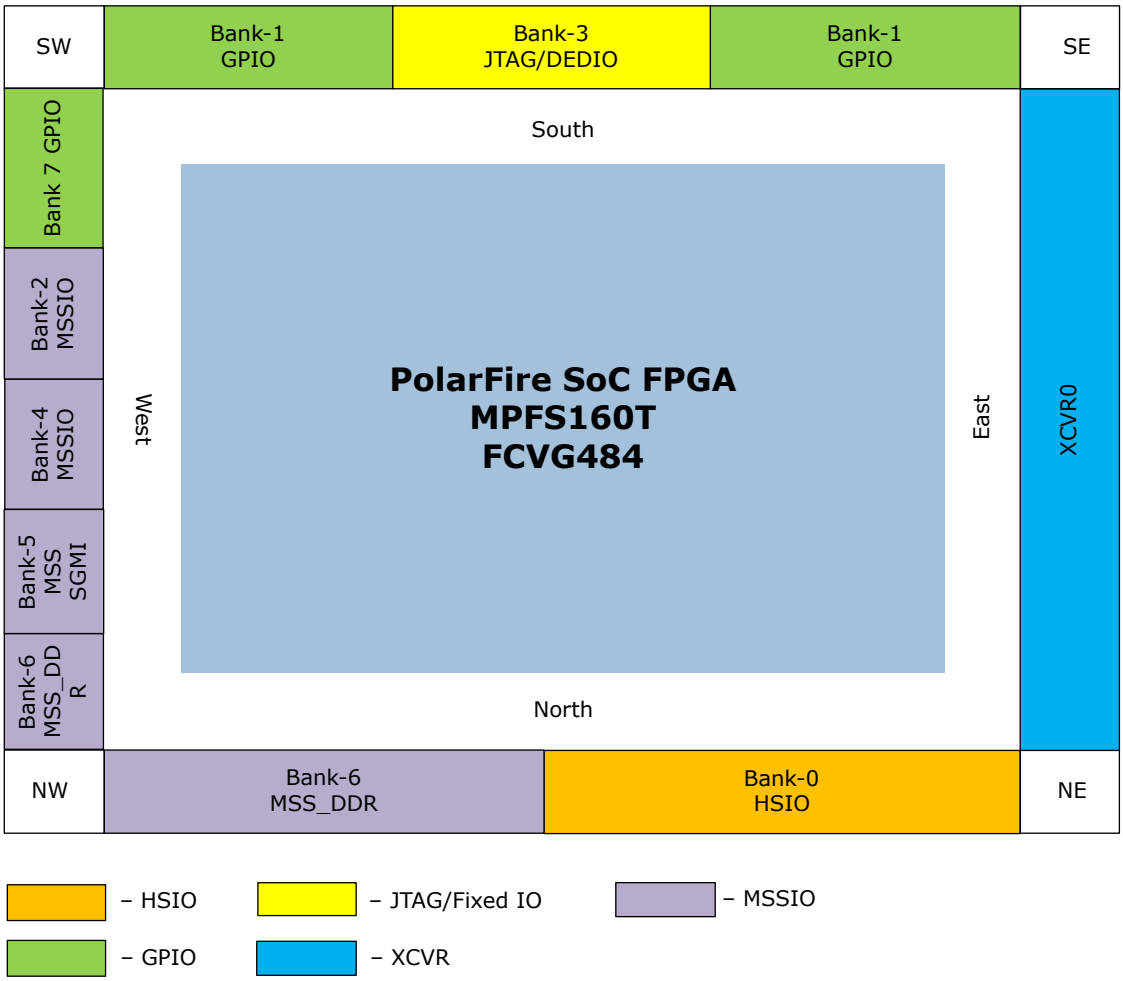
Note: Bank 9 VDDI and VDDAUX power pins are connected to Bank 1 VDDI and VDDAUX power pins, respectively within the package substrate for pin migration compatibility.

Figure 1-5. PolarFire SoC FPGA MPFS250T-FCVG484 I/O Bank Locations



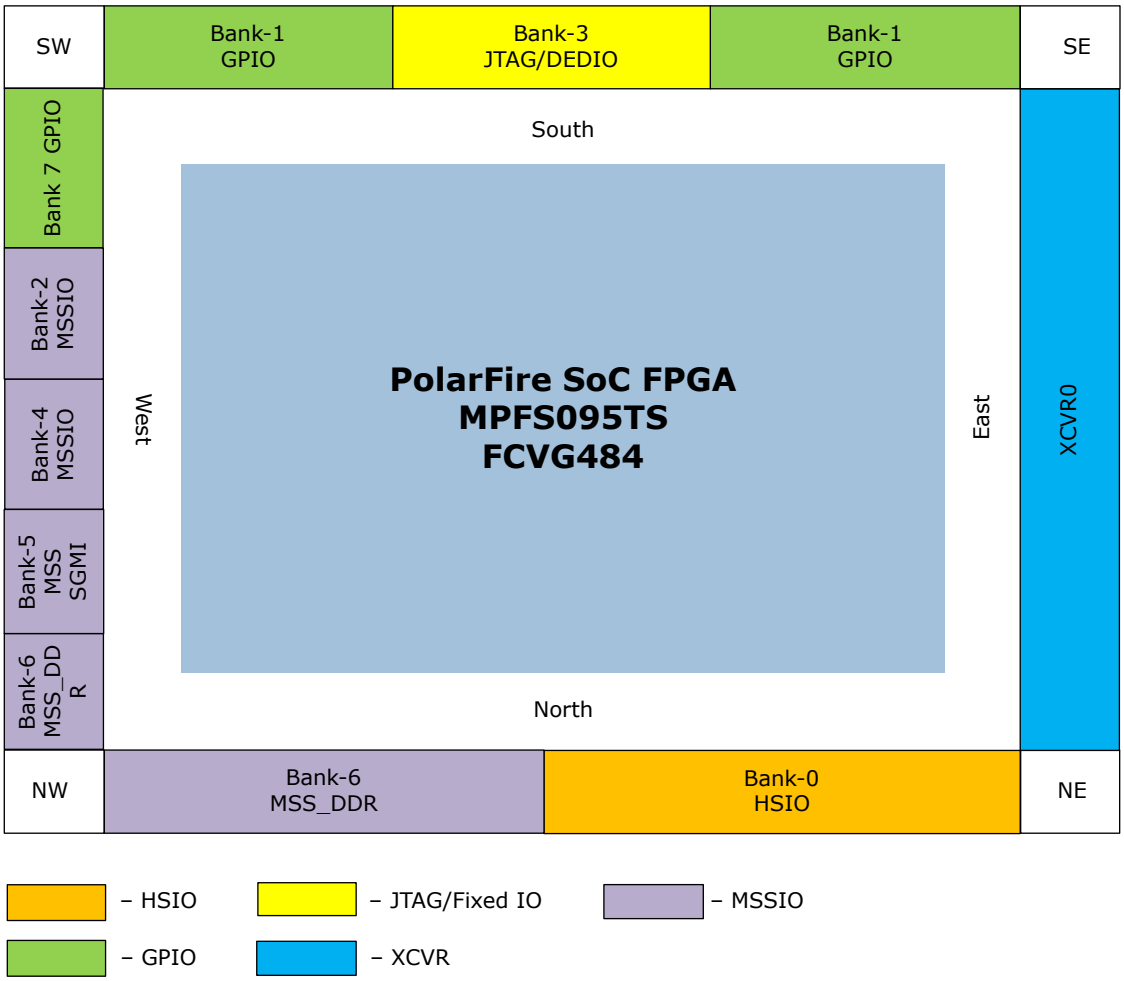
Note: Bank 9 VDDI and VDDAUX power pins are connected to Bank 1 VDDI and VDDAUX power pins, respectively within the package substrate for pin migration compatibility.

Figure 1-6. PolarFire SoC FPGA MPFS160T-FCVG484 I/O Bank Locations



Note: Bank 9 VDDI and VDDAUX power pins are connected to Bank 1 VDDI and VDDAUX power pins, respectively within the package substrate for pin migration compatibility.

Figure 1-7. PolarFire SoC FPGA MPFS095TS-FCVG484 I/O Bank Locations



Note: Bank 9 VDDI and VDDAUX power pins are connected to Bank 1 VDDI and VDDAUX power pins, respectively within the package substrate for pin migration compatibility.

1.2 Packaging Pin Assignment

PolarFire SoC Packaging Pin Assignment Table (PPAT) contains information about recommended DDR pinouts, PCIe capability for XCVR-0, DDR lane information for I/O CDR, and generic IOD interface pin placement.

1.3 Pin Descriptions

PolarFire SoC devices have user I/O (GPIO/HSIO) pins, dedicated I/O bank pins, memory interface, XCVR interface, clocking pins, and supply pins.

1.3.1 User I/O

PolarFire SoC FPGA I/Os are paired up to meet the differential I/O standards and grouped into lanes of 12 buffers with a lane controller for memory interfaces. For more information about the memory controller, see UG0906: PolarFire SoC FPGA DDR Memory Controller User Guide.

There are two types of I/O buffers—HSIO and GPIO. HSIO is optimized for 1.2 Gbps (DDR4) operation with operating supplies between 1.1 V and 1.8 V. GPIO buffers support a wider range of I/O interfaces with speeds of up to 1066 Mbps when using single-ended standards and 1.25 Gbps when using differential standards, and operating

supplies ranging from 1.2 V to 3.3 V. GPIO supports multiple standards, including 3.3 V with an integrated Clock Data Recovery (CDR) to high-speed serial interfaces such as 1GbE.

Each PolarFire SoC FPGA user I/O uses a IOxyBz naming convention, where:

- IO = The type of I/O.
- x = The I/O pair number in Bank z.
- y = P (positive) or N (negative). In Single-Ended mode, the I/O pair operates as two separate I/O—P and N. Differential mode is implemented with a fixed I/O pair and cannot be split with an adjacent I/O.
- B = Bank (see note in 1.3.1.1 Supported I/O Features.
- z = Bank number.
  GPIOxyBz and HSIOxyBz are bi-directional user I/O pins that are capable of differential signaling.

1.3.1.1 Supported I/O Features

The following table lists the I/O features supported on HSIO and GPIO.

Table 1-2. Supported I/O Features

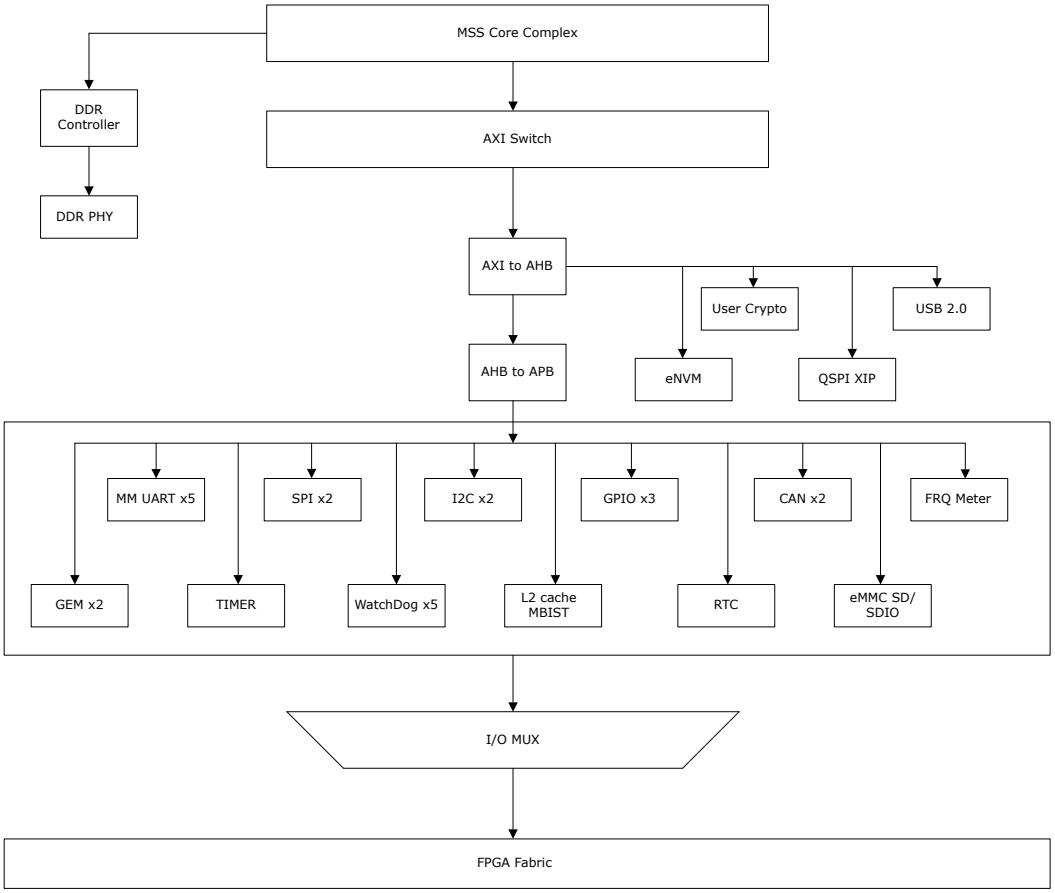
I/O Feature	HSIO	GPIO	Additional Information
Programmable on/off clamp	—	Yes	—
Hot-plug	—	Yes	—
Cold sparing	Yes[1]	Yes	—
True differential output driver	—	Yes	—
Programmable on/off 100 Ω differential termination	—	Yes	—
PVT-compensated output drive	Yes	Yes	—
Programmable slew control	—	Yes	—
PVT compensated slew control	Yes	—	—
Programmable input hysteresis	Yes	Yes	—
Mobile Industry Processor Interface (MIPI) (input)	—	Yes	High-speed and low-power
MIPI (output)	—	Yes	High-speed

Note: 1. HSIO is pseudo-cold spare that is, it requires the spare device to have its HSIO VDDI banks powered-up to prevent I/O leakage through the ESD diodes.

1.3.2 MSS I/Os

The PolarFire SoC family offers the industry's first RISC-V based SoC FPGAs. The PolarFire SoC family combines a powerful 64-bit 5x core RISC-V Microprocessor Sub-System (MSS) with the FPGA fabric in a single device. Packed with this powerful combination, PolarFire SoC devices offer the scalable features of FPGAs and high-performance of ASICs. Only the FPGA fabric resources vary but the MSS remains the same across PolarFire SoC device variants, making these devices ideal for many applications.

Figure 1-8. MSS I/O Block Diagram



There are 38 MSS I/Os that can be configured using the Libero® SoC software to interface with various peripherals. See PolarFire SoC Packaging Pin Assignment Table for the pinout information of the MSS pins. The pinout provides multiple options on where the MSS peripherals can be connected. The following interfaces are configured using the software.

- CAN Controller (x2)
- I2C (x2)
- MMUART (x5)
- SPI (x2)
- Quad SPI with XIP
- Gigabit Ethernet MAC (GEM x2)
- eMMC SD/SDIO
- Universal Serial Bus OTG Controller (USB)
- DDR Controller
- GPIO

1.3.3 Supply Pins

The following table lists multiple power supply pins required for proper device operation. For more information about unused conditions and power sequence, see UG0901: PolarFire SoC FPGA Board Design Guidelines User Guide.

Table 1-3. Supply Pins

Name	Description	Operating Voltage
XCVR_VREF	Voltage reference for transceiver	0.9 V/1.25 V
VDD_XCVR_CLK	Power for transceiver reference clock input buffers	2.5 V/3.3 V
VDDA25	Transceiver PLL power	2.5 V
VDDA	Power for transceiver Tx and Rx lanes 0, 1, 2, and 3	1.0 V/1.05 V
VSS	Core digital ground	NA
VDD	Device core digital supply	1.0 V/1.05 V
VDDIx (JTAG Bank)	Supply for I/O circuits in a bank	1.8 V/2.5 V/3.3 V
VDDIx (GPIO Banks)	Supply for I/O circuits in a bank	1.2 V/1.5 V/1.8 V/2.5 V/3.3 V
VDDIx (MSSIO Banks)	Supply for MSS I/O circuits in a bank	1.2 V/1.5 V/1.8 V/2.5 V/3.3 V
VDDIx (MSS SGMII Banks)	Supply for MSS SGMII circuits in a bank	2.5 V/3.3 V
VDDIx (MSS DDR Bank)	Supply for MSS DDR circuits in a bank	1.2 V/1.5 V/1.8 V
VDDIx (HSIO Banks)	Supply for HSIO I/O circuits in a bank	1.2 V/1.5 V/1.8 V

1.3.3.1 Packaging Decoupling Capacitors

PolarFire SoC 0.8 mm and 1.0 mm pitch packages contain decoupling capacitors to support high-speed I/O operation.

Small, low-profile CSP packages (0.5 mm ball pitch, 16 mm × 16 mm, and smaller) do not have package decoupling capacitors.

The following table lists the packaging decoupling capacitors contained in non-CSP packages.

Table 1-4. Decoupling Capacitor per Die-Package

Supply Name	Bank No./IO Type	Capacitor Rating	FC1152, 35 x 35 mm, 1.0 mm		FC784, 23 x 23 mm, 0.8 mm			FCV484, 19 x 19 mm, 0.8 mm			
			MPFS 450T	MPFS 250T	MPFS 250T	MPFS 150T	MPFS 095T	MPF 250T	MPF S150 T	MPF S095 T	MPF S025 T
VDDA	SERDES Power	4.7 nF	1	1	1	1	1	1	1	1	1
VDDA	SERDES Power	2.2 nF	1	1	1	1	1	—	—	—	—
VDDA	SERDES Power	1.5 nF	1	1	1	1	1	—	—	—	—
VDDA	SERDES Power	1.0 nF	1	1	1	1	1	1	1	1	1
VDDI0	Bank 0/HSIO Bank Power	1.0 µF	1	1	1	1	1	—	—	—	—
VDDI8	Bank 8/HSIO Bank Power	1.0 µF	1	1	1	1	1	—	—	—	—
VDDI6	Bank 6/HSIO - DDR Bank Power	1.0 µF	1	1	1	1	1	—	—	—	—
VDD18	HSIO/MSS_DDR Input Power	1.0 µF	1	1	1	1	1	—	—	—	—
VDDI1	Bank 1/GPIO Bank Power	1.0 µF	1	1	1	1	1	—	—	—	—

.....continued											
Supply Name	Bank No./IO Type	Capacitor Rating	FC1152, 35 x 35 mm, 1.0 mm		FC784, 23 x 23 mm, 0.8 mm			FCV484, 19 x 19 mm, 0.8 mm			
			MPFS 450T	MPFS 250T	MPFS 250T	MPFS 150T	MPFS 095T	MPF 250T	MPF S150 T	MPF S095 T	MPF S025 T
VDDI9	Bank 9/GPIO Bank Power	1.0 µF	1	1	1	1	1	—	—	—	—
VDDI7	Bank 7/GPIO Bank Power	1.0 µF	1	1	1	1	1	—	—	—	—
VDDI2	Bank 2/MSSIO Bank Power	—	—	—	—	—	—	—	—	—	—
VDDI4	Bank 4/MSSIO Bank Power	—	—	—	—	—	—	—	—	—	—
VDDI5	Bank-5/MSS SGMII Bank Power, Pre-Driver	—	—	—	—	—	—	—	—	—	—
VDD25	PGM, PLL Power	1.0 µF	1	1	1	1	1	—	—	—	—
VDD	Core Power	2.2 µF	1	1	1	1	1	—	—	—	—
Total Number of Capacitors			13	13	13	13	13	2	2	2	2

Note: FCSG536 and FCSG325 do not have package capacitors.

1.3.4 Memory Interface

Valid locations for DDR memory interfaces are shown in PolarFire SoC Packaging Pin Assignment Table. By using Libero SoC, all individual DDR interface pins are identified from the DDR macro. For more information about the memory interface, see UG0906: PolarFire SoC FPGA DDR Memory Controller User Guide.

1.3.5 DDR Interface

The DDR subsystems are hardened ASIC blocks for interfacing the LPDDR3, LPDDR4, DDR3, and DDR4 memories. It supports 16-bit, 32-bit, and 64-bit data bus width modes with ECC support. The DDRIO uses fixed impedance calibration for different drive strengths. These values are programmed using Libero SoC software for the selected I/O standard. The values are fed to the pull-up or pull-down reference network to match the impedance with an external resistor. For more information about DDR signals, see UG0906: PolarFire SoC FPGA DDR Memory Controller User Guide.

1.3.6 Clocking Pins

CCC blocks, located at each corner of the PolarFire SoC FPGAs, contain two PLLs and two DLLs that provide flexible on-chip and off-chip clock management and synthesis capabilities. CCCs are labeled according to their locations in the core. For example, the CCC located in the northeast corner is labeled as CCC_NE. For more information about clocking pins, see UG0913: PolarFire SoC FPGA Clocking Resources User Guide.

Preferred clock inputs (CLKIN) are located on three sides of the device, with eight preferred clock inputs on the west side, twelve on the north side, and either 12 or 16 inputs on the south side, depending on the package. For more information about clocking pin names, descriptions, and operating voltages, see Table 1-3

1.3.7 Dedicated I/O Bank Pins

JTAG, SPI, and DEVRST_N signals share the same Bank 3 supply and are not directly available to the fabric. SPI IOs are, however, dynamically switched over to be used by the fabric whenever the PolarFire SoC controller is not using them. Dedicated I/O bank supplies must be powered up higher than their operational threshold and enabled before the PolarFire SoC controller negates the main power-on reset to the fabric. Table 1-5, Table 1-6, and Table 1-7

list the JTAG, SPI, and DEVRST_N pin names and descriptions. Libero configures unused user I/O as input buffer disabled, and output buffer tri-stated with weak pull-up.

For more information about unused conditions and power sequence, see UG0901: PolarFire SoC FPGA Board Design Guidelines User Guide.

The JTAG bank voltages can be set to operate at 1.8 V, 2.5 V, or 3.3 V. The following table lists the JTAG pins.

Table 1-5. JTAG Pins

Pin Names	Direction	Weak Pull-Up/Unused Condition	Description
TMS	Input	Yes/DNC	JTAG test mode select
TRSTB	Input	Yes[1]	JTAG test reset. Must be held low during device operation
TDI	Input	Yes/DNC	JTAG test data in In ATPG or Test mode, when using a 4-bit TDI bus, this I/O is used as TDI[0]
TCK	Input	No[2]	JTAG test clock
TDO	Output	No/DNC	JTAG test data out

Note: 1. If TRSTB is unused and in the Avionics mode, either an external 1 kW pull-down resistor should be connected to it, to override the weak internal pull-up or it should be driven low from the external source.

Note: 2. In unused condition, must be connected to VSS through 10 kW resistor.

Table 1-6. Device Reset Pins

Name	Direction	Weak Pull-up	Description
DEVRST_N	Input	22 kΩ	Device reset (asserted low)

Table 1-7. SPI Interface Pins

Name	Direction	Description
SCK	Bi-directional	SPI clock
SS	Bi-directional	SPI slave select
SDI	Input	SDI input for the shared SPI interface
SDO	Output	SDO output for the shared SPI interface
SPI_EN	Input	Pulled up or down through a resistor or driven dynamically from an external source to enable or tri-state the SPI I/O
IO_CFG_INTF	Input	Pulled up or down through a resistor or driven dynamically from an external source to indicate whether the shared SPI interface is a master or a slave. Dedicated to the system controller. 0: SPI slave interface 1: SPI master interface

Table 1-8. Special Pins

Name	Direction	Description
NC	—	No connect pin. This pin indicates that it is not connected within the circuitry. NC pins can be driven by any voltage or can be left floating with no effect on the operation of the device.

.....continued		
Name	**Direction**	**Description**
DNC	—	Do not connect pin. DNC pins must not be connected to any signal on the PCB, and they must be left unconnected.
LPRB_A	Output	Specifies an internal signal for probing (oscilloscope-like feature). The two live probe I/O cells function as either of the following: – Live probe – User I/O (HSIO)
LPRB_B	Output	
FF_EXIT_N	Input	Reserved
Shield Signal	Output	Shield signal is required for each DDR data byte signal. It must be driven with maximum drive strength to improve the signal integrity.

1.3.8 XCVR Interface

The transceiver I/O available in the PolarFire SoC devices are dedicated for high-speed serial communication protocols. Libero defined DNC pins are pulled up internally when not used in the Libero design.

For more information about unused conditions and power sequence, see UG0901: PolarFire SoC FPGA Board Design Guidelines User Guide.

The following table lists the XCVR Interface pins and descriptions.

Table 1-9. XCVR Interface Pins

Name	Direction	Description
XCVR_xy_REFCLK_P	Input	Differential serial reference clock. xy - location x - transceiver number (0, 1, 2, 3) y - lane number (0, 1, 2, 3)
XCVR_xy_REFCLK_N		
XCVR_x_TXy_P	Output	Differential serial transmit pins. x - transceiver number (0, 1, 2, 3) y - lane number (0, 1, 2, 3)
XCVR_x_TXy_N		
XCVR_x_RXy_P	Input	Differential serial receive pins. x - transceiver number (0, 1, 2, 3) y - lane number (0, 1, 2, 3)
XCVR_x_RXy_N		

1.4 Package Pinouts

For more information about the pinout, see PolarFire SoC Packaging Pin Assignment Table.

1.5 Mechanical Drawings

The following illustrations show the top, bottom, and side views, and dimensions for the PolarFire SoC FPGAs.

Figure 1-9. MPFS460T/MPFS250T-FCG1152 Package Top-View and Side-View

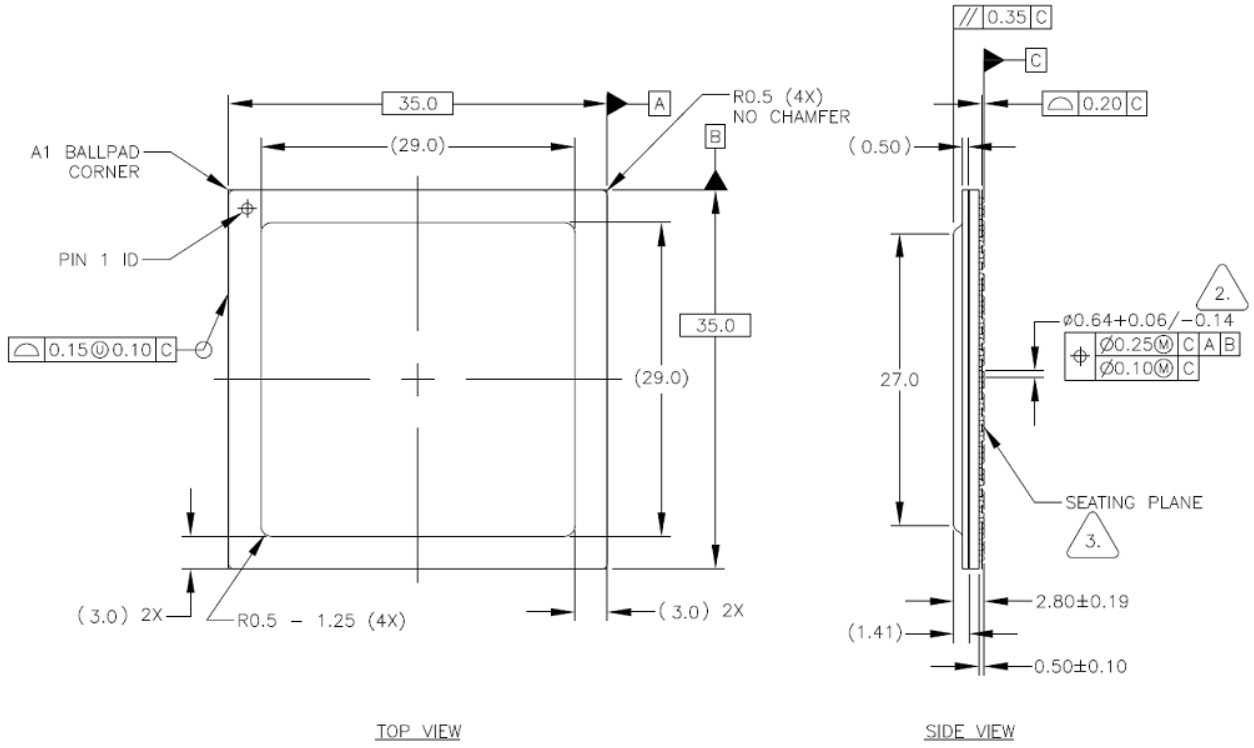


Figure 1-10. MPFS460T/MPFS250T-FCG1152 Package Bottom-View

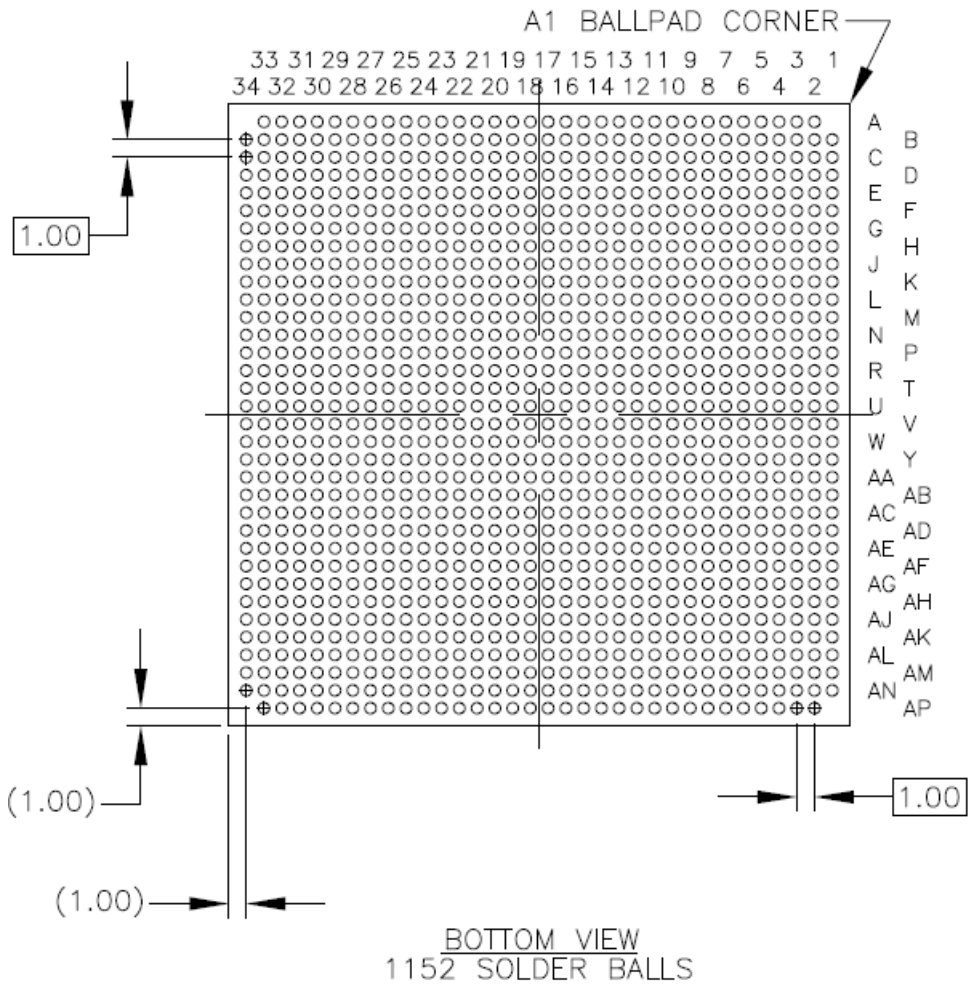


Figure 1-11. MPFS250T-MPFS160T-MPFS095T-FCVG784 Package Top-View and Side-View

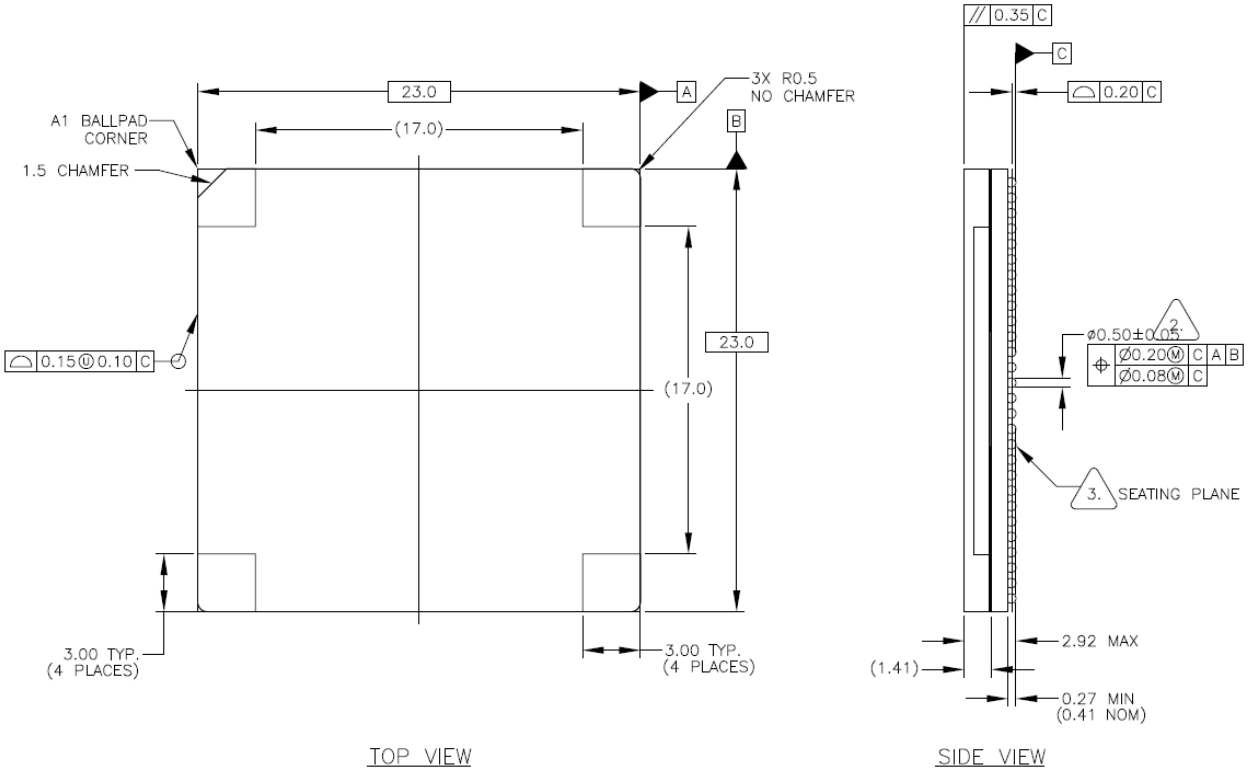


Figure 1-12. MPFS250T-MPFS160T-MPFS095T-FCVG784 Package Bottom-View

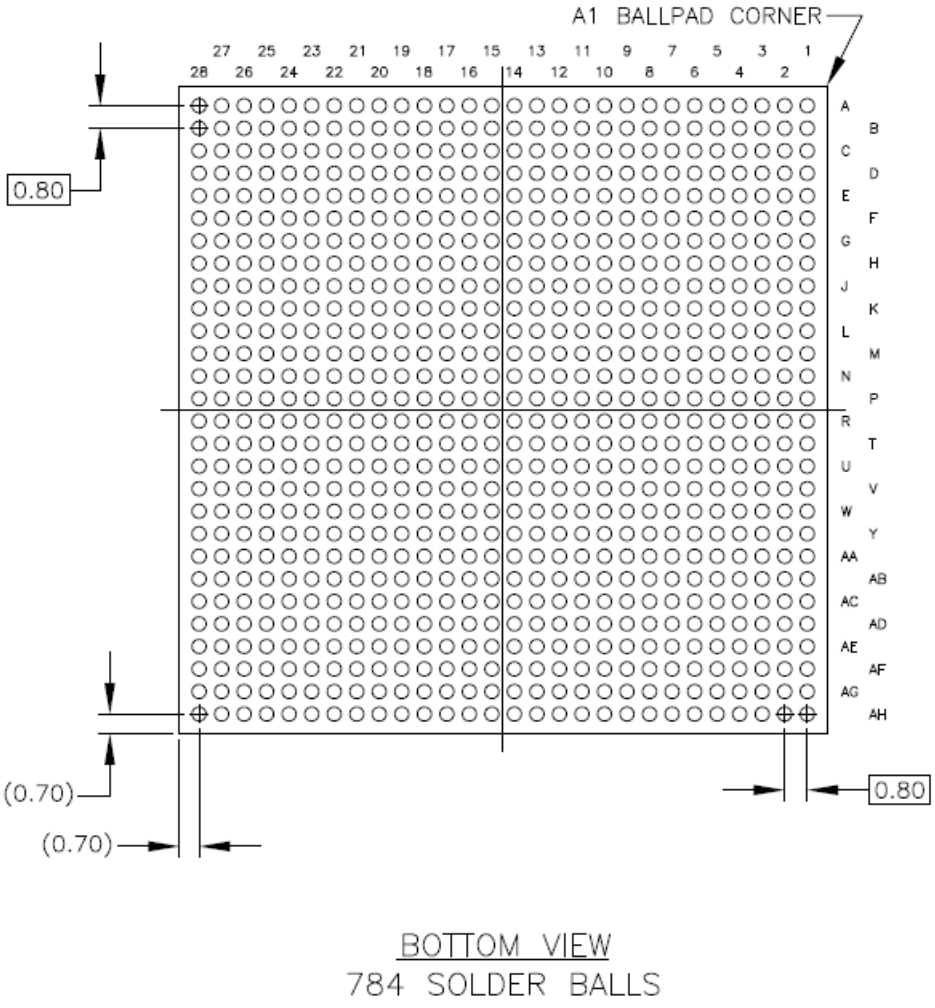


Figure 1-13. MPFS250T/MPFS160T/MPFS095T/MPFS025T - FCVG484 Package Top-View and Side-View

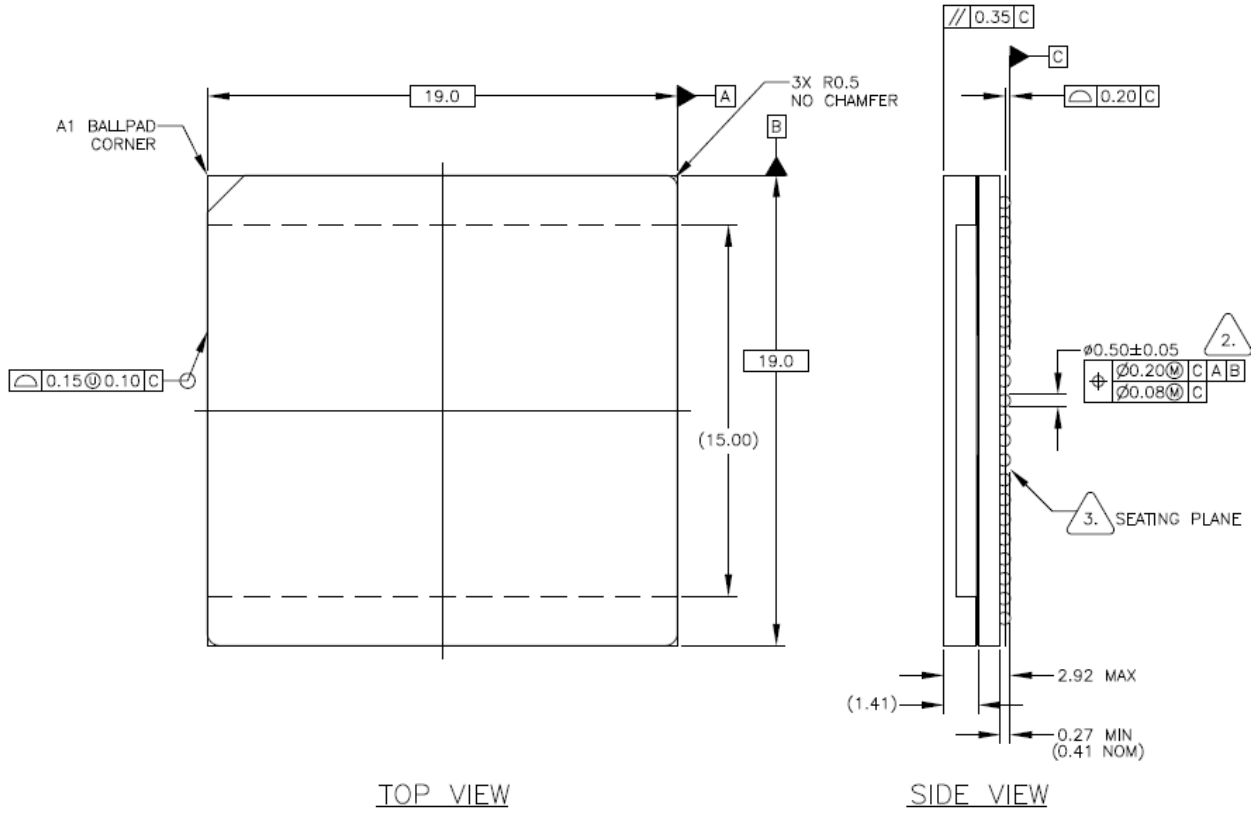
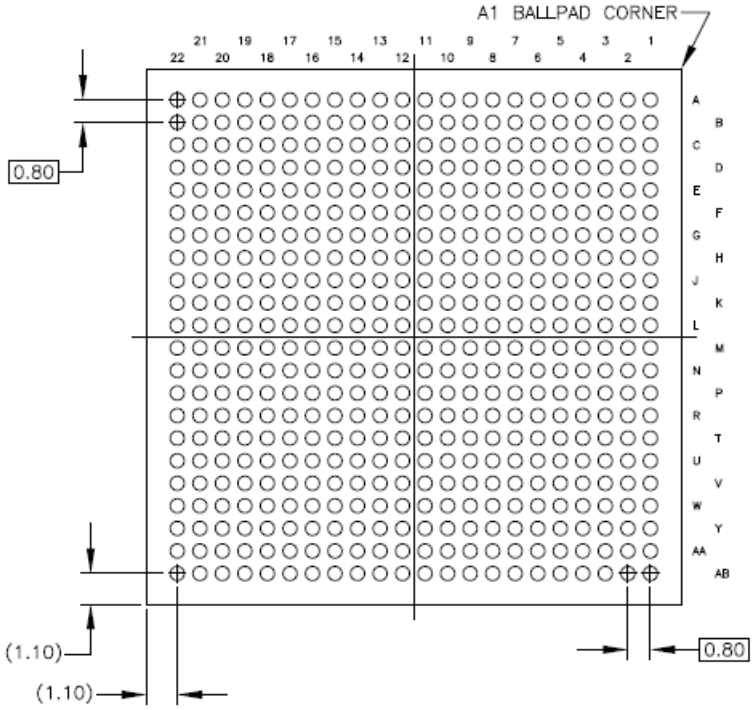


Figure 1-14. MPFS250T/MPFS160T/MPFS095T/MPFS025T - FCVG484 Package Bottom-View



BOTTOM VIEW
484 SOLDER BALLS

Figure 1-15. MPFS250T/MPFS160T/MPFS095T-FCSG536 Package Top-View and Side-View

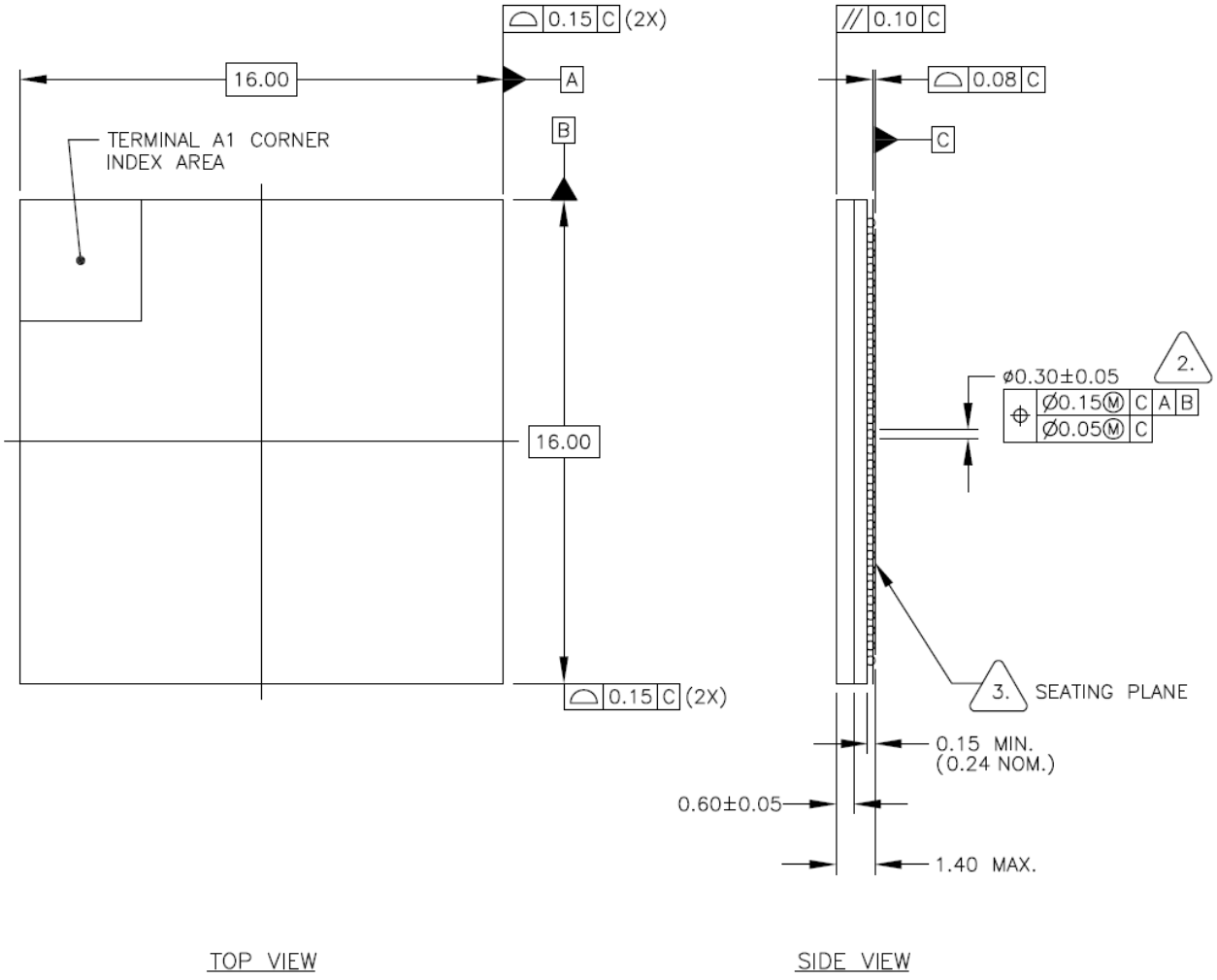
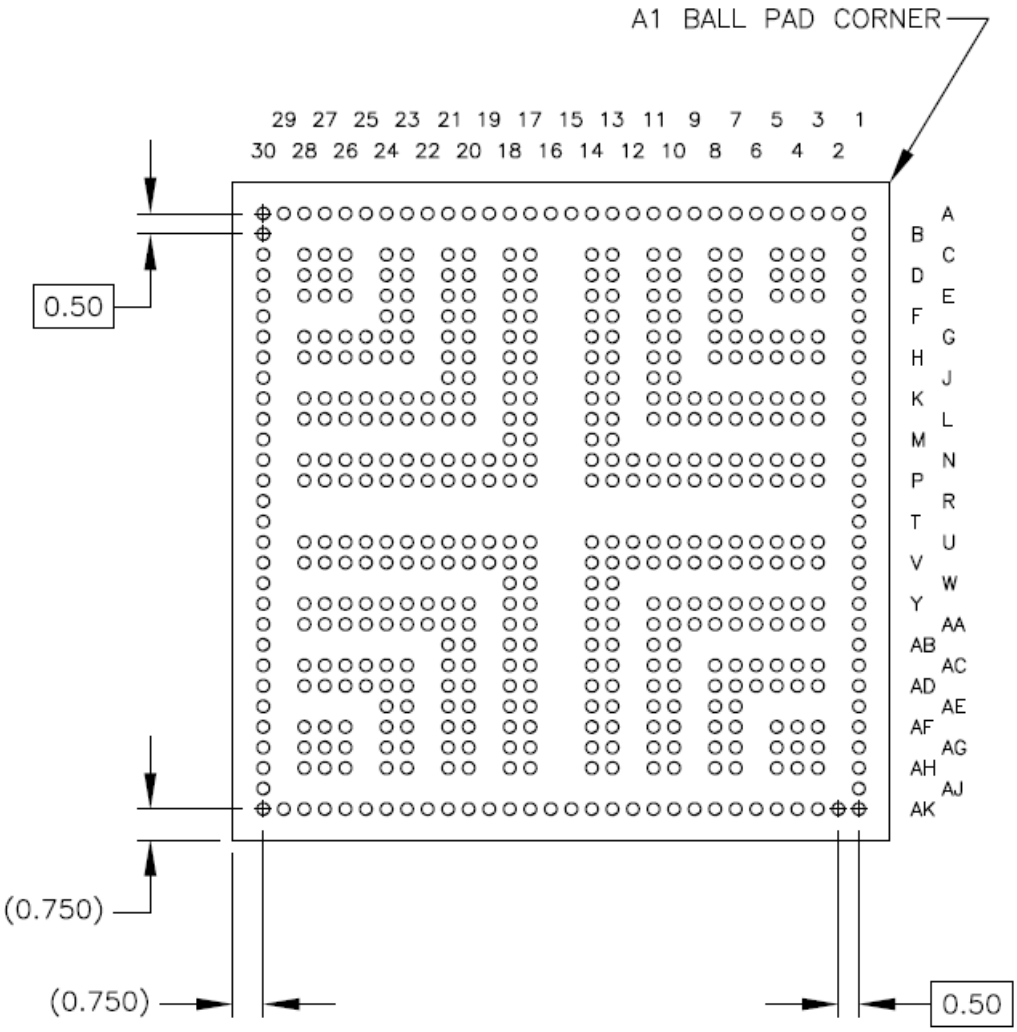


Figure 1-16. MPFS250T/MPFS160T/MPFS095T-FCSG536 Package Bottom-View



BOTTOM VIEW
536 SOLDER BALLS

The following table lists the PolarFire SoC FPGAs Package description and specification.

Table 1-10. PolarFire SoC FPGAs Package Information

Package	Description	Package Specifications			
		Package type	Pitch (mm)	Size (mm)	Maximum I/Os
MPFS460T-FCG1152	Flip-chip with lid	BGA	—	35 × 35	—
MPFS250T-FCG1152	Flip-chip with lid	BGA	1	35 × 35	512
MPFS250T-FCVG784	Flip-chip with lid	BGA	0.8	23 x 23	—
MPFS160T-FCVG784	Flip-chip with lid	BGA	0.8	23 x 23	—
MPFS095T-FCVG784	Flip-chip with lid	BGA	0.8	23 x 23	—

.....continued

Package	Description	Package Specifications			
		Package type	Pitch (mm)	Size (mm)	Maximum I/Os
MPFS250T-FCVG484	Flip-chip with lid	BGA	0.8	19 × 19	284
MPFS160T-FCVG484	Flip-chip with lid	BGA	0.8	19 × 19	—
MPFS095T-FCVG484	Flip-chip with lid	BGA	0.8	19 x 19	280
MPFS250T-FCSG536	—	BGA	0.5	16 x 16	304
MPFS160T-FCSG536	—	BGA	—	16 x 16	—
MPFS095T-FCSG536	—	BGA	—	16 x 16	—

2. Package Material Information

The following table lists the PolarFire SoC ball grid array RoHS packages.

Table 2-1. PolarFire SoC Ball Grid Array RoHS Packages

Package Balls	FCG1152	FCVG784	FCVG484	FCSG536
Package Pitch	1 mm	1 mm	0.8 mm	1 mm
Substrate Material	Epoxy Glass	Epoxy Glass	Epoxy Glass	Epoxy Glass
Solder Ball Composition RoHS	SAC305	SAC305	SAC305	SAC305
Solder Bump Material	Sn98.2/Ag1.8	Sn98.2/Ag1.8	Sn98.2/Ag1.8	Copper + SnAg

Note: For all flip-chip BGA packages—Only FCG1152 and FCSG536 are not vented. FCVG784 and FCVG484 are vented.

3. Thermal Specifications

To be updated.

4. Package Marking

To be updated.

5. Packing and Shipping

The PolarFire SoC series devices are packed in trays, which are used to pack most of the Microchip surface-mount devices. Trays provide excellent protection from mechanical damage. In addition, they are manufactured using the anti-static material to provide limited protection against ESD damage.

Table 5-1. Standard Device Counts per Tray and Carton

Package	Maximum Number of Devices per Tray	Maximum Number of Trays per Stack	Maximum Number of Units per Inner Carton
FCG1152	TBD	TBD	TBD
FCVG784	TBD	TBD	TBD
FCVG484	TBD	TBD	TBD
FCSG536	TBD	TBD	TBD

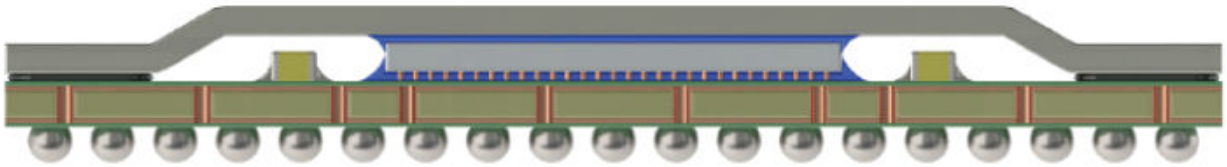
6. Thermal Management

Microchip PolarFire SoC FPGAs are offered in lidded flip-chip BGA (FCBGA) format. Lidded FCBGA features a controlled bond-line thermal interface material (TIM) thickness that reduces the thermal resistance (Theta-JC) between the junction and the externally applied thermal solution. The lid or heat spreader also spreads the heat away from the die to the package perimeter and to the printed circuit board.

Optimized package electrical performance with multiple power and ground planes to take care of signal return paths, and dense core via under the die to improve power delivery adds benefit in dissipating heat through the bottom of the package and to the board.

PolarFire SoC FPGAs in FCVG484 are also available in bare-die FCBGA. Bare-die flip-chip BGA produces the lowest possible thermal resistance (Theta-JC) between the junction and any externally applied thermal solution.

Figure 6-1. Heat Spreader with Thermal Interface Material



6.1 System Level Heat Sink Solutions

The use of external heat sinks, component placement in the PCB, and air flow in the system depends on the physical and mechanical limitations of the system. A system level thermal design engineer must understand these limitations and device capabilities to effectively manage the complete thermal strategy.

7. Thermal Interface Material

When using external heat sinks, a suitable thermal interface material must be considered to effectively transfer the heat from the component to the heat sink, and eventually to the environment.

For bare-die flip-chip BGAs, the surface of the silicon contacts the heat sink. For lidded flip-chip BGAs, the lid contacts the heat sink. The surface size of the bare-die flip-chip BGAs and lidded flip-chip BGAs are different. Microchip recommends a different type of thermal material for long-term use with each type of flip-chip BGA's package.

For lidded flip-chip BGAs, the lid contacts the external heat sink while bare-die flip-chip BGAs, the surface of the silicon contacts the external heat sink. The surface areas of lidded flip-chip BGAs and bare-die flip-chip BGAs are different. The system level thermal design engineer must choose the appropriate TIM to be used.

Thermal interface material is required because the surfaces of the PolarFire SoC package and the heat sinks base are not smooth. The surface roughness reduces the effective contact area between the package and the heat sinks base. The insulating air gaps created by voids between contacting surfaces are too large. The thermal interface materials fill these gaps and allow an effective conductive transfer of heat from the package to the external heat sink.

The selection of the appropriate thermal interface material is critical to ensure the lowest thermal contact resistance. One must consider the thermal conductivity of the TIM:

- The flatness of the surface contact areas
- The applied pressure on the thermal interface material
- The total thermal contact area.

In addition to thermal performance, TIMs are selected based on the ease of use in assembly and long-term reliability.

7.1 Heat Sink Attachments

There are six main methods for heat sink attachment. The following table lists their advantages and disadvantages.

- Thermal tape
- Thermally conductive adhesive
- Wire form Z-clips
- Plastic clip-ons
- Threaded stand-offs (PEMs) and compression springs
- Push-pins and compression springs
- Thermal compound (also called as thermal gel, thermal grease, thermal paste, heat-sink paste, or heat-sink compound)

8. Heat Sink Removal Procedure

The heat spreader on the package provides mechanical protection for the die and serves as the primary heat dissipation path. It is attached with an epoxy adhesive to provide the necessary adhesion strength to hold the package together. For an application in which an external heat sink subjects the lid adhesion joint to continuous tension or shear, extra support might be required.

If the removal of an attached external heat sink subjects the joint to tension, torque, or shear, care should be exercised to ensure that the lid itself does not come off. In such cases, it is recommended to use a small metal blade or metal wire to break the lid to heat sink joint from the corners and carefully pry the heat sink off. The initial cut should reach far enough so the blade has leverage to exert upward pressure against the heat sink. Contact the heat sink and heat sink adhesive manufacturer for more specific recommendations on heat sink removal.

9. Recommended PCB Design Rules for BGA Packages

Microchip provides the diameter of a land pad on the package side. This information is required before starting the board layout so the board pads can be designed to match the component-side land geometry. The typical values of these land pads are shown in the following figure and summarized in Table 9-1. For Microchip BGA packages, Non-Solder Mask Defined (NSMD) pads on the board are suggested to allow a clearance between the land metal (diameter) and the solder mask opening (diameter) as shown in the following figure.

The space between the NSMD pad and the solder mask, the actual signal trace widths, and via dimensions depend on the capability of the PCB vendor. The cost of the PCB is higher when the line width and spaces are smaller.

Figure 9-1. Ball and Via Dimensions

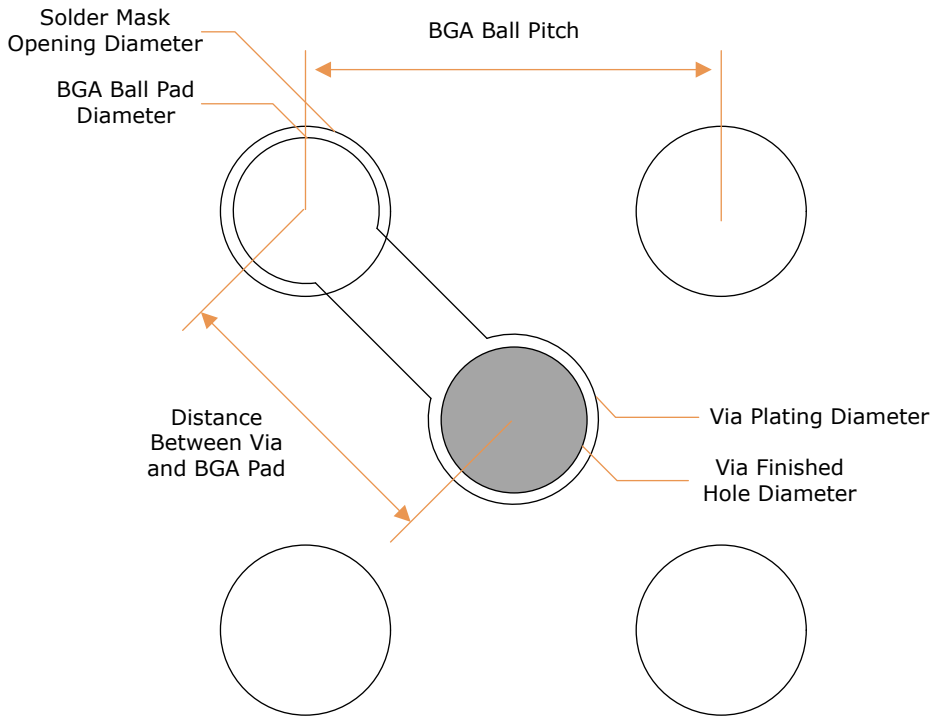


Table 9-1. Recommended PCB Design Rules

Design Rule for Packages	0.8 mm Pitch	1.0 mm Pitch	0.5 mm Pitch
	FCVG	FCG	FCSG
Ball Pad diameter	0.5 mm	0.6 mm	0.35 mm
Ball Pad opening	0.4 mm	0.5 mm	0.275 mm
Solder Ball pitch	0.8 mm	1.00 mm	0.50 mm
Line width between via and solder land	—	—	—
Distance between via and solder land	—	—	—
Via finished hole diameter	—	—	—
Via plating diameter	—	—	—

Note: For more information about package fanout, see *PolarFire SoC FPGA Package Fanout Application Note* (yet to be published).

10. Moisture Sensitive Level (MSL)

The following table lists MSL of Microchip PolarFire SoC packages'. For more information about solder re-flow guidelines for Sn/Pb and Pb-free, see https://www.microsemi.com/company/quality/soldering-profiles.

Table 10-1. Moisture Sensitive Levels

Package	MSL
FCG1152	4
FCVG784	4
FCVG484	4
FCSG536	3

11. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most— current publication.

11.1 Revision B

The following is a summary of the changes made in revision B of this document.

- Updated Table 1-1
- Updated 1.3.1.1 Supported I/O Features
- Updated Table 1-4
- Updated Table 1-5
- Updated 1.5 Mechanical Drawings
- Updated Table 1-10
- Updated Table 2-1
- Updated Table 9-1
- Updated Table 10-1

11.2 Revision A

The following is a summary of the changes made in revision A of this document.

- Updated Table 1-1
- Updated Table 1-2
- Updated Table 1-3
- Updated Table 1-6

11.3 Revision 2.0

The following is a summary of the changes made in revision 2.0 of this document.

- Updated 1.3.2 MSS I/Os. Added refer to PolarFire SoC Packaging Pin Assignment Table for the pin out information for the MSS pins.
- Deleted Unused Condition columns from all the details. Added refer to UG0901: PolarFire SoC FPGA Board Design Guidelines User Guide.
- Added LPDDR4 memory in 1.3.5 DDR Interface.
- Updated 1.3.7 Dedicated I/O Bank Pins. Added UG0901: PolarFire SoC FPGA Board Design Guidelines User Guide.
- Updated 1.3.8 XCVR Interface. Added UG0901: PolarFire SoC FPGA Board Design Guidelines User Guide.

11.4 Revision 1.0

The first publication of this document.

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