

# HDSDI-Daughter Board

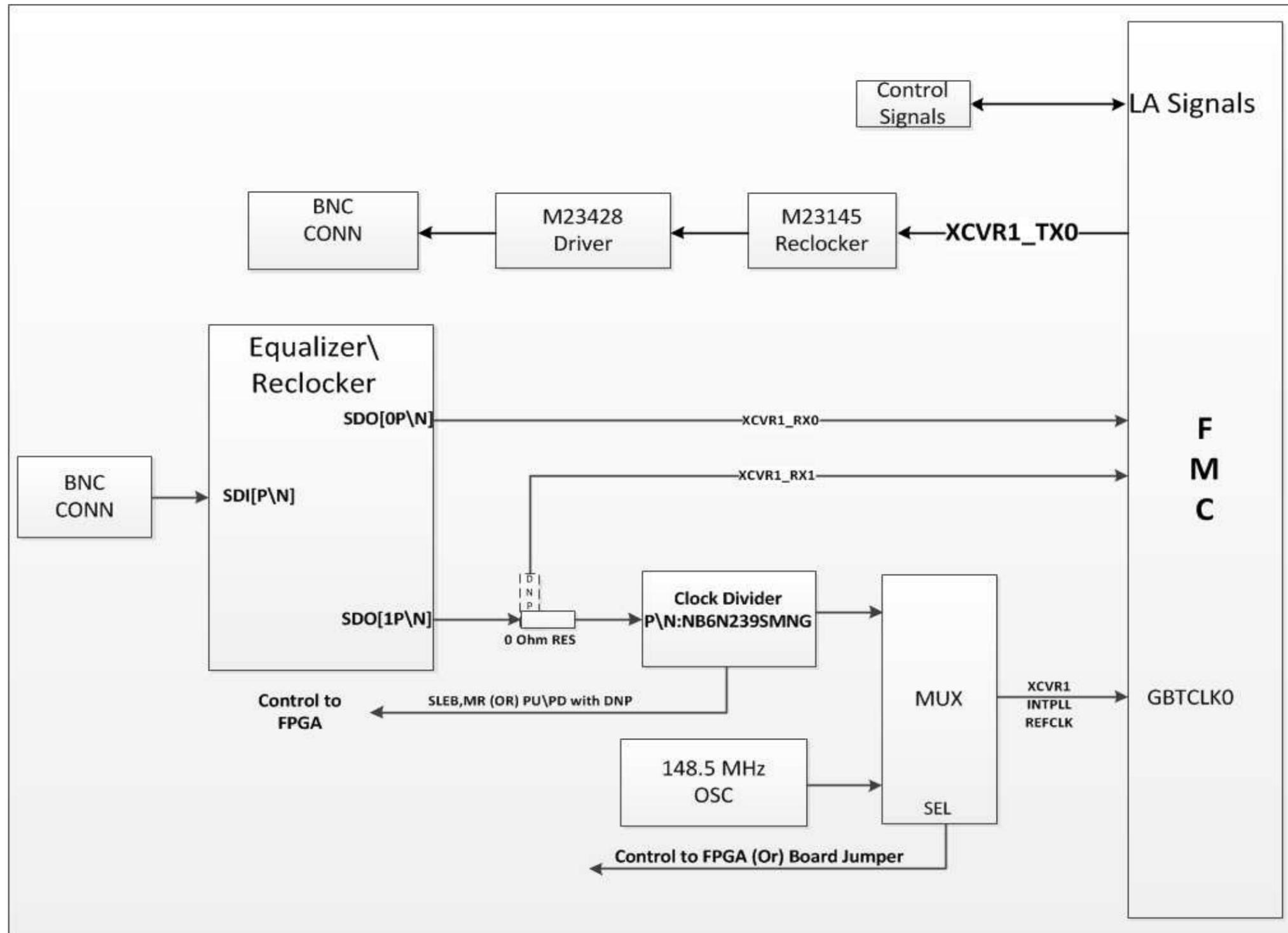
PAGE NO	TITLE
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03	12G HD-SDI TX/RX CONN
04	CLOCK MULTIPLEXER
05	FMC_MALE_CONNECTOR



Project Name: <b>HDSDI-Daughter Board</b>		
Rev <b>1</b>	Part Number: MICROSEMI <b>DVP-100-000514-001</b>	PACTRON:
Originator: <b>GHURU KUMARAVELU</b>		
Size <b>A</b>	Date: <b>Monday, July 09, 2018</b>	Sheet <b>8</b> of <b>12</b>

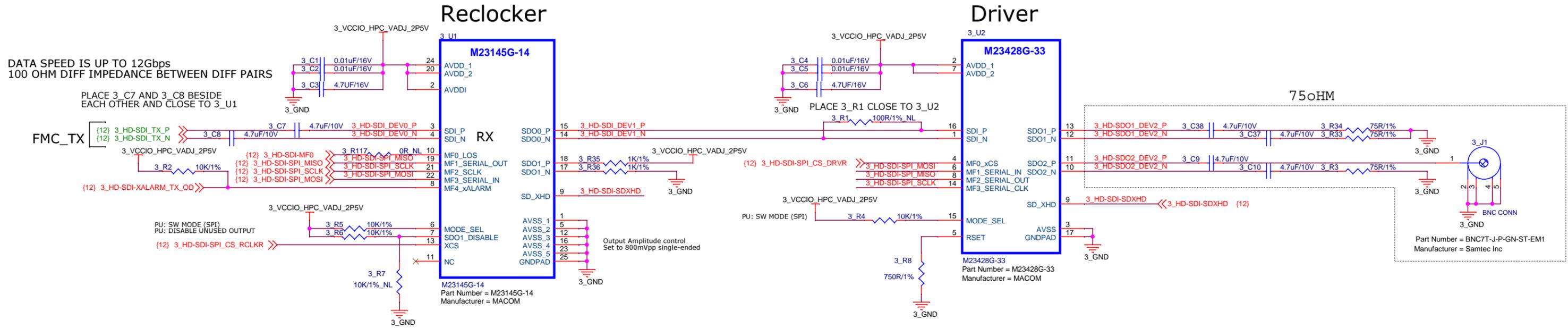
# HD-SDI\_FMC\_DAUGHTER\_BOARD

## BLOCK\_DIAGRAM



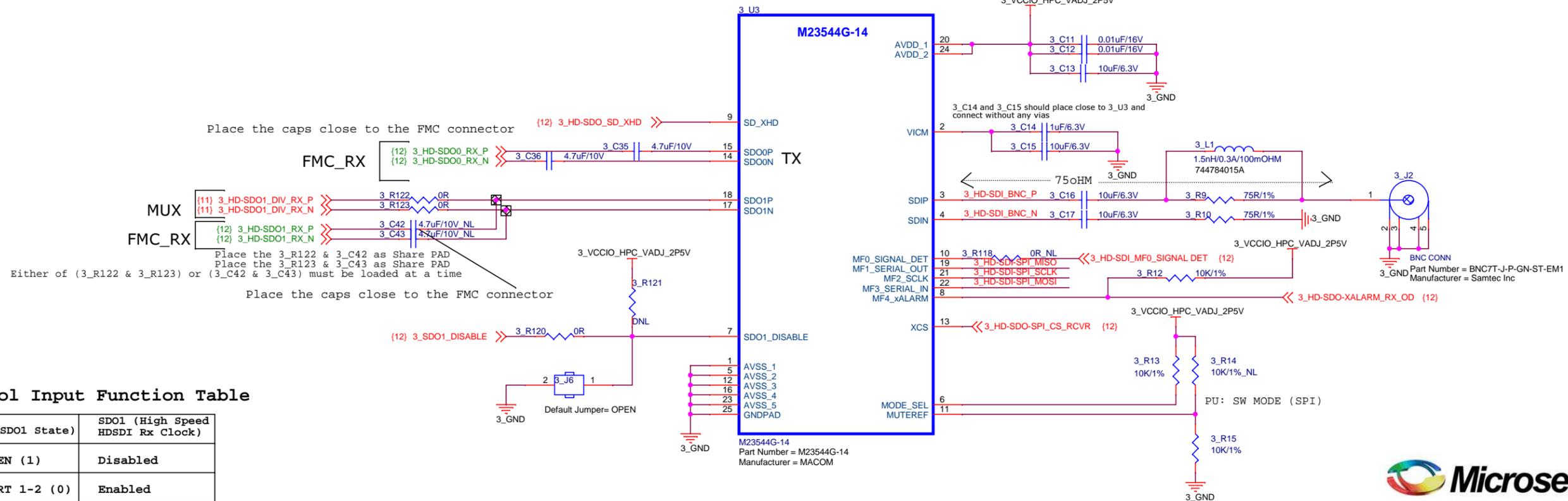
TITLE			
HSDI-Daughter Board			
Microsemi			
SIZE	DOCUMENT NO.	DVP-100-000514-001	REV
Custom			1
DATE:		Monday, July 09, 2018	SH 9 OF 12

# 12G HD-SDI Transmitter



# 12G HD-SDI Receiver

## Equalizer/ Reclocker



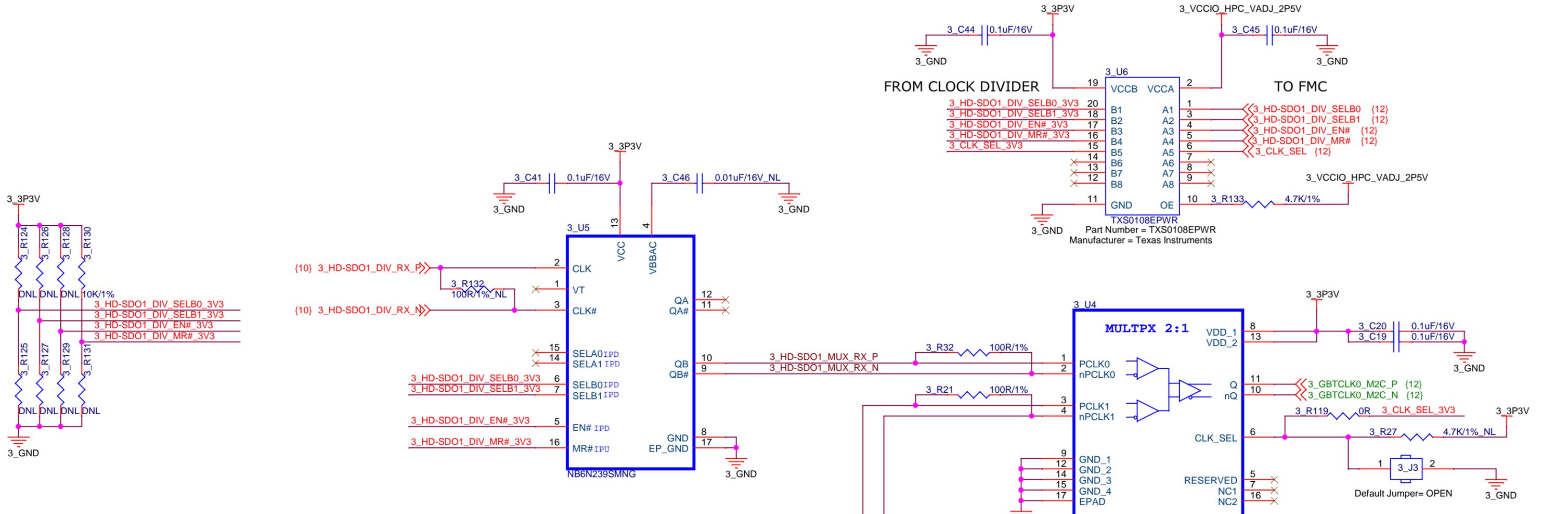
Control Input Function Table

J6 (SD01 State)	SD01 (High Speed HDSOI Rx Clock)
OPEN (1)	Disabled
SHRT 1-2 (0)	Enabled

TITLE: HDSOI-Daughter Board		
Microsemi		
SIZE: Custom	DOCUMENT NO. DVP-100-000514-001	REV: 1
DATE: Monday, July 09, 2018	SH 10 OF 12	



# DIFFERENTIAL-TO-LVDS CLOCK MULTIPLEXER FMC-GBTCLK0



HD-SDI default clock is 148.25 MHz

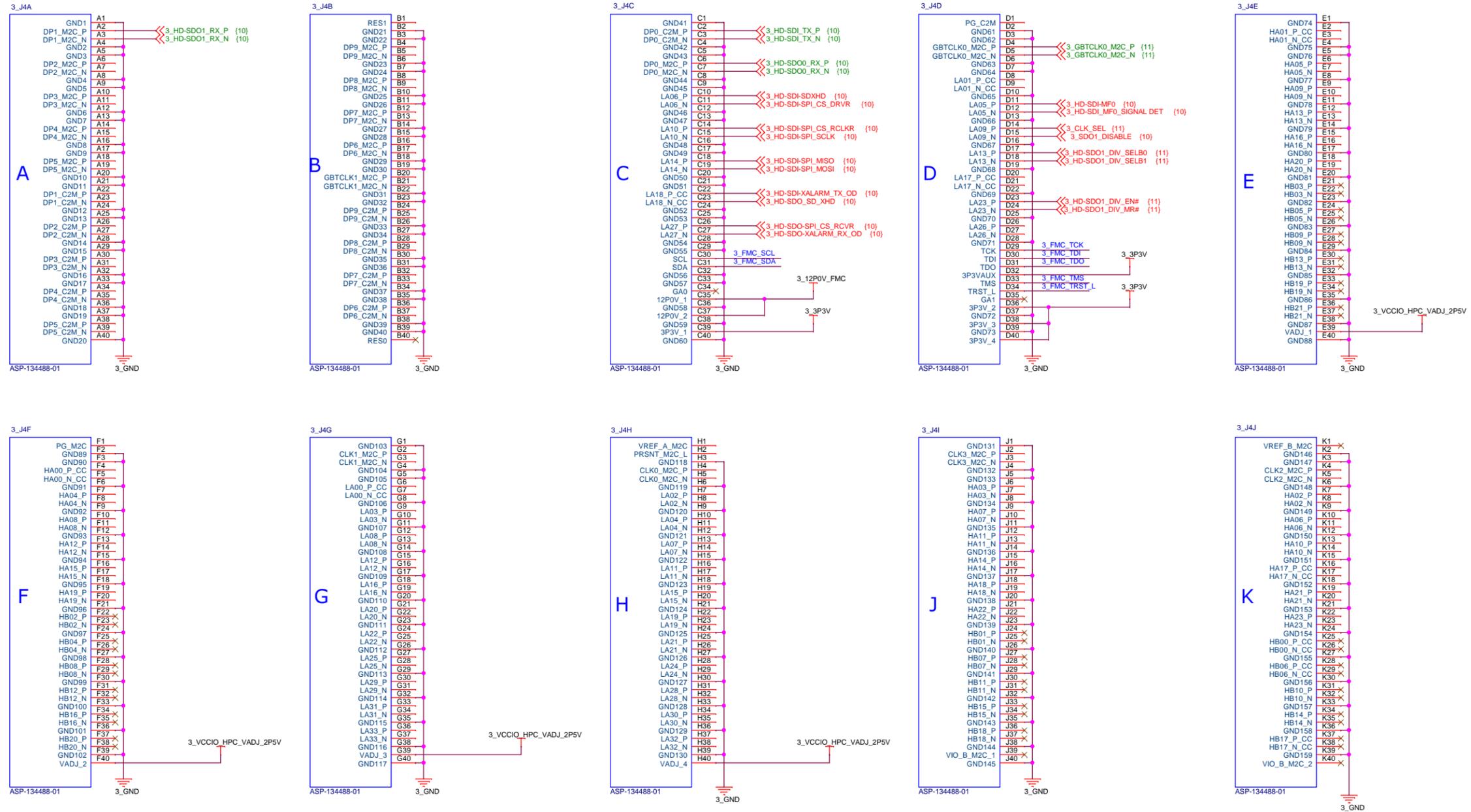
Control Input Function Table

CLK_SEL	PCLK Selected
0	PCLK0, nPCLK0
1	PCLK1, nPCLK1

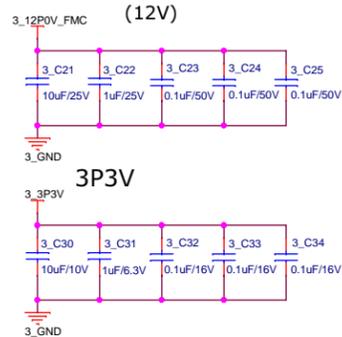


<b>TITLE</b> HSDSI-Daughter Board			
<b>Microsemi</b>			
<b>SIZE</b> B	<b>DOCUMENT NO.</b> DVP-100-000514-001	<b>REV</b> 1	<b>SH</b> 11 <b>OF</b> 12
<b>DATE:</b> Monday, July 09, 2018			

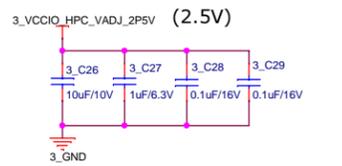
# FMC Male Connection



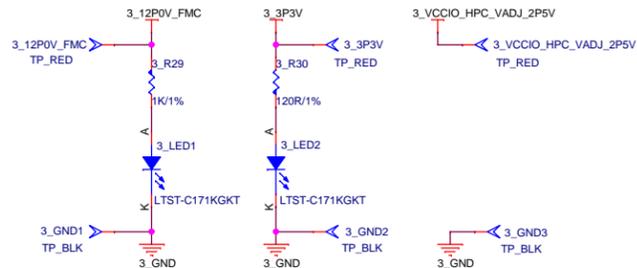
## 12P0V\_FMC



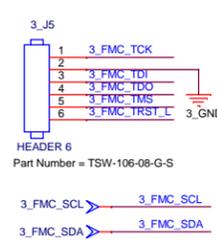
## VCCIO\_HPC\_VADJ



## INDICATION LED



## JTAG HEADER



TITLE		HDSI-Daughter Board	
Microsemi			
SIZE	DOCUMENT NO. DVP-100-000514-001	REV	1
DATE	Monday, July 08, 2018	SR	12 OF 12