# Libero SoC v11.9 SP5

# Release Notes

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# Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

## Revision 1.0

Revision 1.0 is the first publication of this document.

# Contents

# 1 Libero SoC v11.9 SP5 Release Notes

The Libero® system on chip (SoC) v11.9 SP5 is a service pack release of the Libero SoC v11.9 software for designing with Microsemi's power efficient flash FPGAs, SoC FPGAs, and rad-tolerant FPGAs. The suite integrates industry standard Synopsys Synplify Pro® synthesis and Mentor Graphics ModelSim® simulation with best-in-class constraints management, debug capabilities, and secure production programming support.

To access datasheets, silicon user guides, tutorials, and application notes, visit www.microsemi.com, navigate to the relevant product family page, and click the **Documentation** tab. Development Kits & Boards are listed in the **Design Resources** tab.

*Note:* Enhancements and new features for SmartFusion2, IGLOO2, and RTG4 device families will no longer be added to the Libero SoC v11.9 software branch. Please create new projects in **Libero SoC v12.2** release or later using the **Enhanced Constraints Flow**.

*Note:* The Classic Constraints Flow is no longer recommended for SmartFusion2, IGLOO2, and RTG4. Consider migrating such designs to a new project using the **Enhanced Constraints Flow**. Refer to the Migration Guide.

# 2 What's New in Libero SoC v11.9 SP5

Libero SoC v11.9 SP5 includes the following features and enhancements:

## 2.1 RTG4 Enhanced PLL Calibration

Libero SoC v11.9 SP5 includes a new RTG4 Fabric CCC configurator core to remove PLL lock stability dependence on the operating junction temperature across the supported RTG4 operating temperature range (CN19009).

- New RTG4 Fabric Clock Conditioning Circuit (FCCC **v2.1.009**) with Enhanced PLL Calibration for non-triplicated PLL

In this release, enhanced PLL calibration is being offered for RTG4 Fabric CCCs operating in the non-triplicated PLL mode. Support for the triplicated Fabric PLL mode will be added in a future release. Similarly, enhanced PLL calibration will be added to an upcoming release of the RTG4 DDR Memory Controller and High-Speed Serial Interface cores that generate register initialization microcode (for use with CoreABC). These upcoming core revisions will add PLL calibration initialization sequences to the DDR FPLL and PCIe/XAUI SPLL.

## 2.2 RTG4 Fabric Clock Conditioning Circuit (FCCC)

The RTG4 Fabric Clock Conditioning Circuit (FCCC **v2.0.104**) no longer supports PLL Lock window settings of 500 ppm and 1000 ppm. Upon generation, the PLL Lock window setting is validated against the maximum Phase/Frequency Detector (PFD) rate. Refer to the RTG4 Clocking Resources User Guide (UG0586) Lock Window section containing a minimum lock window formula for a given PLL configuration.

Existing designs will have their design state invalidated to the Pre-synthesis state upon opening with Libero SoC v11.9 SP5. The log window will print an invalidation message asking the user to update the FCCC and regenerate the affected component instances. Consider migrating to the RTG4 FCCC with Enhanced PLL Calibration core as described in section 3 below.

## 2.3 ProASIC3 Silicon Support

Libero SoC v11.9 SP5 includes the new A3P1000-FCG256M (STD speed grade) device.

## 2.4 SmartFusion2 MSS Watchdog Timer: WD_TIMEOUT port can no longer be exposed to Fabric

Libero SoC v11.9 SP5 and Libero SoC v12.2 add a Design Rule Check (DRC) to the SmartFusion2 MSS Watchdog Timer. Starting with this release, the WD_TIMEOUT port can no longer be exposed to the FPGA fabric. The option to expose this port is now grayed-out in the MSS Watchdog Timer configurator and in the System Builder. If your design uses this port, you must edit your MSS Watchdog Timer configuration or your System Builder configuration as appropriate and disable the port. Refer to CN19020.

## 2.5 SmartFusion2 and IGLOO2 RGB Area Coverage Limitation

A specific Row Global Buffer (RGB) routing configuration used for routed clocks, promoted via RCLKINT macros, that span large areas in SmartFusion2 and IGLOO2 designs has been disabled as of Libero SoC v11.9 SP5 and Libero SoC v12.2 onwards. If your design uses such a configuration, you will not be able to generate a programming file using this release. In that case, rerun Place and Route using the Incremental option, and then regenerate the programming file. Refer to CN19024.2.

## 2.6 Multiple Constraints on DDR Inputs

Prior to Libero SoC v11.9 SP5, designs which applied multiple duplicate or overlapping constraints could face a scenario where SmartTime did not apply the last valid constraint entered, but instead applied a combination of the duplicate constraints.

Upgrade to Libero SoC v11.9 SP5 to ensure that only the last valid constraint is applied when duplicate constraints exist. Re-run static timing analysis with SmartTime using Libero SoC v11.9 SP5, if you are using multiple constraints on DDR inputs.

*Note:* Refer to Knowledge Base article SL5692 for tips to constrain DDR I/Os. Alternatively, migrate to Libero SoC v12.2 or later where the *-add_delay* SDC syntax is supported, allowing the user to add both rising and falling edge input delay constraints on the same port.

*Note:* Refer to Knowledge Base article KI9027 for an explanation of the issue with duplicate constraints on the DDR inputs.

# 3 Migrating an Existing RTG4 Design to Libero SoC v11.9 SP5

With Libero SoC v11.9 SP5, users opening existing designs have the choice to continue using the standard RTG4 FCCC core or manually migrating to the RTG4 FCCC with Enhanced PLL Calibration core.

Continuing with the PLL instantiated via the standard RTG4 FCCC core means that the PLL lock stability will be dependent on the operating junction temperature as discussed in CN19009. Users are encouraged to review the CN and confirm the supported temperature rise window for each PLL used in the design via the PLL Temp Rise Window calculator spreadsheet.

Migrating to the PLL instantiated in the RTG4 FCCC core with Enhanced PLL Calibration means that the non-triplicated fabric PLL lock stability is no longer dependent on the operating junction temperature.

Migration from the standard RTG4 FCCC core to the RTG4 FCCC with Enhanced PLL Calibration is recommended in the following scenario:

- The non-triplicated RTG4 Fabric PLL is used in the design and the application must support operation at a junction temperature rise window beyond that predicted by the PLL Temp Rise Window calculator described in CN19009.

Designs using the FCCC without the PLL or with triplicated PLL (internal feedback) do not need to migrate to the Enhanced PLL Calibration core unless the CCC shares the device corner with another fabric CCC that is using the non-triplicated PLL. Designs using the triplicated PLL (via PLL internal feedback) can only use the standard FCCC core in this release. Enhanced calibration for the triplicated PLL is planned for a future release.

## 3.1 Summary of Migration Steps

1. Note the configuration of each CCC instantiated in the existing design. This can be done by either opening the configuration GUI for each CCC and saving screenshots of each tab, or by opening the CCC configuration report for each component instance.

    - Opening Existing CCC GUI: When opening an existing CCC in Libero SoC v11.9 SP5, the instance version must first be updated to RTG4 FCCC **v2.0.104** by right-clicking the component in the Design Hierarchy pane and selecting “Replace Component Version”

    Note: PLLs configured to Lock Window settings of 500 ppm or 1000 ppm will have their respective Lock Window setting reset to the 6000 ppm default

    - Using CCC configuration report: The configuration report is an XML file found in the example path shown below:
      `<libero_prj_folder>/component/work/<ccc_comp_name>/<inst_name>/<ccc_comp_name>_<inst_name>_configuration.xml`

    Note: The XML file can be viewed in a web browser if the rptstyle.xsl file is placed in the same folder as the XML file, before opening the file. The rtpstyle.xsl can be found in the Libero project folder path below:

    `<libero_prj_folder>/designer/<top_level_inst_name>/rptstyle.xsl`

2. Note the location and CCC number for each CCC instantiated in the existing design and group them by device corner (NW, NE, SW, or SE) and CCC number (0 or 1). This information is found in the Global Net Report available after running the Place and Route design flow step. Refer to the CCC Input Connections table for the CCC Location column to identify the die corner (NW,

NE, SW, or SE) and CCC number (0, or 1). For example, a CCC Location can be listed as CCC-SE1 for CCC #1 in the Southeast corner.

- The Global Net Report can be viewed in the Libero Reports tab under the Place and Route report list or by opening the file directly in a web browser from the default file location within the project folder. The file name format follows the convention: `<top_level_inst_name>_glb_net_report.xml` and it can be found in the project folder path `<libero_prj_folder>/designer/<top_level_inst_name>/`.

3. Delete all existing CCC instances that are being migrated to the CCC with Enhanced PLL Calibration, even those not using the PLL, if they share the device corner location with a PLL that *is* being migrated.
4. Configure a new instance of RTG4 FCCC with Enhanced PLL Calibration **v2.1.009** for each pair of CCCs being migrated.
    - Use the CCC configurations noted in step 1 above for each CCC location per device corner, ensuring that respective settings are mapped to the correct CCC tab in the configuration GUI for CCC_0 and CCC_1.
    - Refer to the RTG4 FCCC with Enhanced PLL Calibration Configurator User Guide for information about using the configurator GUI.
    - Refer to UG0586: RTG4 Clocking Resources User Guide *revision 8 or newer* for information about the CCC / PLL settings and use models, including Lock Window settings and Auto-Reset logic.
5. Open the Constraints Manager from the Design Flow tab, and click **Derive Constraints** in the Timing tab to generate the required clock and false-path constraints for the CCC/PLL instances.
6. Integrate the new CCC component into the design hierarchy by replacing the module instantiations and connections to the standard FCCC with an instantiation of the new FCCC with Enhanced PLL Calibration containing ports for CCC_0 and CCC_1 on the same component instance.

# 4 RTG4 New Cores

The following table lists new RTG4 cores for Libero SoC v11.9 SP5.

| Core | Version | Description |
|---|---|---|
| RTG4 FCCC with Enhanced PLL Calibration | 2.1.009 | The enhanced PLL calibration removes any Fabric PLL lock stability dependence on the operating junction temperature across the supported RTG4 operating temperature range for non-triplicated PLL. |
| RTG4 Clock Conditioning Circuit (CCC) | 2.0.104 | PLL Lock Window settings of 500 ppm or 1000 ppm are no longer supported. The Lock Window setting will be reset to the 6000 ppm default upon opening the configuration core. Upon generation, the setting is validated against the maximum PFD rate. |
| RTG4 CCC APB Interface | 1.1.109 | Resolve hold violations |

# 5 Resolved Issues

The following table lists the customer-reported SARs resolved in Libero SoC v11.9 SP5. Resolution of previously reported “Known Issues and Limitations” is also noted in this table.

## 5.1 List of Resolved Issues

| Case Number | Description |
|---|---|
| 493642-2576826423 | Inconsistent SmartTime behavior for DDR in Libero v11.9 |
| 493642-2598159498 | Incorrect functioning of Libero Constraint Checker A3P device |
| 493642-2590132384 | PROASIC3E: invalid timing constraints path should be reported in Libero SoC as reported in Libero IDE |
| 493642-2649856222 | SmartFusion2 Watchdog configurator does not match silicon behavior |
| 493642-2613431562; 493642-2633681357 | Classic Constraints Flow Only: Libero Not Responding after opening SynplifyPro |
| 493642-2552029001 | Functional failure: state machine is not changing its state on the edge detect trigger event |
| 493642-2601274887 | Mismatch in the hardwired net from IOPAD_IN:Y to GBM:An between post-layout simulation and SmartTime reports |

# 6 Known Limitations, Issues and Workarounds

Known issues from Libero SoC v11.9 and its service packs may also apply to Libero SoC v11.9 SP5. Review the Libero SoC v11.9 Release Notes for Known Issues in Libero SoC v11.9.

## 6.1 Generating RTG4FCCC and RTG4FCCCECALIB cores in the same design shows an error message in the Log Window

If you generate RTG4FCCC and RTG4FCCCECALIB cores in the same design, you will see the following error message in the Log Window:

```
Error: The BUFD_DELAY module is defined in multiple files. Duplicate modules
are not supported.

Select the file you want to use from the Design Hierarchy.
```

This message will not cause any stoppage to the design flow and can be ignored.

## 6.2 Secure IP flow is failing at Compile when Mentor simulation key is removed

Compile fails in the Secure IP flow when the Mentor simulation key is removed. This issue is fixed in the Libero SoC v12.0 release.

## 6.3 FlashPro will error out, if an existing PDB is modified to disable the fabric

If an existing PDB file is modified to disable the fabric and programmed only with eNVM, FlashPro will error out.

**Workaround:**
Create a new FlashPro project and create a new PDB. Enable eNVM and import the efc file required for programming eNVM. Save the PDB and use this PDB to program the device.

## 6.4 SmartTime reports False Failure during max/best or min/worst case analysis

Timing reports may have incorrect slacks for the secondary corners “max/best” and “min/worst” if they were created with the constraint coverage option turned on. The reports for “max/worst” and “min/best” corners are not affected.

**Workaround:**

1. First, enable the constraint coverage option before running Verify Timing to generate and analyze the coverage report (but disregard the timing reports for “max/best” and “min/worst”). Then, disable the constraint coverage option before re-running Verify Timing to generate and analyze the timing reports at all corners, including “max/best” and “min/worst”.
2. Upgrade to Libero SoC v12.0 or later, where this issue has been fixed.

## 6.5 RTG4CCCECALIB generation fails when only local clock outputs are used

Generation of the RTG4CCCECALIB configurator fails when only local clock outputs are used.

**Workaround:** To use local clocks Y[0..3], select the GL associated with Y[0..3] which has lower frequency.

# 7 System Requirements

For information about operating system support and minimum system requirements, see the System Requirements web page.

For Linux OS setup instructions, see How to Set Up Linux Environment for Libero User Guide:

## 7.1 Operating System Support

### Supported

- Windows 7, Windows 10
- RHEL 5*, RHEL 6, RHEL 7, CentOS 5*, CentOS 6, and CentOS 7
- SuSE 11 SP4 (Libero only. FlashPro Express, SmartDebug, and Job Manager are not supported.)

**Note:** * RHEL 5 and CentOS 5 do not support programming using FlashPro5.

# 8 Libero SoC v11.9 SP5 Download

Click the following links to download Libero SoC v11.9 SP5 on Windows and Linux operating systems:

- Windows Download
- Linux Download

**Note:** Installation requires administrator privileges to the system.

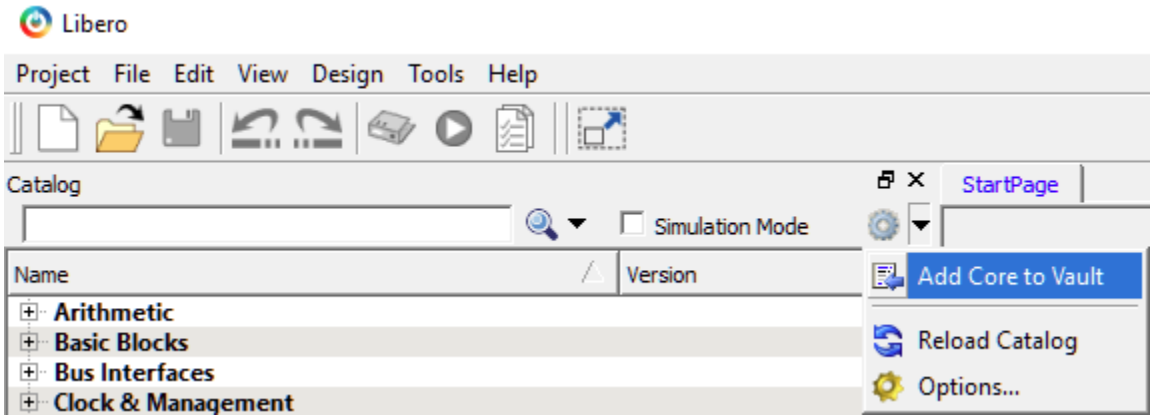
Libero SoC v11.9 SP5 is an incremental service pack and can be installed over Libero SoC v11.9 or Libero SoC v11.9 SP4.

After successful installation, clicking **Help-> About Libero** will show Version: 11.9.5.5.

## 8.1 Instructions for Megavault Users

Several cores have changed between Libero SoC v11.9 SP4 and vSP5: As a result, if you do not permit Libero to have access to the Internet, you must do the following:

1. Download and install the Megavault for Libero SoC v11.9 if you have not already done so
   a. Ensure that you have write access to the Megavault
2. Download the following files:
   - Actel_SgCore_RTG4FCCCECALIB_2.1.009.cpz
   - Actel_SgCore_RTG4FCCC_2.0.104.cpz
   - Actel_SgCore_RTG4CCCAPB_IF_1.1.109.cpz
3. Install and open Libero SoC v11.9 SP5. From Libero:
   a. Set the vault location to that of the Megavault
   b. Switch to the Catalog view by clicking View -> Windows -> Catalog
   c. Click “Add Core to Vault” to import the .cpz files listed above




The above steps need only be done once per instance of a Megavault; they do not need to be repeated for other users whose Libero install points to the same instance of the Megavault

## 8.2 Downloading SoftConsole 3.4/4.0/5.1

Libero SoC v11.9 SP5 is compatible with SoftConsole v3.4 SP1, SoftConsole v4.0 and SoftConsole v5.x

- SoftConsole Download