Total Ionizing Dose Test Report

No. 17T-RTSX32SU-CQ256-D1LK51

April 13, 2017

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I. Summary Table

Parameter	Tolerance
1. Gross Functionality	Passed 100 krad (SiO_2)
2. Power Supply Current (ICCA/ICCI)	Passed 60 krad (SiO_2)
3. Input Threshold (VTIL/VIH)	Passed 100 krad (SiO_2)
4. Output Drive (VOL/VOH)	Passed 100 krad (SiO_2)
5. Propagation Delay	Passed 100 krad (SiO_2) for 10% degradation criterion
6. Transition Characteristics	Passed 100 krad (SiO_2)

II. Total Ionizing Dose (TID) Testing

This testing is designed on the base of an extensive database (see TID data of antifuse-based FPGAs at http://www.klabs.org and http://www.microsemi.com/soc) accumulated from the TID testing of many generations of antifuse-based FPGAs.

A. Device-Under-Test (DUT) and Irradiation Parameters

Table 1 lists the DUT and irradiation parameters. During irradiation each input or output is grounded through a resistor; during annealing each input or output is grounded through a 1-k ohm resistor. Appendix A contains the schematics of the bias circuit.

Table 1 DUT and Irradiation Parameters

Part Number	RTSX32SU
Package	CQ256
Foundry	United Microelectronics Corp.
Technology	0.25 μm CMOS
DUT Design	TDSX32SCQFP256
Die Lot Number	D1LK51
Quantity Tested	6
Serial Number	100 krad(SiO2): 11170, 11255 60 krad(SiO2): 11118, 11134 40 krad(SiO2): 11048, 11080
Radiation Facility	Defense Microelectronics Activity
Radiation Source	Co-60
Dose Rate (±5%)	10 krad(SiO_2)/min
Irradiation Temperature	Room
Irradiation and Measurement Bias (VCCI/VCCA)	Static at 5.0 V/2.5 V

B. Test Method

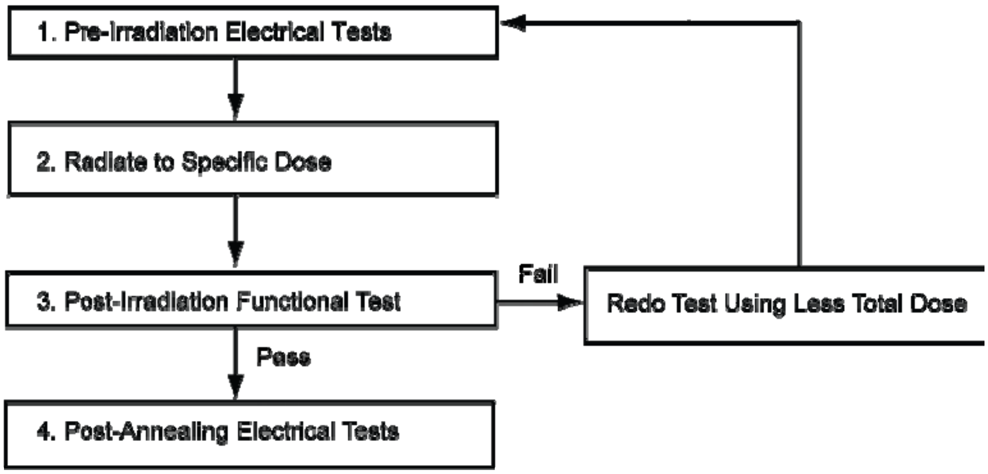

Figure 1 Parametric Test Flow Chart

The test method generally follows the guidelines in the military standard TM1019.8. Figure 1 is the flow chart describing the steps for functional and parametric tests, irradiation, and post-irradiation annealing.

The accelerated aging, or rebound test mentioned in TM1019.8 is unnecessary because there is no adverse time-dependent effect (TDE) in Microsemi products manufactured by deep sub-micron CMOS technologies. Elevated temperature annealing basically reduces the effects originating from radiation-induced leakage currents. As indicated by test data in the following sections, the predominant radiation effects in RTSX72SU are due to radiation-induced leakage currents.

Room temperature annealing is performed in this test; the duration is approximately 7 days.

C. Design and Parametric Measurements

DUTs use a high utilization generic design (TDSX32CQFP256) to test total dose effects in typical space applications. Appendix B contains the schematics illustrating the logic design.

Table 2 lists each electrical parameter and the corresponding logic design. The functionality is measured on the output pins (O_AND3 and O_AND4) of two combinational buffer-strings with 1400 buffers each and output pins (O_OR4 and O_NAND4) of a shift register with 1536 bits. ICC is measured on the power supply of the logic-array (ICCA) and I/O (ICCI) respectively. The input logic thresholds (VTIL/VIH) and output-drive voltages (VOL/VOH) are measured on combinational nets listed in Row 3 and 4 in Table 2. The propagation delays are measured on the O_AND4 output of one buffer string. The delay is defined as the time delay from the time of triggering edge at the CLOCK input to the time of switching state at the output O_AND4. Both the low-to-high and high-to-low output transitions are measured; the propagation delay is defined as the average of these two transitions. The transition characteristics, measured on the output O_AND4, are displayed as oscilloscope snapshots showing the rising and falling edge during logic transitions.

Table 2 Logic Design for Parametric Measurements

Parameters	Logic Design
1. Functionality	All key architectural functions (pins O_AND3, O_AND4, O_OR3, O_OR4, and O_NAND4)
2. ICC (ICCA/ICCI)	DUT power supply
3. Input Threshold (VIL/VIH)	Input buffers (DA/QA0, DAH/QA0H, ENCNTRH/YO0H, IDII0/IDIO0, IDII1/IDIO1, IDII2/IDIO2, IDII3/IDIO3, IDII4/IDIO4, IDII5/IDIO5, IDII6/IDIO6, IDII7/IDIO7)
4. Output Drive (VOL/VOH)	Output buffer (DA/QA0)
5. Propagation Delay	String of buffers (pin LOADIN to O_AND4)
6. Transition Characteristic	D flip-flop output (O_AND4)

III. Test Results

A. Functionality

Every DUT passes the pre-irradiation, post-irradiation, and post-annealing functional tests.

B. Power Supply Current (ICCA and ICCI)

Table 3 summarizes the pre-irradiation, post-irradiation—right after irradiation and before anneal, and post-annealing ICCA and ICCI data.

Table 3 Pre-Irradiation, Post Irradiation and Post-Annealing ICC

DUT	Total Dose	ICCA (mA)			ICCI (mA)		
		Pre-irrad	Post-irrad	Post-ann	Pre-irrad	Post-irrad	Post-ann
11170	100 krad	6	222.6	67	1	164.4	56
11255	100 krad	6	149.5	48	1	119.9	38
11118	60 krad	6	10.5	10	1	28.4	12
11134	60 krad	6	8.9	7	1	19.4	8
11048	40 krad	6	3.7	1	1	3.8	2
11080	40 krad	6	2	2	1	3.3	3

In compliance with TM1019.8, the post-irradiation-parametric limit (PIPL) for the post-annealing ICCA/ICCI in this test is defined as the highest ICCA/ICCI in the RTSX32SU spec sheet of 25mA.

Figure 2 through Figure 7 plot the influx standby ICCA and ICCI versus total dose for each DUT.

There are unexpected ICCI increases during irradiation, as shown in Figures 3 through 7, where the ICCI would drop back at some points of time. The suspect is an intermittent continuity problem of the socket on the test board. The post-anneal ICCI measurements are more stable.

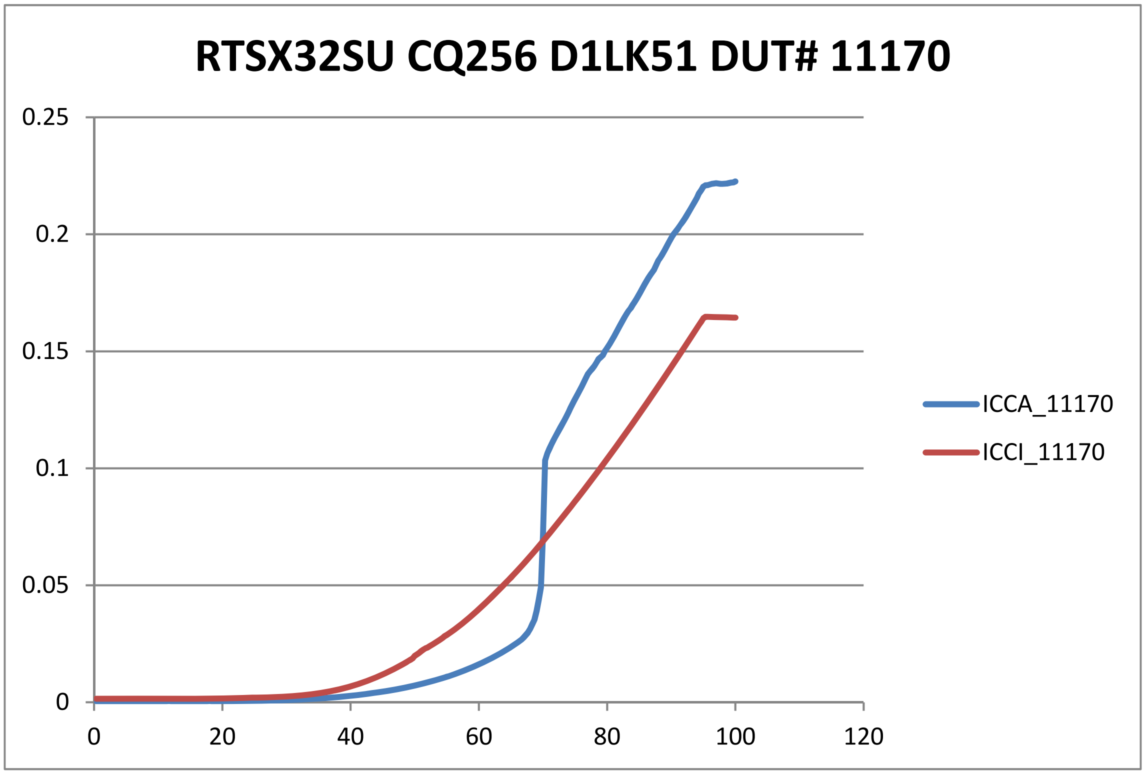

Figure 2 DUT 11170 Influx ICCA and ICCI

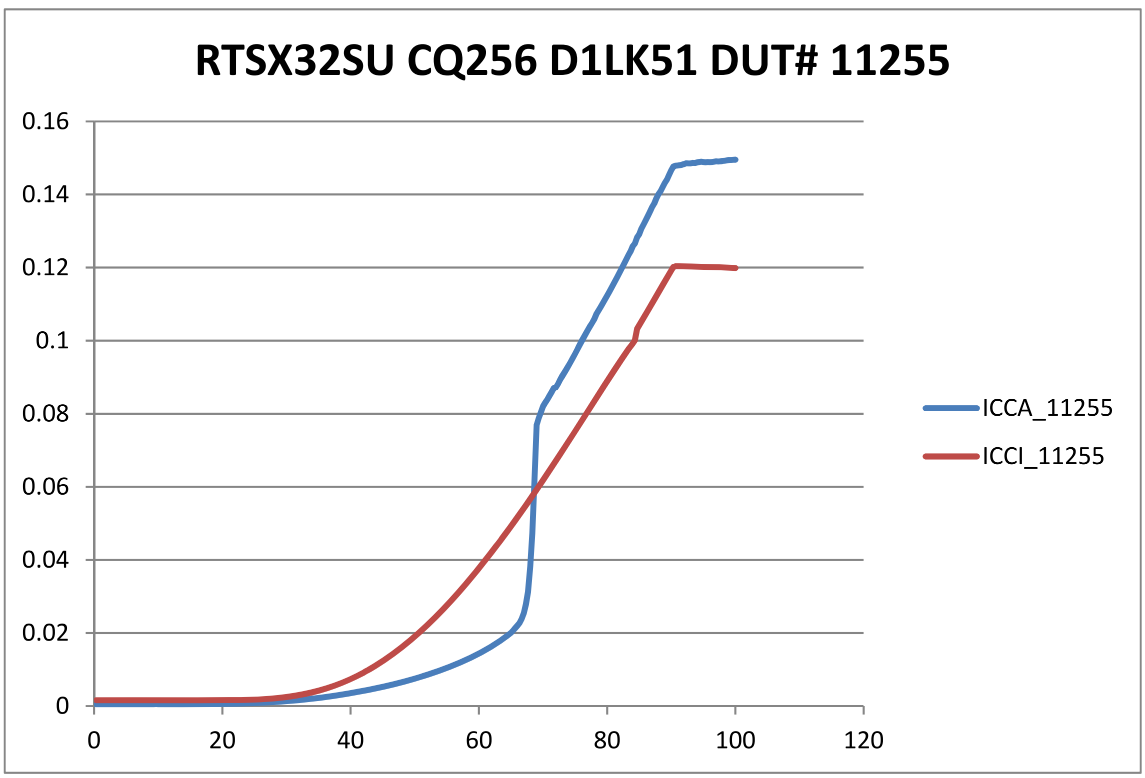

Figure 3 DUT 11255 Influx ICCA and ICCI

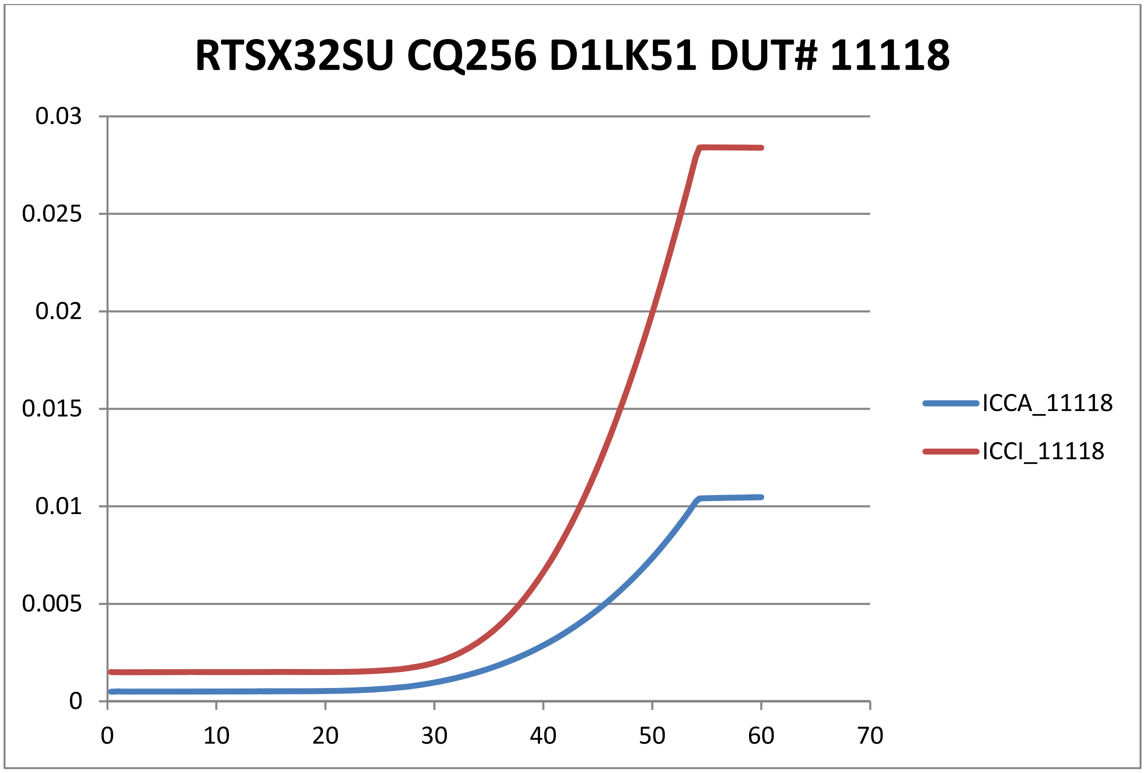

Figure 4 DUT 11118 Influx ICCA and ICCI

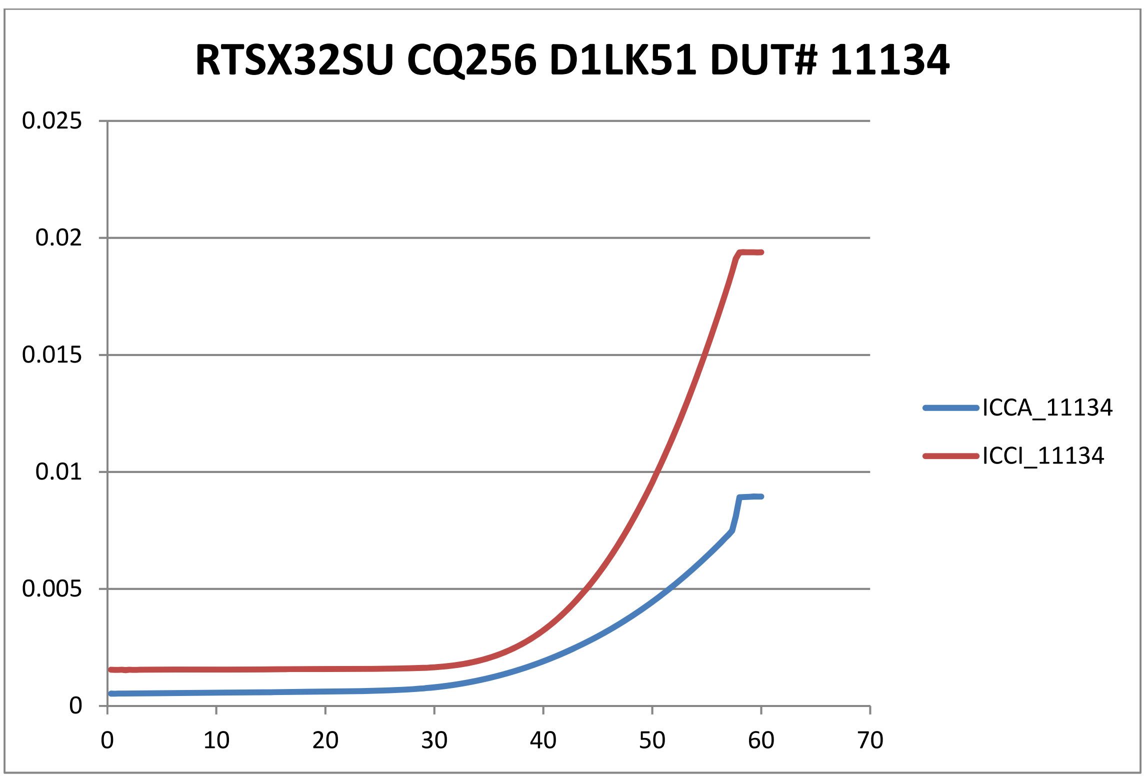

Figure 5 DUT 11134 Influx ICCA and ICCI

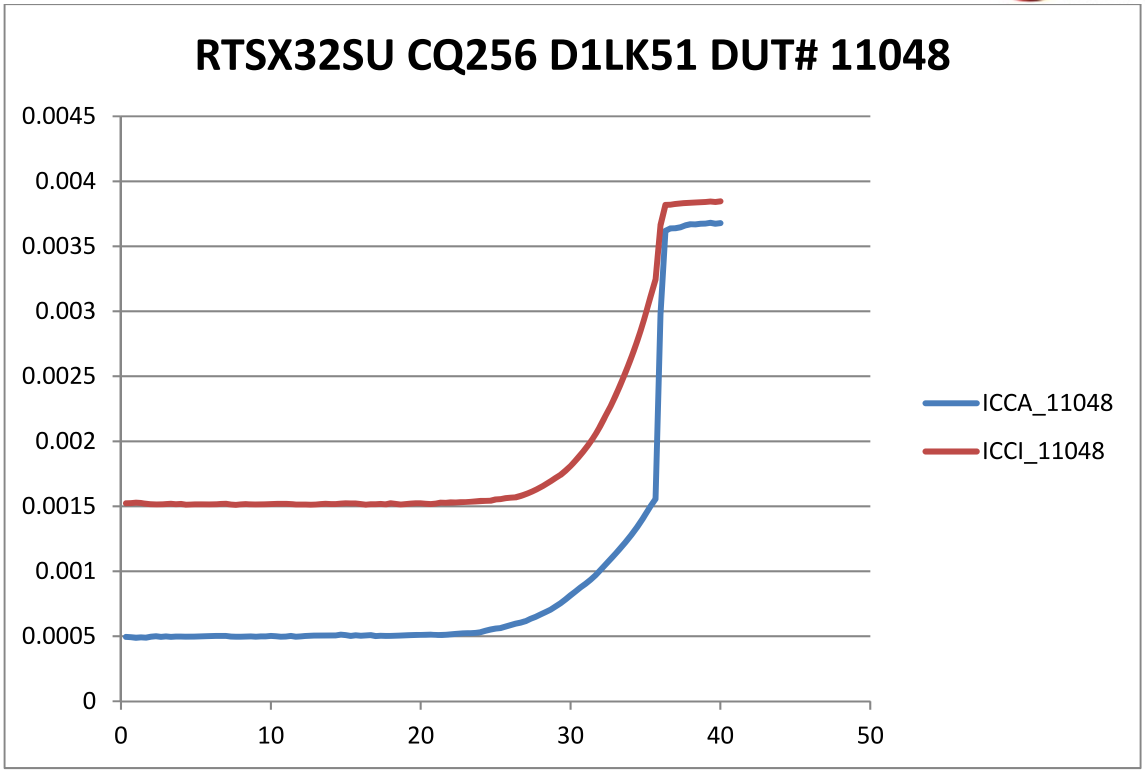

Figure 6 DUT 11048 Influx ICCA and ICCI

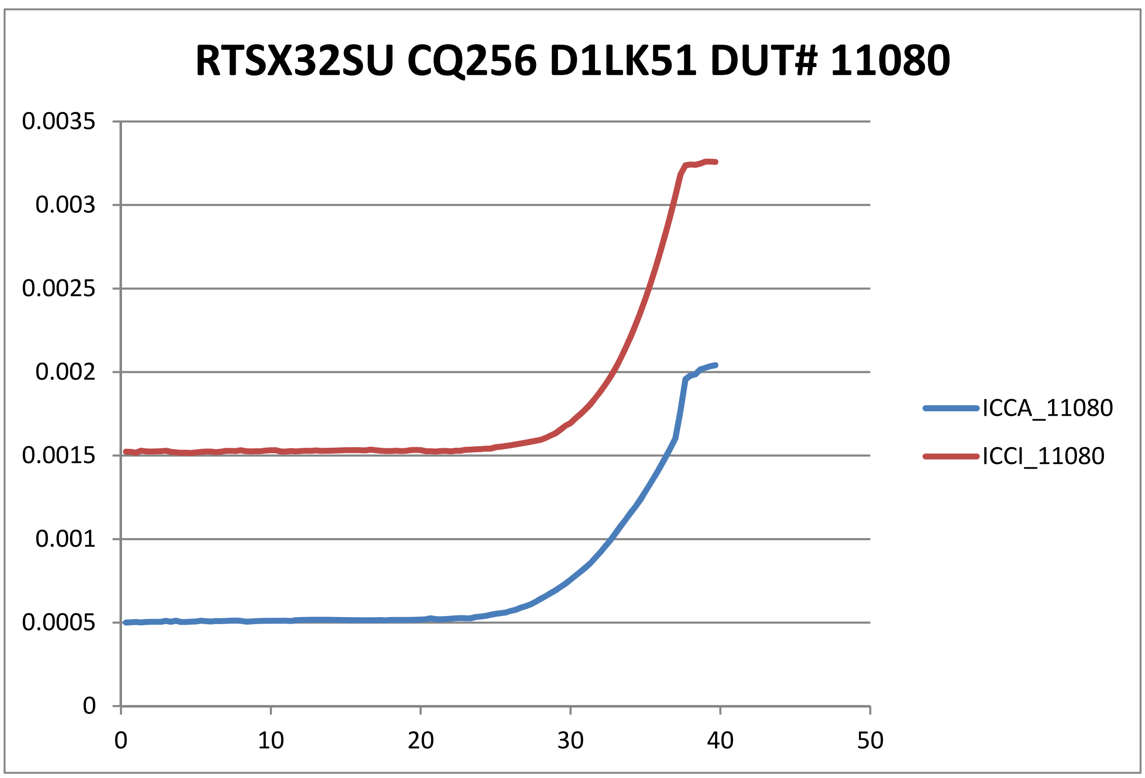

Figure 7 DUT 11080 Influx ICCA and ICCI

C. Input Logic Threshold (VIL/VIH)

Table 4a through Table 4c lists the pre-irradiation and post-annealing input logic thresholds. All data is within the specification limits. The post-annealing shift in every case is very small.

Table 4a Pre-Irradiation and Post-Annealing Input Thresholds

DUT	11170 (100 krad)				11255 (100 krad)			
Input Pin	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
	VIL (mV)		VIH (mV)		VIL (mV)		VIH (mV)	
DA/QA0	1405	1005	1460	1880	1490	1480	1425	1400
DAH/QA0H	1525	1530	1400	1440	1440	1475	1555	1425
ENCNTRH/YO0	1445	1545	1405	1600	1480	1475	1425	1575
IDII0/IDIO0	1425	1445	1555	1490	1455	1350	1530	1500
IDII1/IDIO1	1360	1320	1385	1475	1270	1205	1535	1385
IDII2/IDIO2	1245	1450	1565	1395	1500	1455	1415	1385
IDII3/IDIO3	1115	1150	1700	1710	1110	1115	1700	1665
IDII4/IDIO4	1455	1295	1500	1515	1385	1395	1420	1540
IDII5/IDIO5	1500	1465	1390	1455	1480	1470	1465	1425
IDII6/IDIO6	1350	1355	1425	1435	1420	1440	1495	1395
IDII7/IDIO7	1425	1455	1430	1430	1435	1435	1435	1435

Table 4b Pre-Irradiation and Post-Annealing Input Thresholds

DUT	11118 (60 krad)				11134 (60 krad)			
Input Pin	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
	VIL (mV)		VIH (mV)		VIL (mV)		VIH (mV)	
DA/QA0	1480	935	1405	1870	1385	1475	1520	1395
DAH/QA0H	1385	1565	1510	1415	1580	1395	1395	1495
ENCNTRH/YO0	1500	1535	1405	1575	1420	1480	1405	1395
IDII0/IDIO0	1425	1450	1515	1475	1360	1315	1570	1500
IDII1/IDIO1	1225	1310	1525	1450	1460	1225	1385	1415
IDII2/IDIO2	1450	1430	1380	1375	1555	1455	1565	1380
IDII3/IDIO3	1100	1105	1685	1690	1170	1100	1700	1680
IDII4/IDIO4	1395	1450	1415	1495	1335	1370	1495	1415
IDII5/IDIO5	1450	1455	1395	1390	1520	1425	1420	1375
IDII6/IDIO6	1375	1230	1485	1400	1435	1390	1425	1445
IDII7/IDIO7	1440	1420	1435	1390	1490	1410	1435	1400

Table 4c Pre-Irradiation and Post-Annealing Input Thresholds

DUT	11048 (40 krad)				11080 (40 krad)			
Input Pin	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
	VIL (mV)		VIH (mV)		VIL (mV)		VIH (mV)	
DA/QA0	1470	1465	1395	1585	1485	940	1655	1840
DAH/QA0H	1455	1422	1515	1500	1545	1600	1600	1400
ENCNTRH/YO0	1515	1515	1400	1395	1500	1490	1500	1390
IDII0/IDIO0	1425	1305	1515	1500	1380	1435	1555	1485
IDII1/IDIO1	1235	1220	1520	1505	1285	1305	1545	1465
IDII2/IDIO2	1460	1445	1385	1380	1485	1440	1435	1380
IDII3/IDIO3	1110	1095	1695	1695	1090	1105	1690	1685
IDII4/IDIO4	1390	1380	1500	1420	1400	1455	1535	1490
IDII5/IDIO5	1425	1430	1390	1385	1530	1500	1550	1415
IDII6/IDIO6	1375	1380	1490	1445	1430	1220	1475	1380
IDII7/IDIO7	1420	1430	1425	1410	1460	1420	1440	1415

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D. Output-Drive Voltage (VOL/VOH)

The pre-irradiation and post-annealing VOL/VOH are listed in Tables 5 and 6. The post-annealing data are within the specification limits.

Table 5a Pre-Irradiation and Post-Annealing VOL (mV) at Various Sinking Current

Sourcing Current	Pin\DUT	11170 (100 krad)		11255 (100 krad)	
		Pre-rad	Post-an	Pre-rad	Post-an
1 mA	QA0	11.1109	11.7889	11.4864	12.1331
	YQ0	11.1113	11.9671	10.7203	11.2322
12 mA	QA0	127.00	127.5662	131.3495	135.7488
	YQ0	126.4551	127.7303	122.4206	123.3362
20 mA	QA0	211.3783	211.3326	218.6066	225.398
	YQ0	210.4297	212.0781	203.7524	204.9318
50 mA	QA0	531.6183	528.922	549.4233	567.1913
	YQ0	529.1735	531.7365	512.8008	514.9263
100 mA	QA0	1087.9	1080.5	1124.6	1164.6
	YQ0	1083.8	1087.2	1050.7	1054.5

Table 5b Pre-Irradiation and Post-Annealing VOL (mV) at Various Sinking Current

Sourcing Current	Pin\DUT	11118 (60 krad)		11134 (60 krad)	
		Pre-rad	Post-an	Pre-rad	Post-an
1 mA	QA0	11.6115	11.4917	11.6272	11.0536
	YQ0	10.4388	11.7482	11.5178	10.9976
12 mA	QA0	132.2413	126.9873	131.4590	125.0786
	YQ0	118.5581	126.1197	129.6608	122.8202
20 mA	QA0	220.1556	210.4721	218.9821	208.1253
	YQ0	197.4660	209.5918	215.7309	204.4940
50 mA	QA0	552.3178	527.0917	550.5029	523.5245
	YQ0	496.8190	525.6536	542.5437	513.8161
100 mA	QA0	1124.7	1076.4	1126.3	1071.7
	YQ0	1018.4	1074.5	1110.8	1052.3

Table 5c Pre-Irradiation and Post-Annealing VOL (mV) at Various Sinking Current

Sourcing Current	Pin\DUT	11048 (40 krad)		11080 (40 krad)	
		Pre-rad	Post-an	Pre-rad	Post-an
1 mA	QA0	11.1891	10.6781	10.8605	11.5543
	YQ0	10.3137	10.6067	10.9080	11.6856
12 mA	QA0	127.3598	120.1033	122.8851	127.0812
	YQ0	118.1046	118.1290	124.2189	126.9641
20 mA	QA0	212.1136	199.9896	204.4784	210.6599
	YQ0	196.7623	196.7066	206.7705	210.8271
50 mA	QA0	533.2455	502.9662	514.2827	527.9991
	YQ0	495.3803	494.6134	520.7134	528.9843
100 mA	QA0	1091.5	1029.0	1053.6	1079.1
	YQ0	1015.6	1013.3	1067.4	1082.4

Table 6a Pre-Irradiation and Post-Annealing VOH (mV) at Various Sourcing Current

Sourcing Current	Pin\DUT	11170 (100 krad)		11255 (100 krad)	
		Pre-rad	Post-an	Pre-rad	Post-an
1 mA	QA0	4976.6	4972.5	4977.1	4954.4
	YQ0	4975.7	4971.2	4976.7	4954.1
8 mA	QA0	4841.7	4835.9	4841.1	4806.6
	YQ0	4841.1	4835.1	4845.7	4814.1
20 mA	QA0	4605.1	4598.4	4603.4	4551.7
	YQ0	4605.2	4596.7	4616.2	4570.9
50 mA	QA0	3970.4	3958.4	3966.5	3964.6
	YQ0	3971.3	3954.1	3999.8	3914.6
100 mA	QA0	2576.1	2521.9	2576.2	2304.9
	YQ0	2578.7	2513.6	2647.7	2411.4

Table 6b Pre-Irradiation and Post-Annealing VOH (mV) at Various Sourcing Current

Sourcing Current	Pin\DUT	11118 (60 krad)		11134 (60 krad)	
		Pre-rad	Post-an	Pre-rad	Post-an
1 mA	QA0	4976.9	4976.3	4976.4	4975.5
	YQ0	4976.6	4974.8	4975.5	4974.9
8 mA	QA0	4839.4	4840.2	4839.2	4841.6
	YQ0	4845.7	4839.3	4839.4	4842.3
20 mA	QA0	4601.7	4603.8	4599.0	4606.9
	YQ0	4616.3	4601.8	4600.5	4609.2
50 mA	QA0	3961.9	3967.8	3953.4	3974.4
	YQ0	3998.6	3963.0	3958.1	3981.0
100 mA	QA0	2562.9	2551.7	2522.9	2551.6
	YQ0	2623.2	2535.1	2530.5	2563.2

Table 6c Pre-Irradiation and Post-Annealing VOH (mV) at Various Sourcing Current

Sourcing Current	Pin\DUT	11048 (40 krad)		11080 (40 krad)	
		Pre-rad	Post-an	Pre-rad	Post-an
1 mA	QA0	4977.3	4975.3	4977.3	4976.7
	YQ0	4977.0	4974.8	4976.1	4975.5
8 mA	QA0	4842.9	4844.4	4844.4	4841.3
	YQ0	4847.0	4844.7	4842.6	4840.9
20 mA	QA0	4607.1	4615.1	4611.8	4605.6
	YQ0	4618.5	4615.4	4608.5	4605.0
50 mA	QA0	3974.8	3997.7	3985.1	3971.4
	YQ0	4004.1	3998.0	3979.2	3970.4
100 mA	QA0	2589.1	2626.5	2591.3	2558.7
	YQ0	2638.3	2616.6	2586.1	2563.2

E. Propagation Delay

Table 7 lists the pre-irradiation and post-annealing propagation delays, and also lists the radiation-induced degradations in percentage. The radiation delta in every case is well within the 10% degradation criterion. The user can take the worst case for the design-margin consideration.

Table 7 Radiation-Induced Propagation Delay Degradations

DUT	Total Dose	Pre-Irradiation (µs)	Post-Anneal (µs)	Degradation (%)
11170	100 krad	23.08	23.19	0.48%
11255	100 krad	23.07	23.26	0.82%
11118	60 krad	22.91	23.14	1.00%
11134	60 krad	23.07	23.68	2.64%
11048	40 krad	23.01	23.12	0.48%
11080	40 krad	22.9	23.69	3.45%

F. Transition Characteristics

Figure 9a to Figure 20b show the pre-irradiation and post-annealing transition edges. In each case, the radiation-induced transition-time degradation is insignificant.

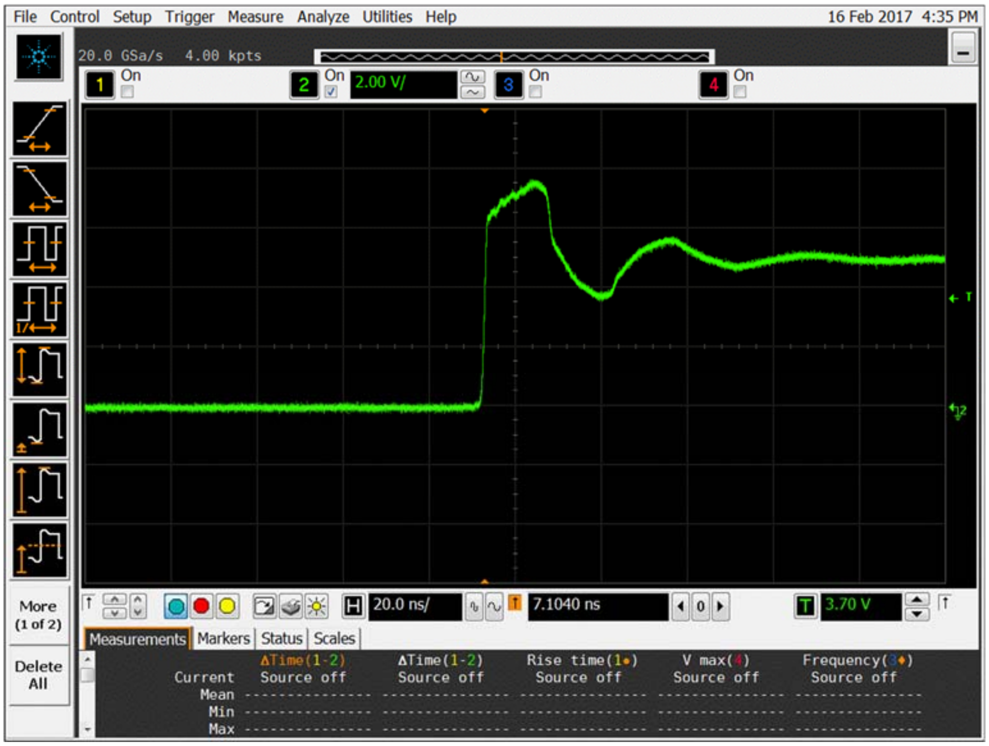

Figure 9a DUT 11170 Pre-Irradiation Rising Edge

Figure 9b DUT 11170 Post-Annealing Rising Edge

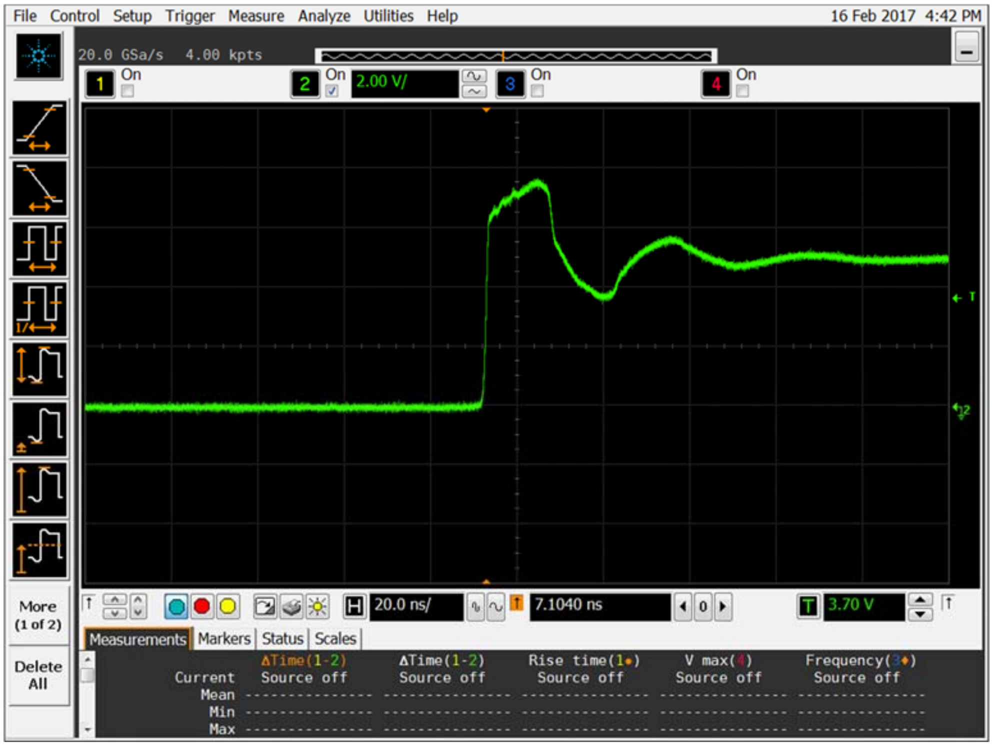

Figure 10a DUT 11255 Pre-Irradiation Rising Edge

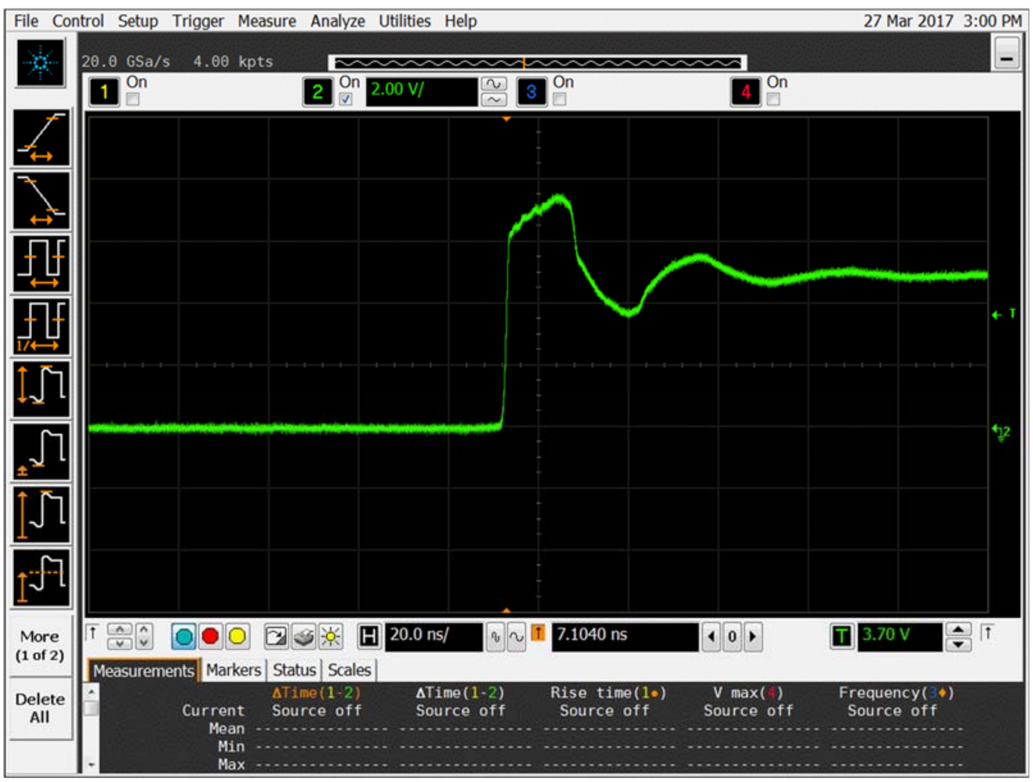

Figure 10b DUT 11255 Post-Annealing Rising Edge

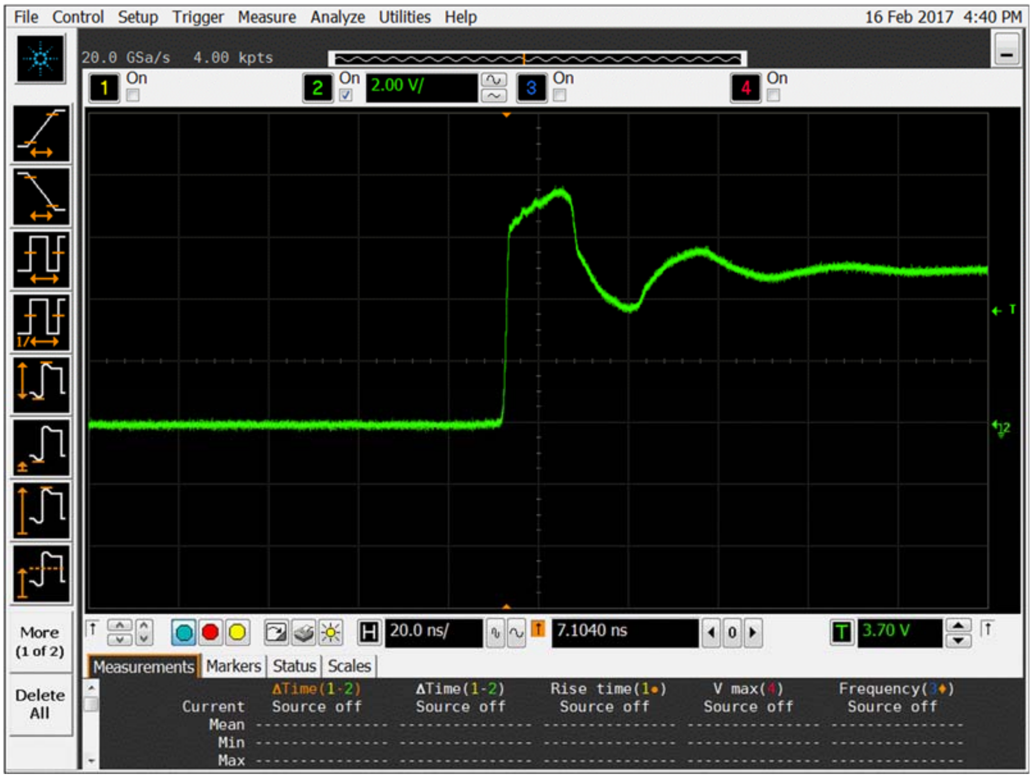

Figure 11a DUT 11118 Pre-Radiation Rising Edge

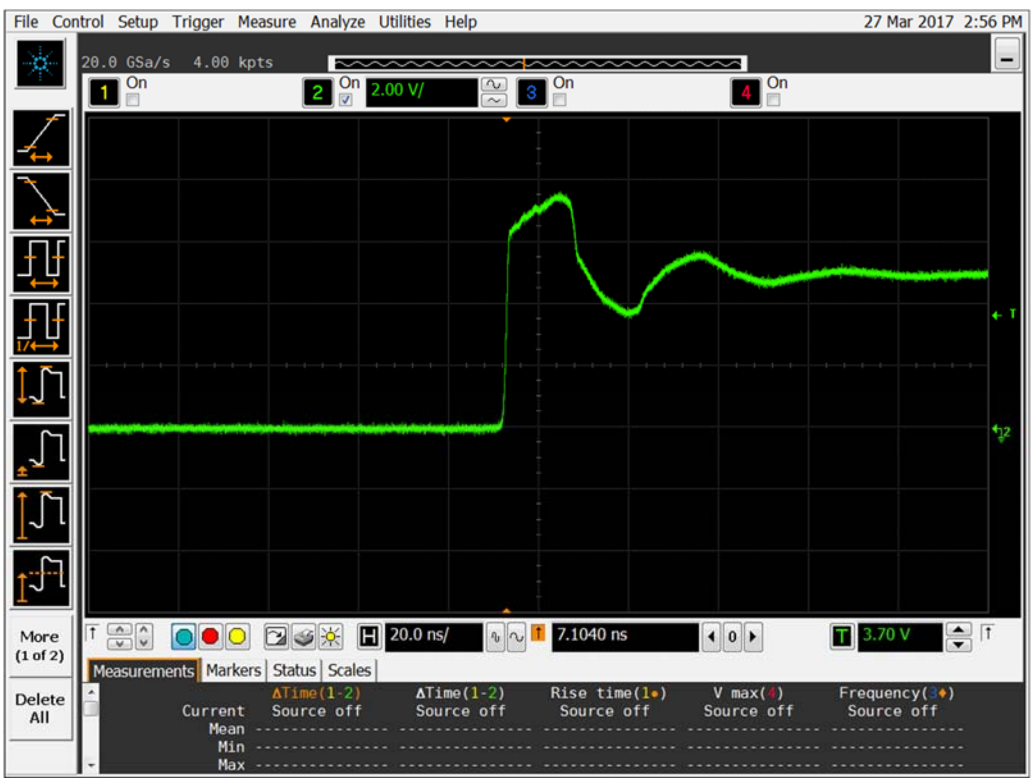

Figure 11b DUT 11118 Post-Annealing Rising edge

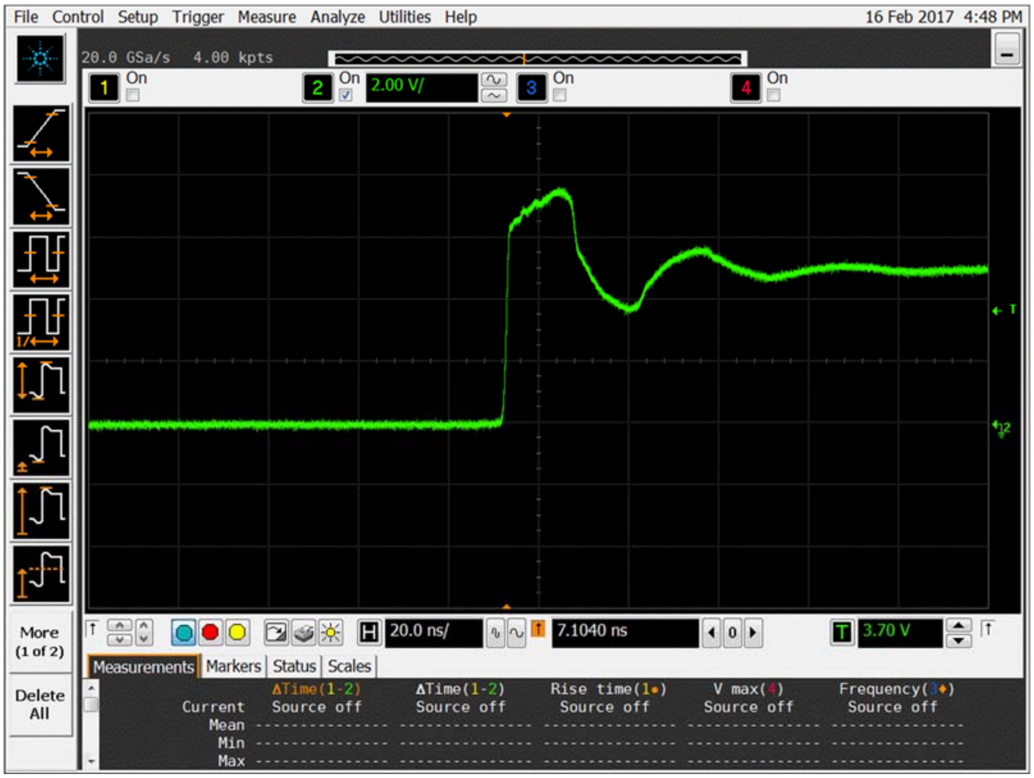

Figure 12a DUT 11134 Pre-Irradiation Rising Edge

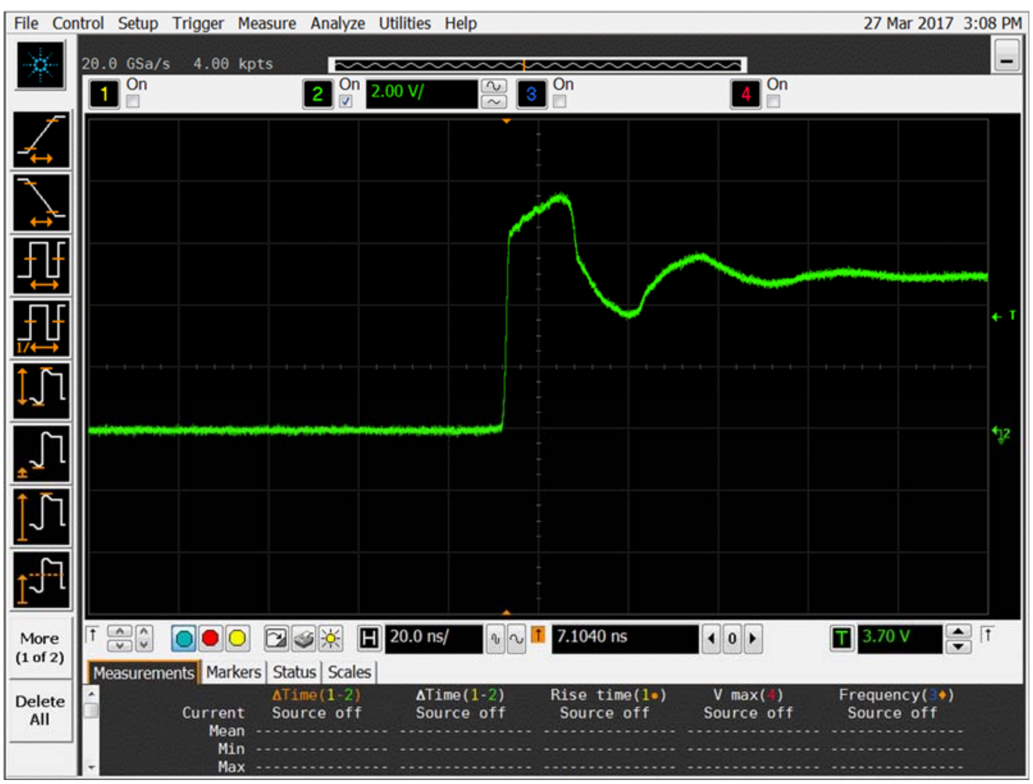

Figure 12b DUT 11134 Post-Annealing Rising Edge

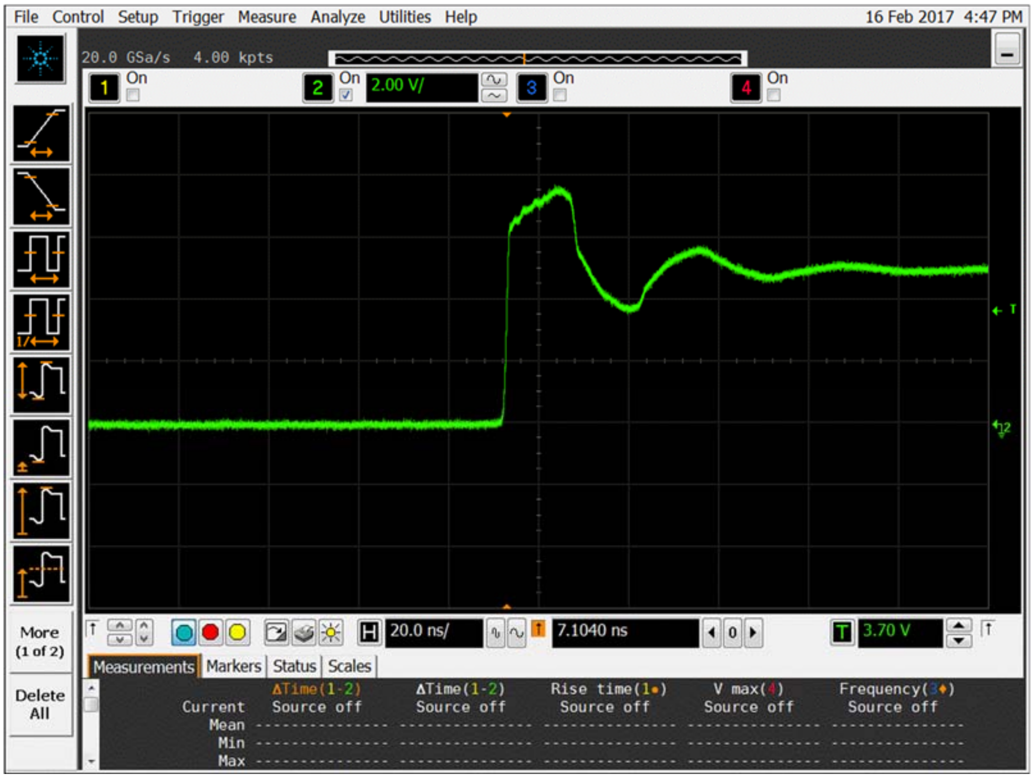

Figure 13a DUT 11048 Pre-Irradiation Rising Edge

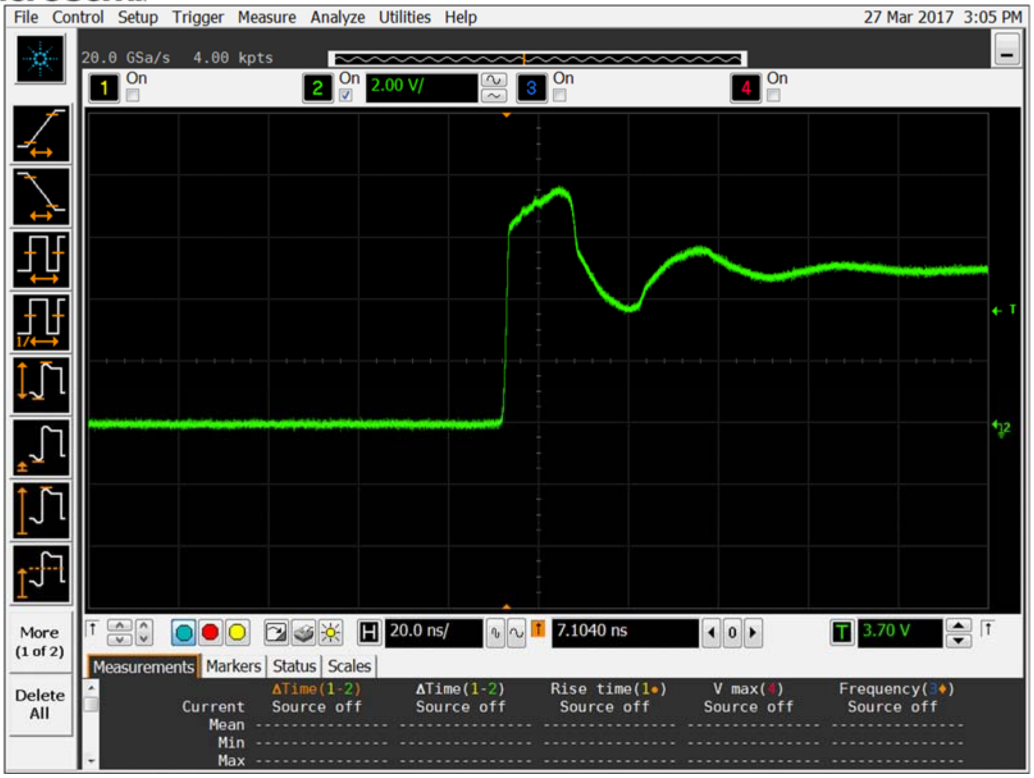

Figure 13b DUT 11048 Post-Annealing Rising Edge

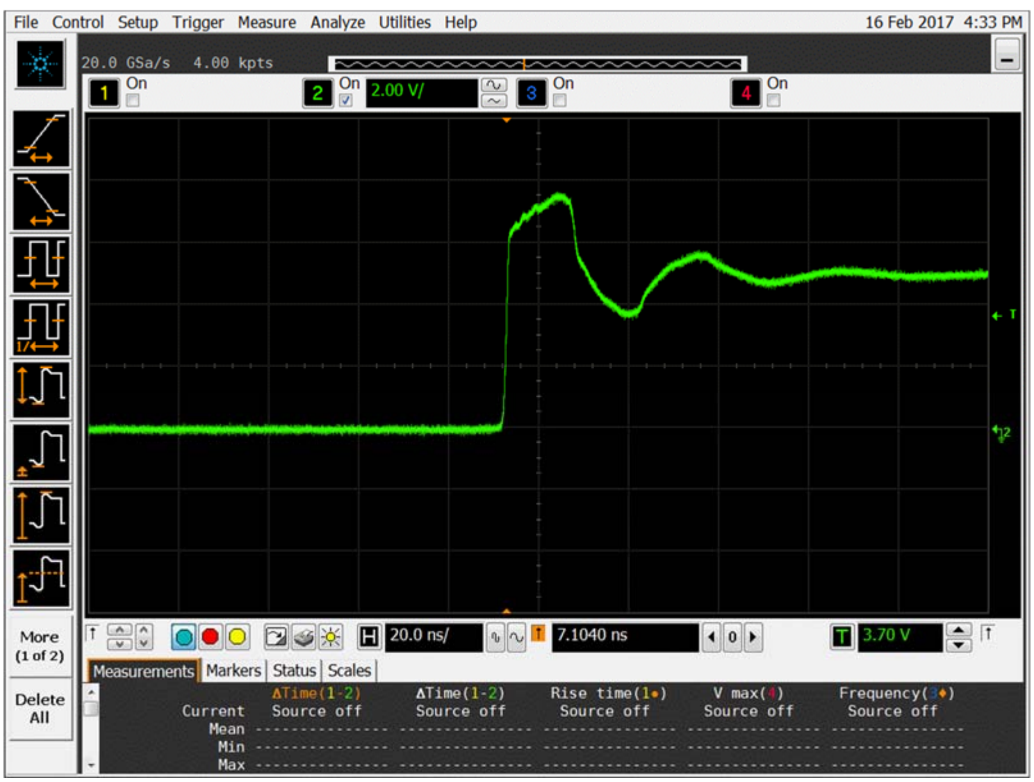

Figure 14a DUT 11080 Pre-Irradiation Rising Edge

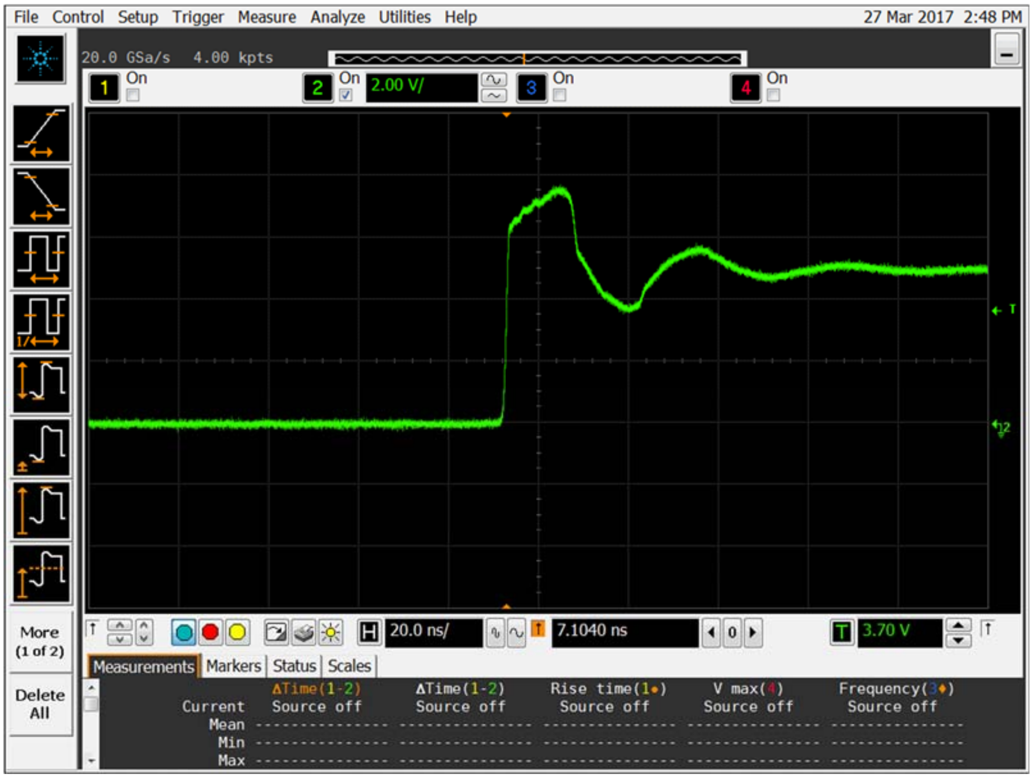

Figure 14b DUT 11080 Post-Annealing Rising Edge

Figure 15a DUT 11170 Pre-Radiation Falling Edge

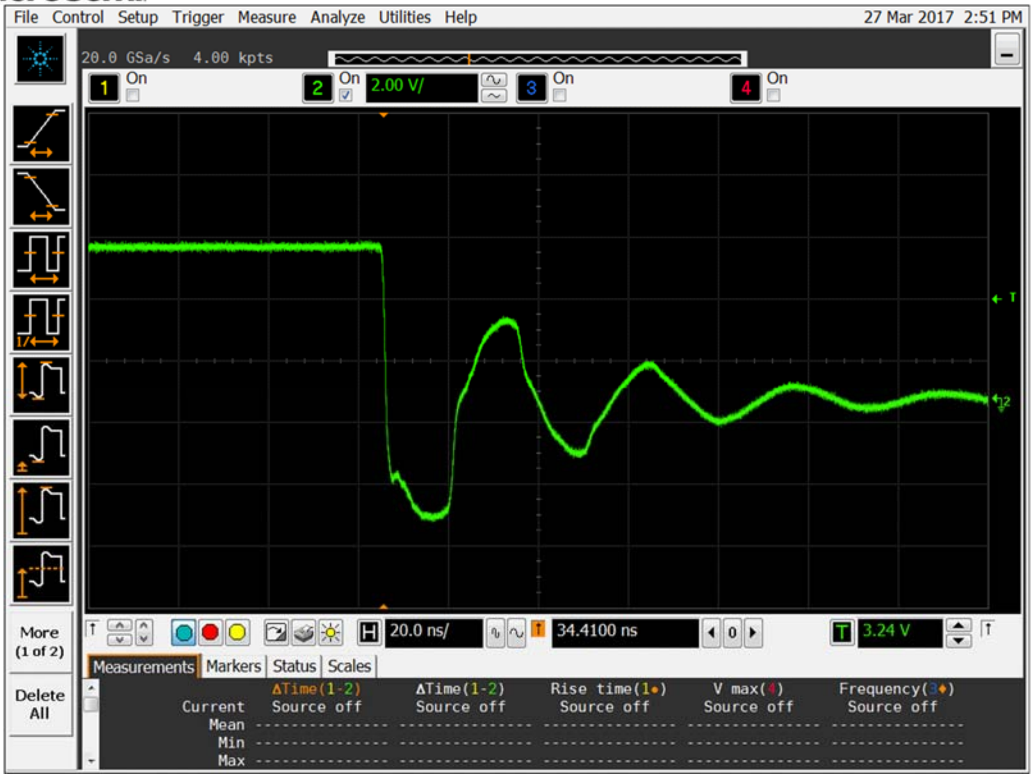

Figure 15b DUT 11170 Post-Annealing Falling Edge

Figure 16a DUT 11255 Pre-Irradiation Falling Edge

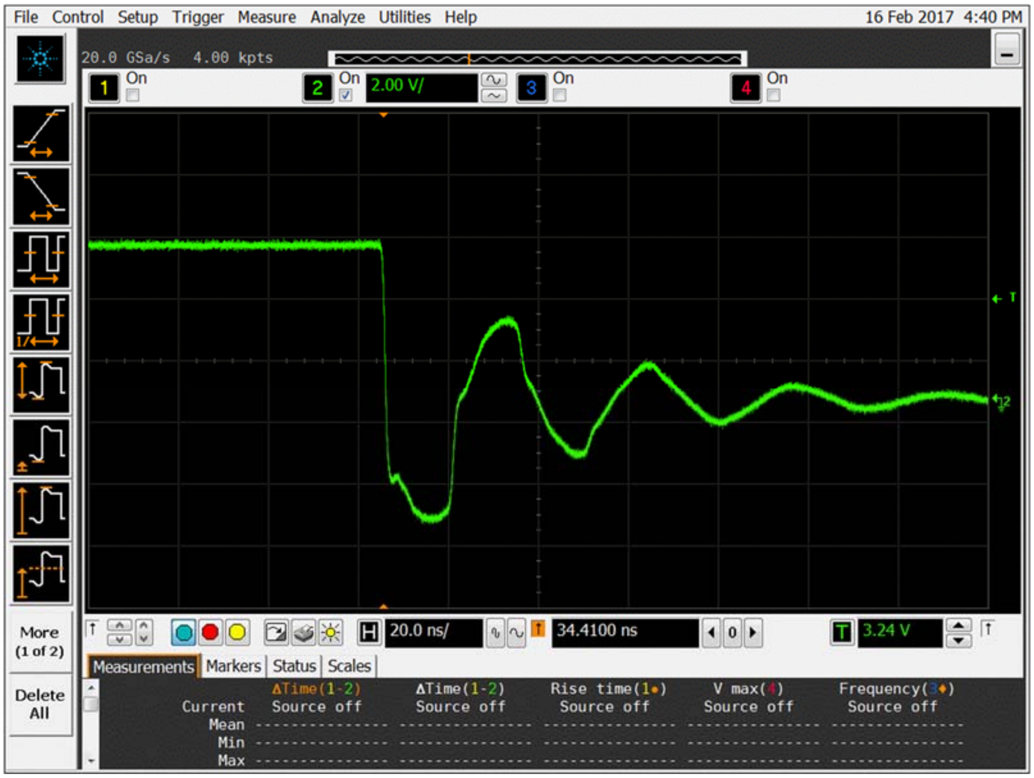

Figure 16b DUT 11255 Post-Annealing Falling Edge

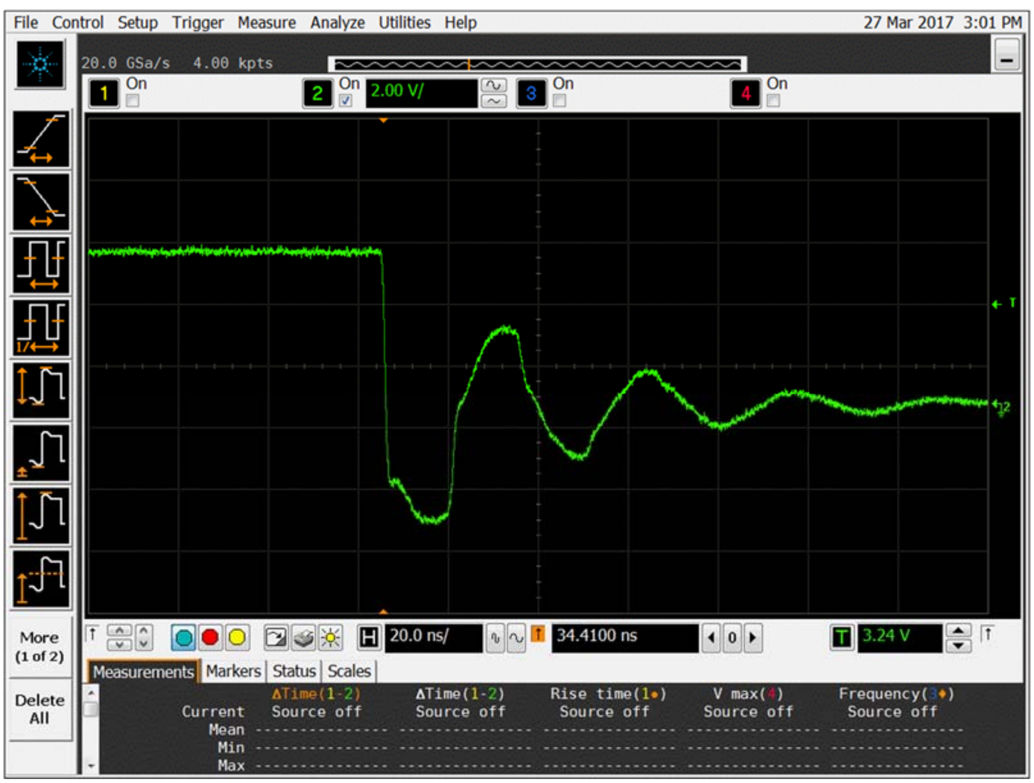

Figure 17a DUT 11118 Pre-Irradiation Falling Edge

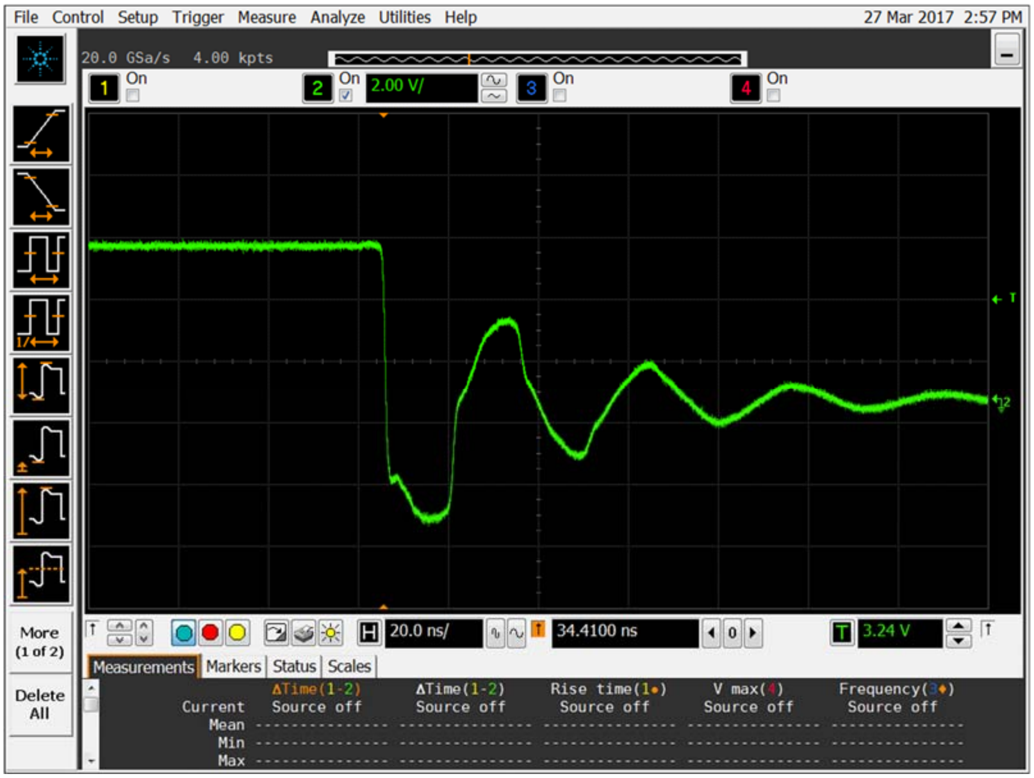

Figure 17b DUT 11118 Post-Annealing Falling Edge

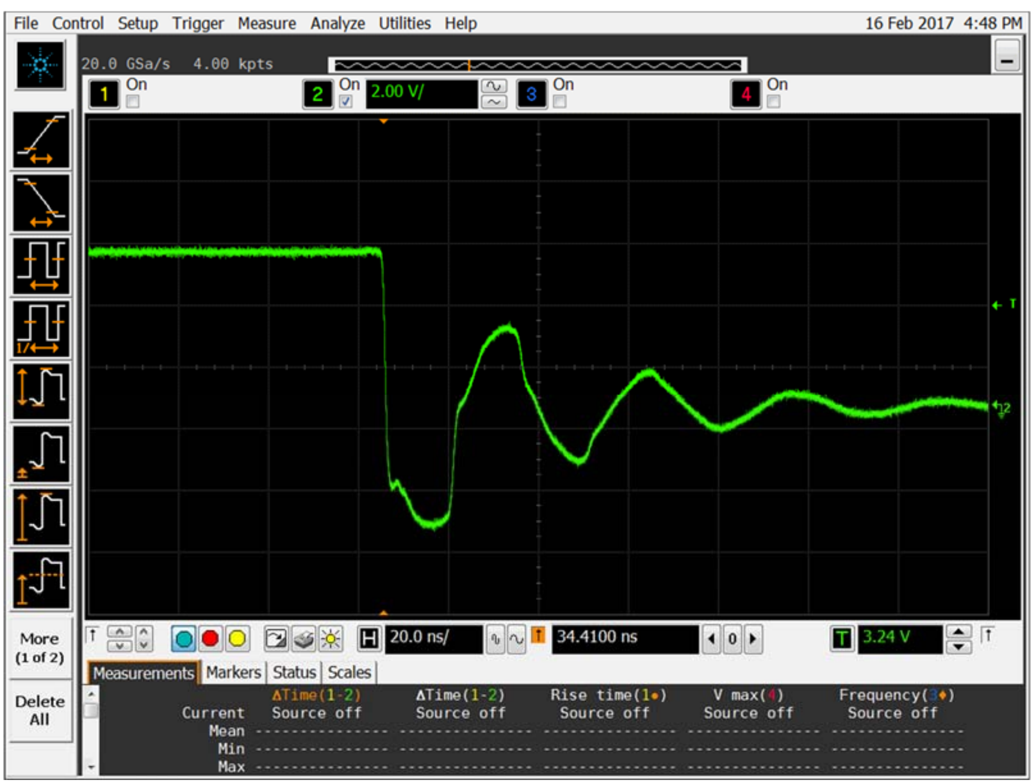

Figure 18a DUT 11134 Pre-Irradiation Falling Edge

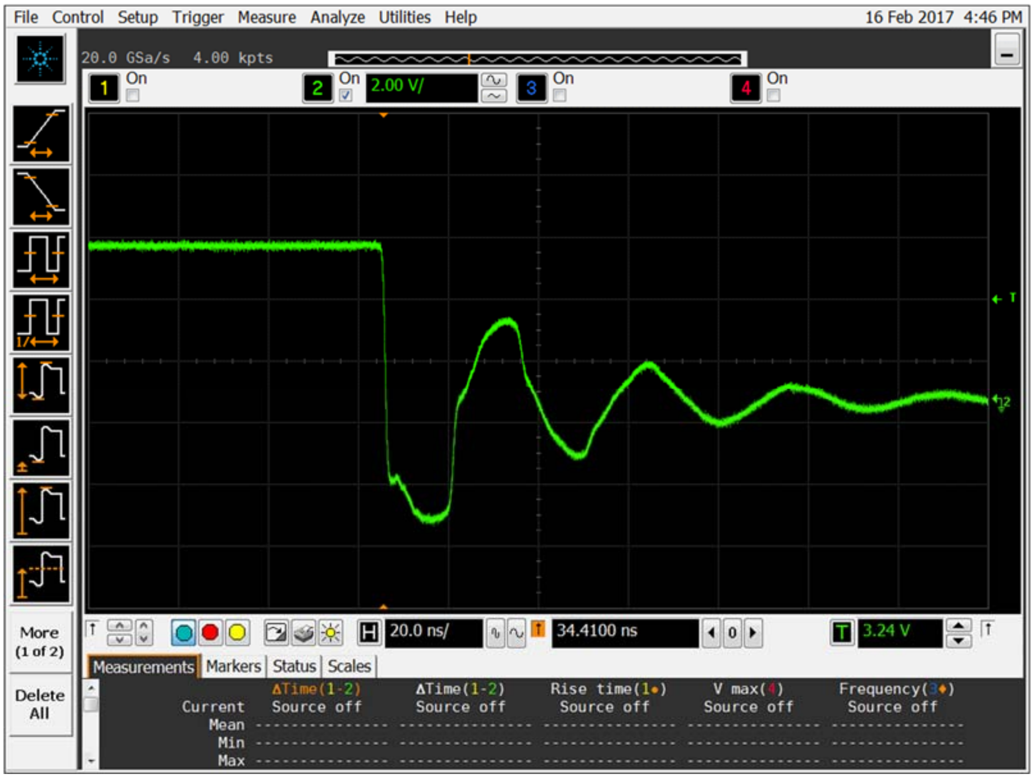

Figure 18b DUT 11134 Post-Annealing Falling Edge

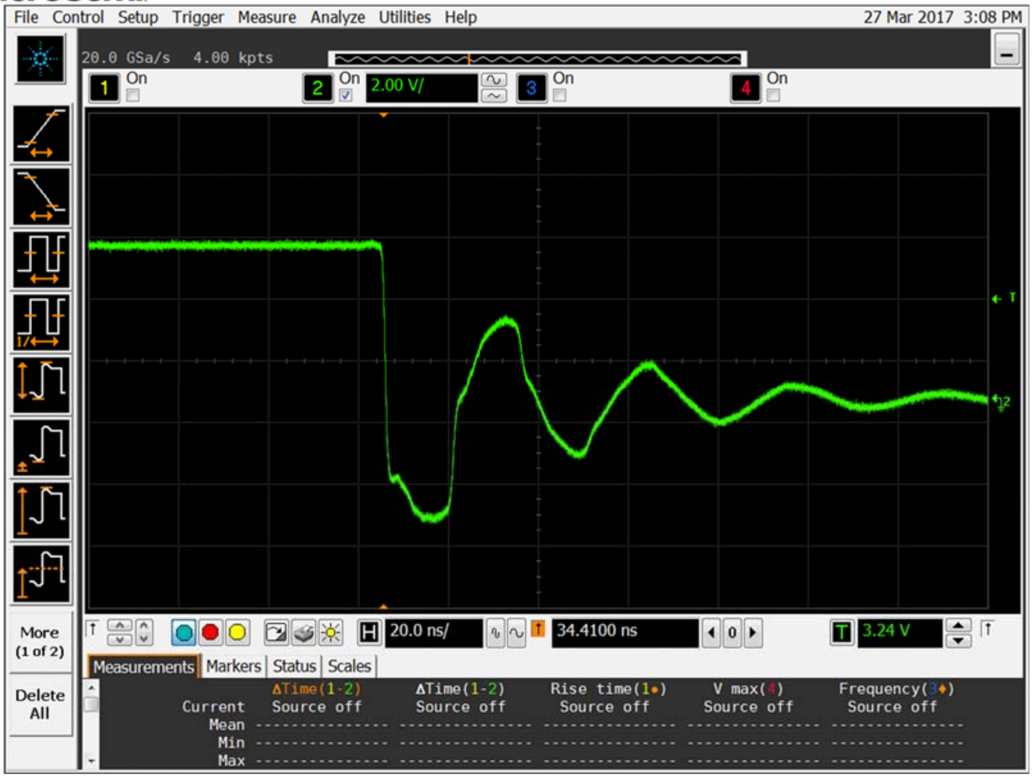

Figure 19a DUT 11048 Pre-Irradiation Falling Edge

Figure 19b DUT 11048 Post-Annealing Falling Edge

Figure 20a DUT 11080 Pre-Irradiation Falling Edge

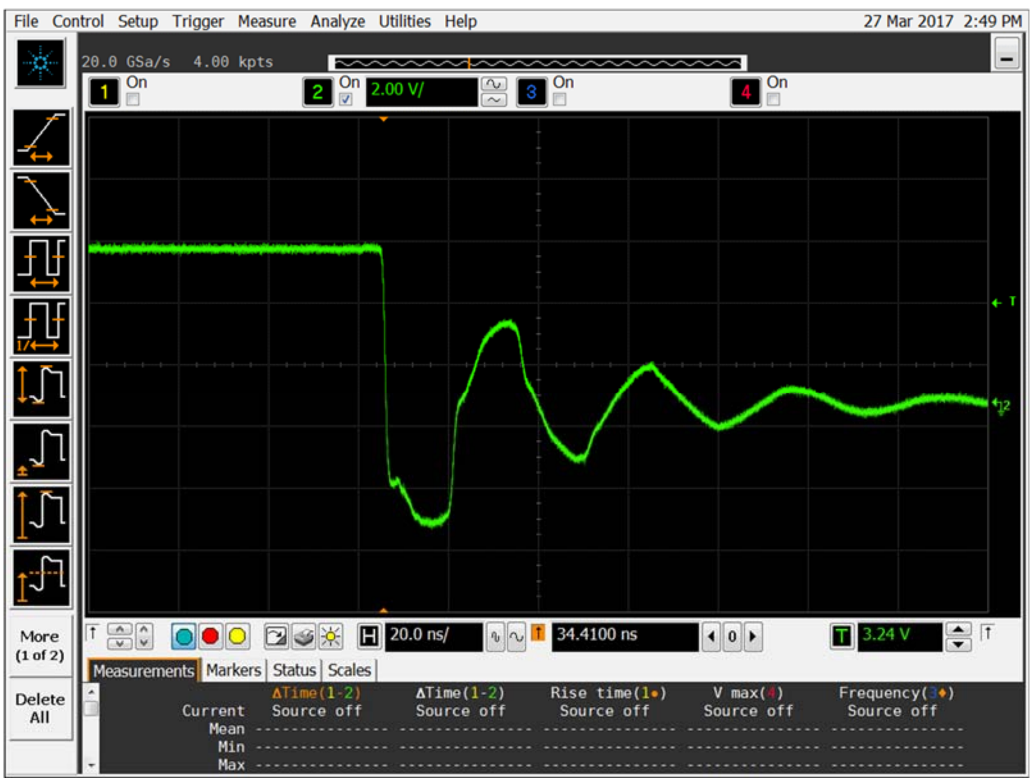

Figure 20b DUT 11080 Post-Annealing Falling Edge

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Appendix A: DUT Bias

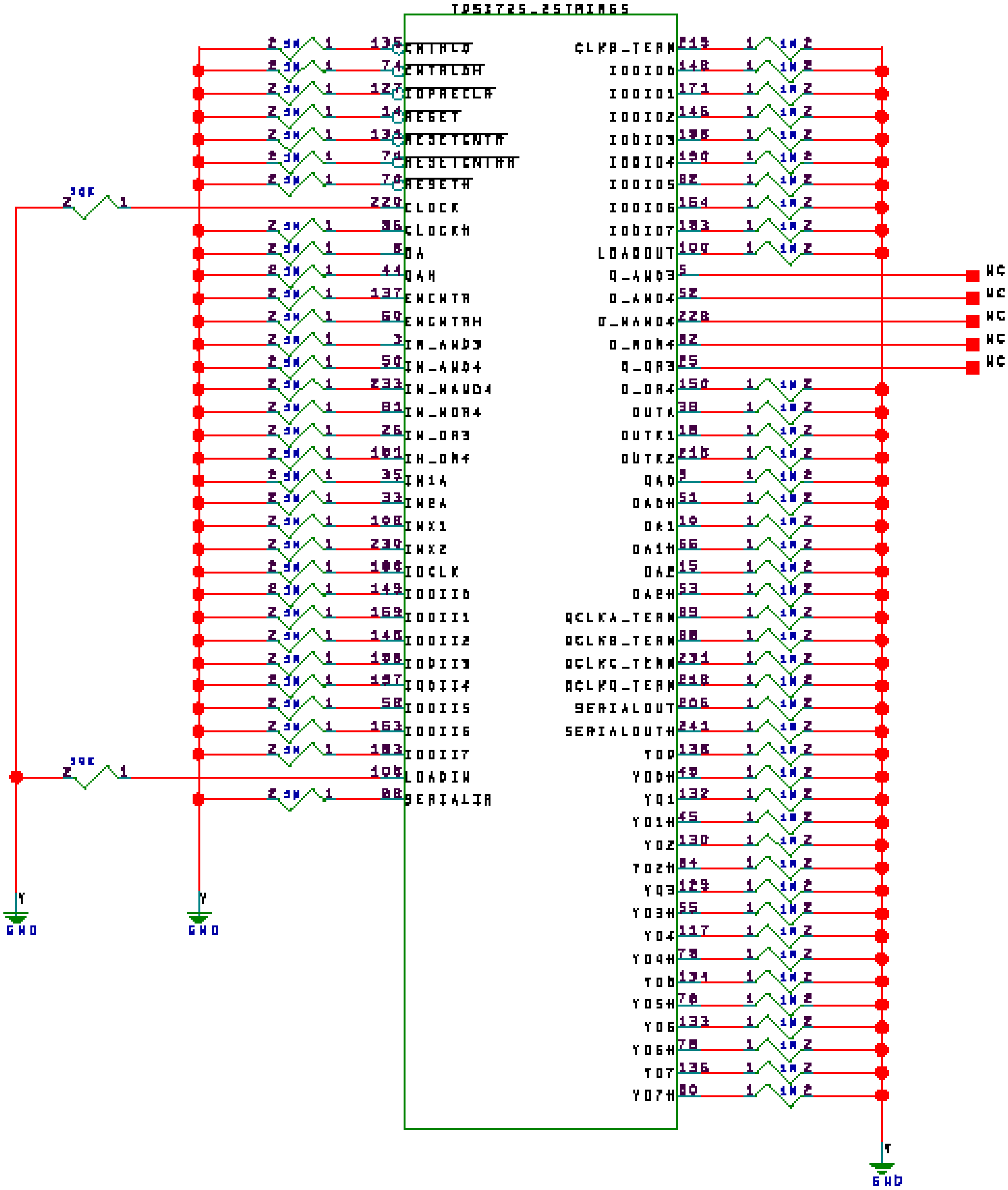

Figure A1 I/O Bias During Irradiation

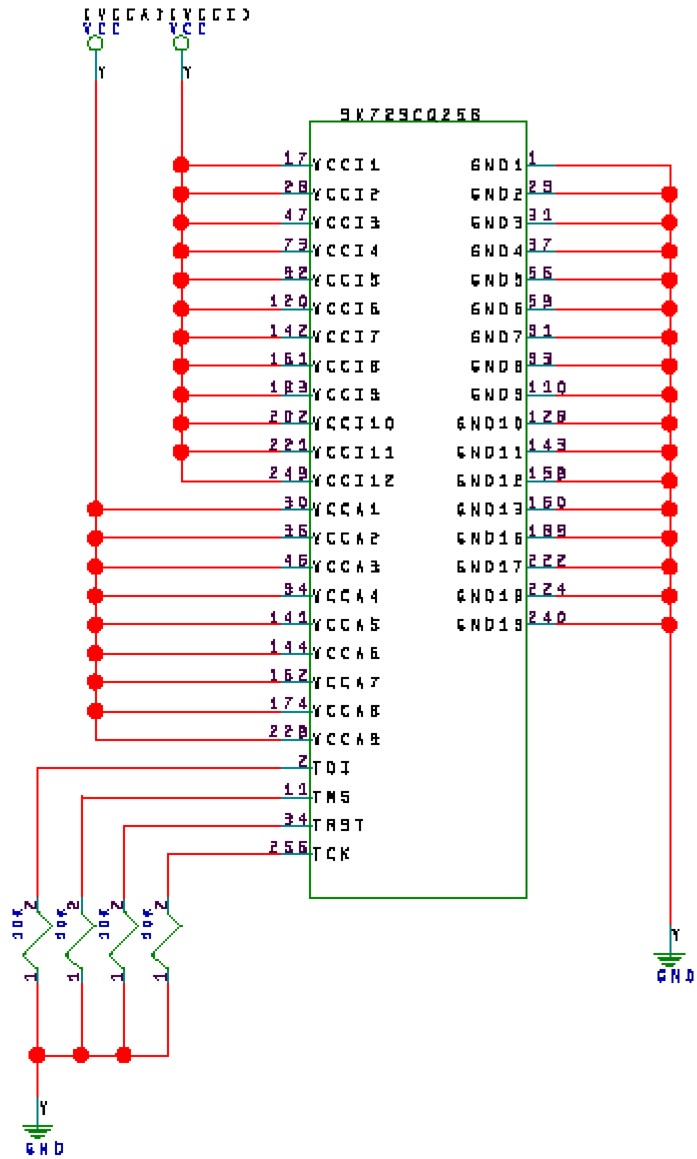

Figure A2 Power Supply, Ground and Special Pins Bias During Irradiation

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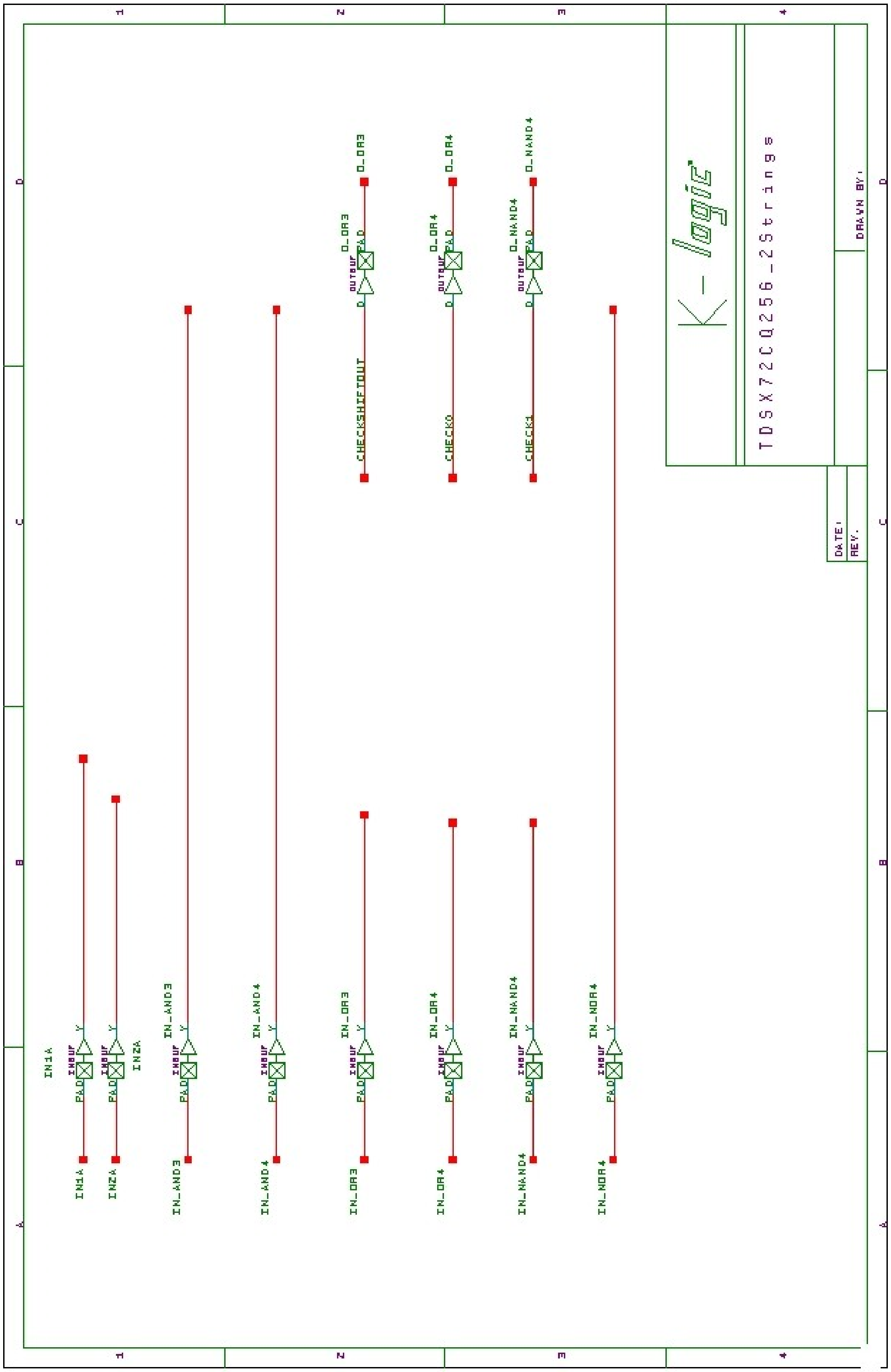
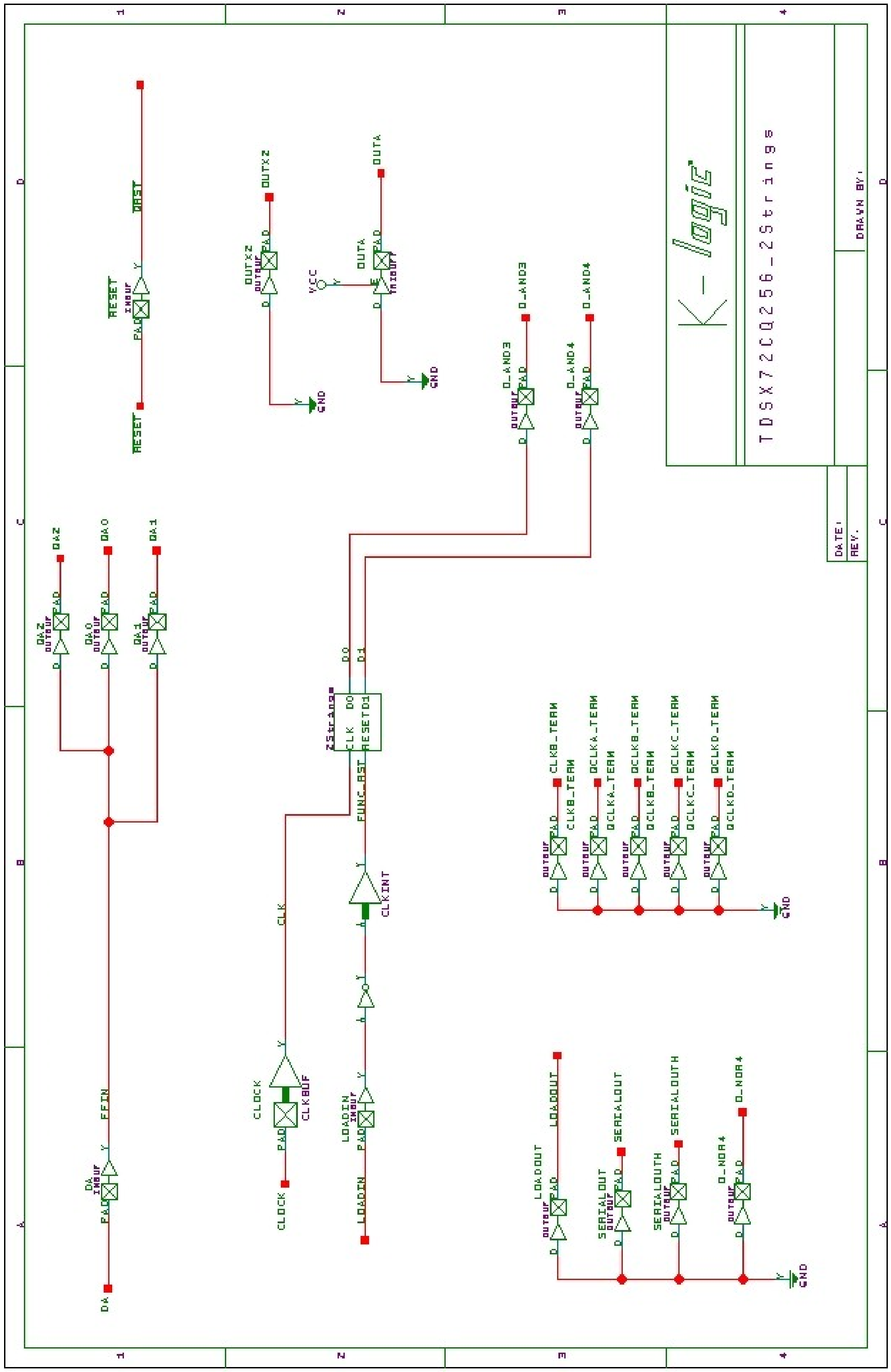
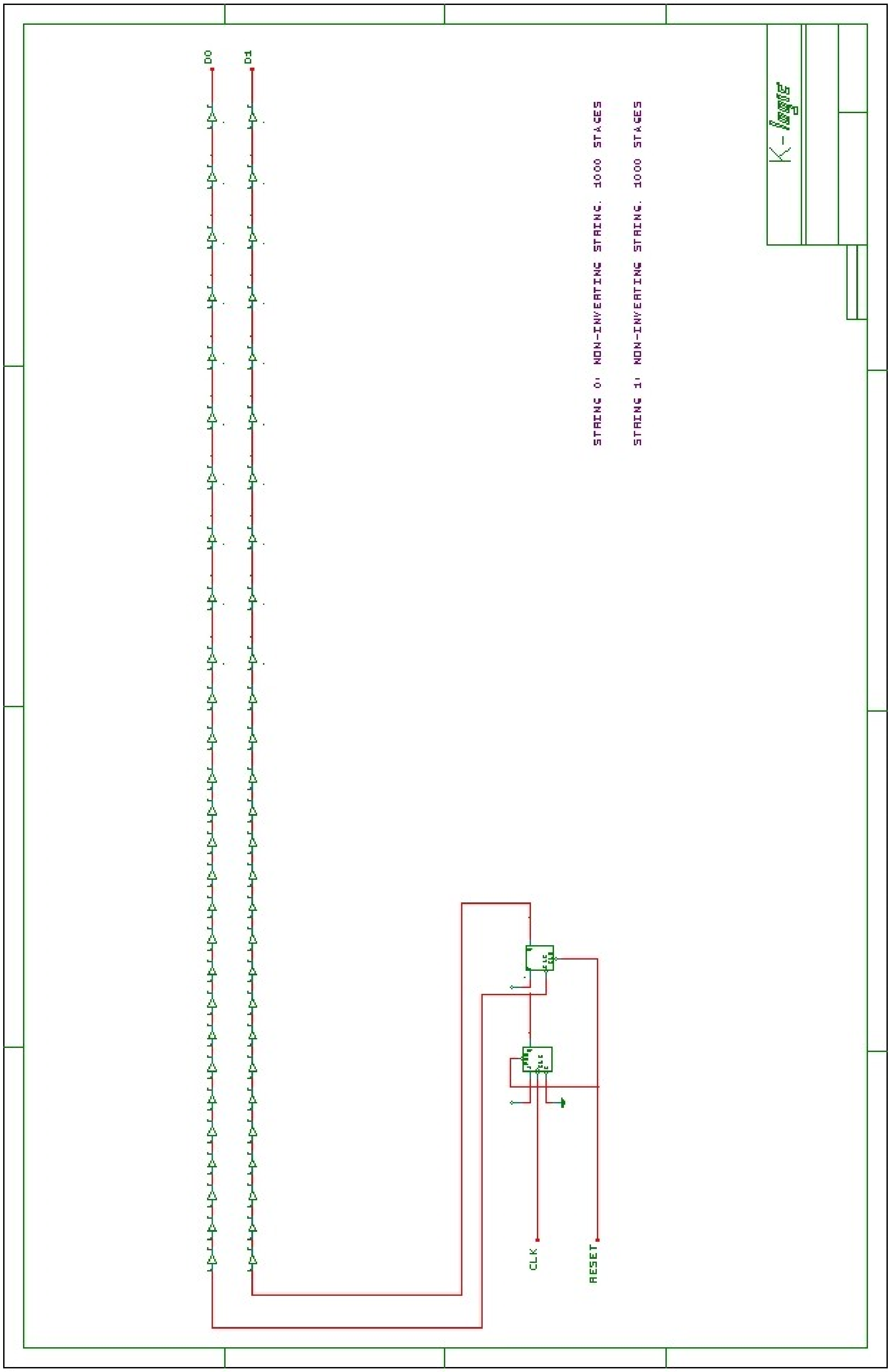
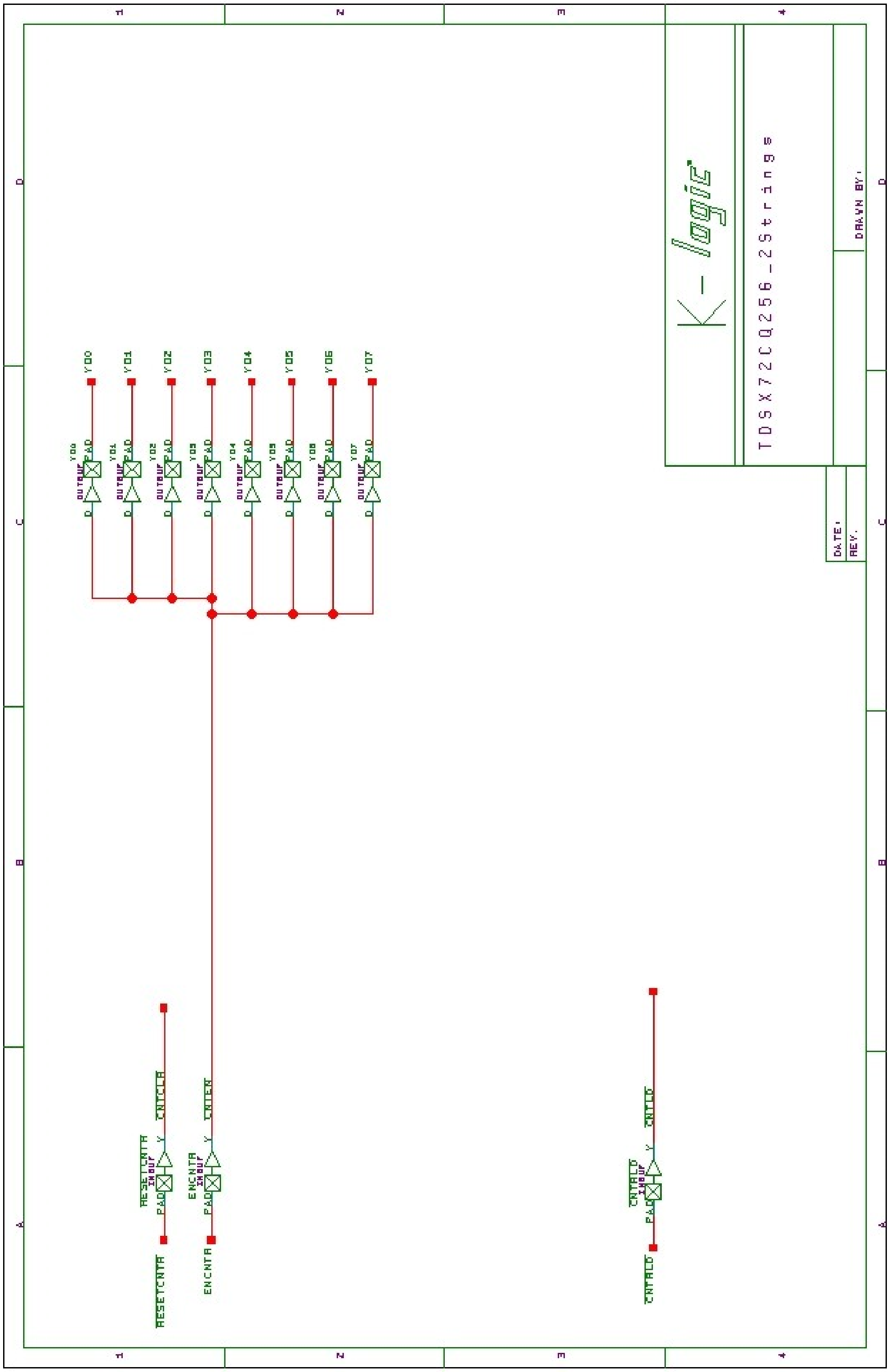
Appendix B: DUT Design Schematics

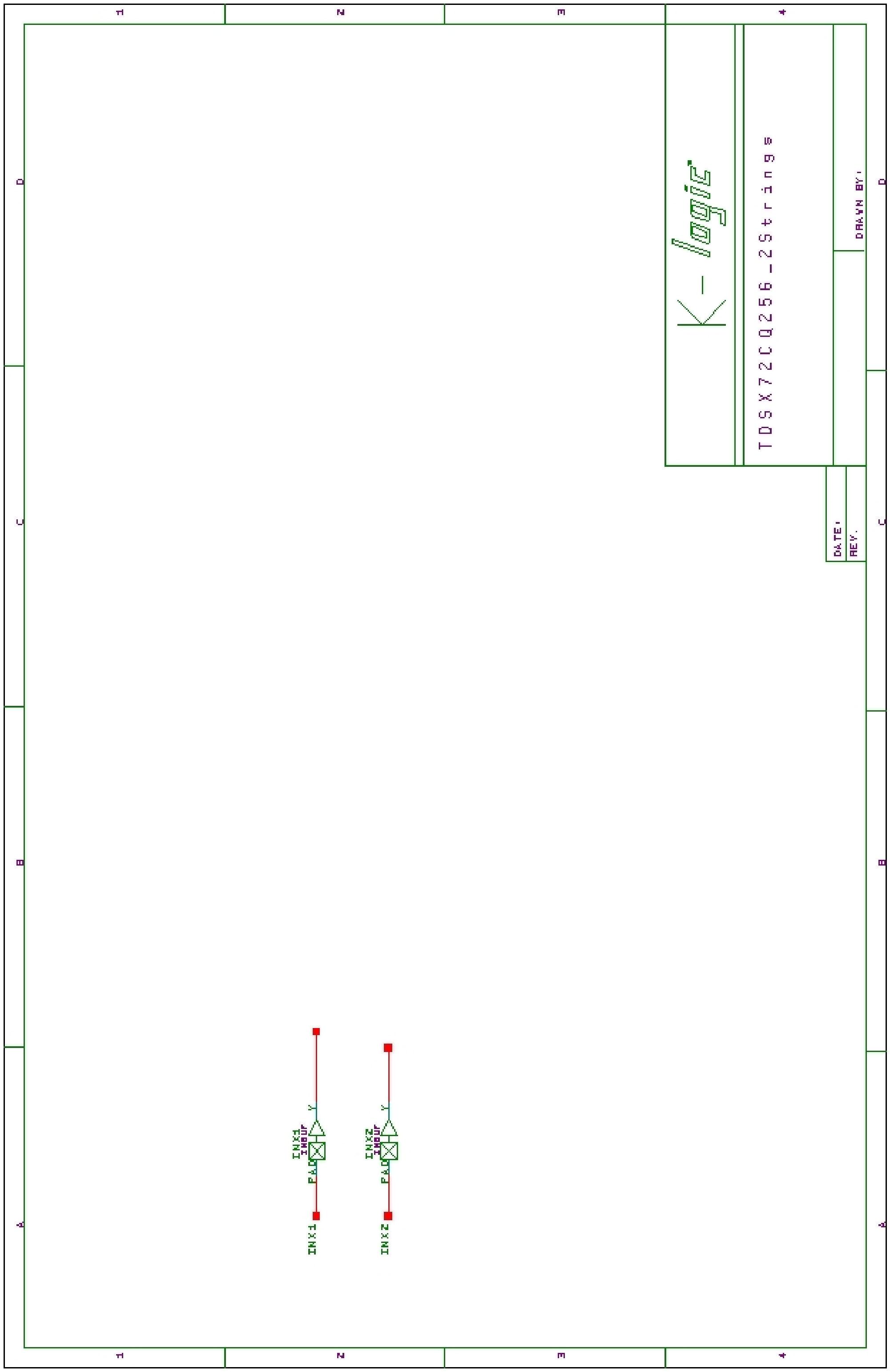


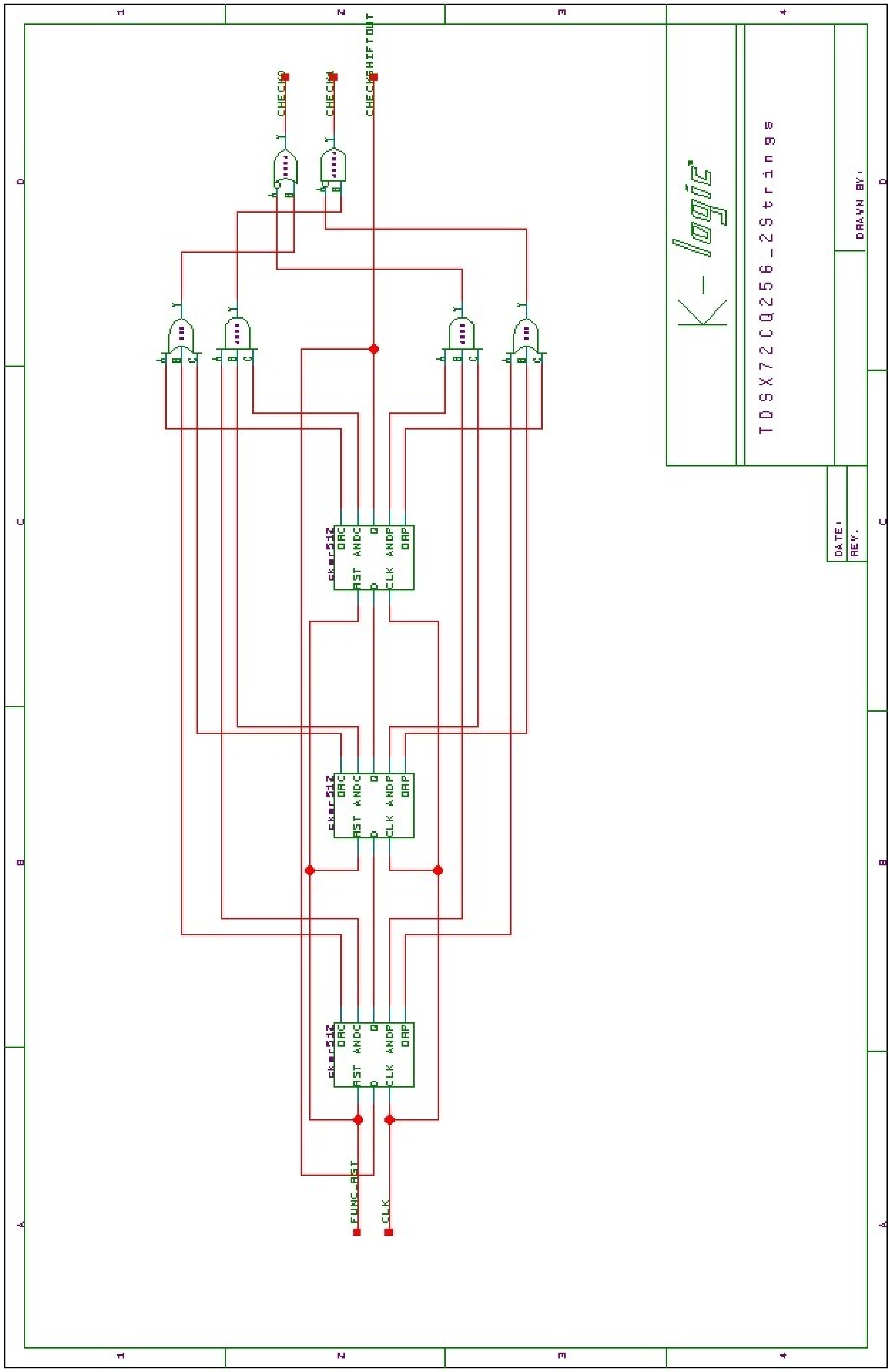

TDSX72CQ256_25strings
K-logic
DRAWN BY:
DATE:
REV.

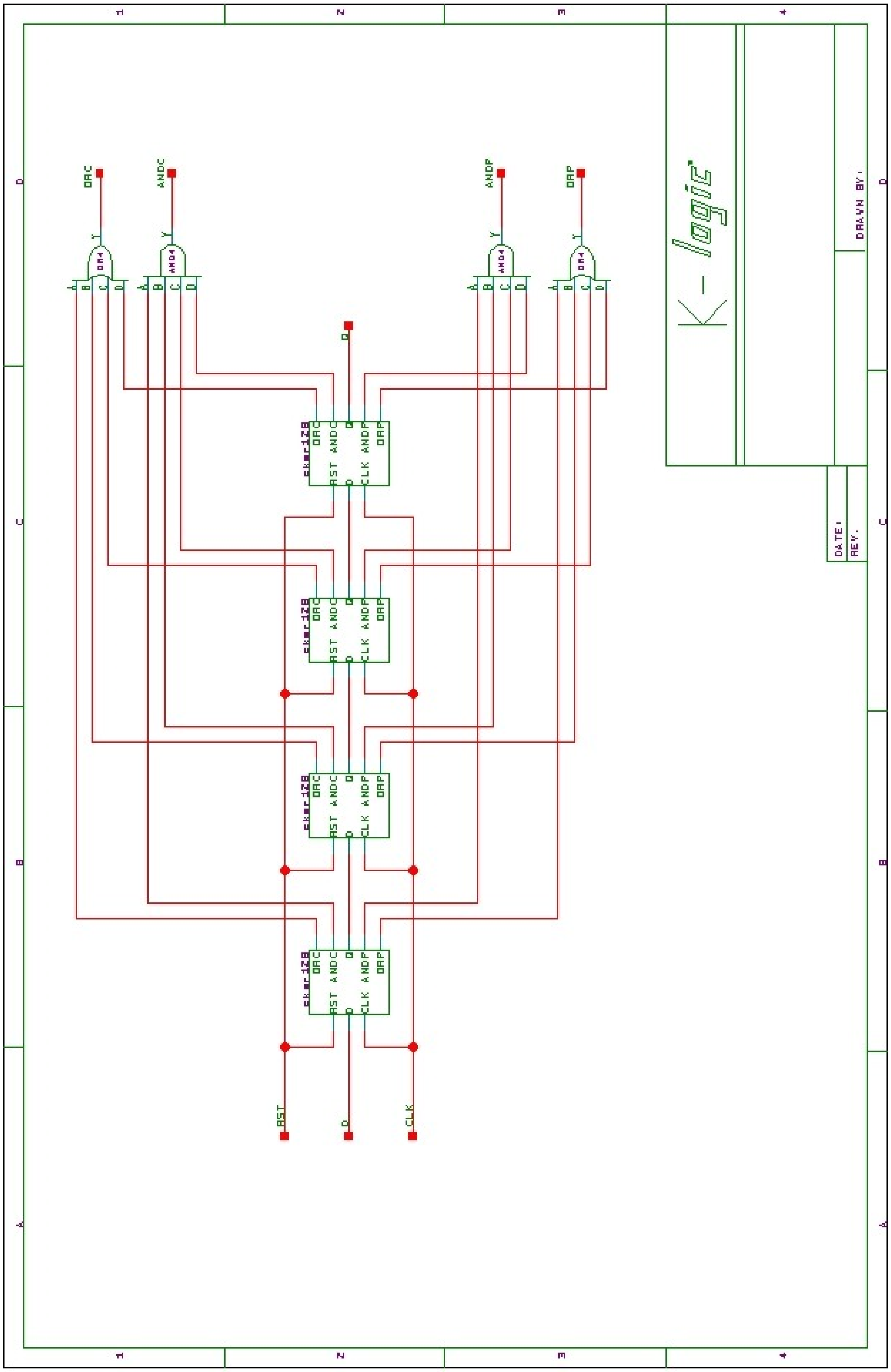

D0
D1
STRING 0: NON-INVERTING STRING, 1000 STAGES
STRING 1: NON-INVERTING STRING, 1000 STAGES
CLK
RESET


K-logic
TDACT3SXCQ\BUF50NINV
DRAWN BY: ABK
DATE:
REV.

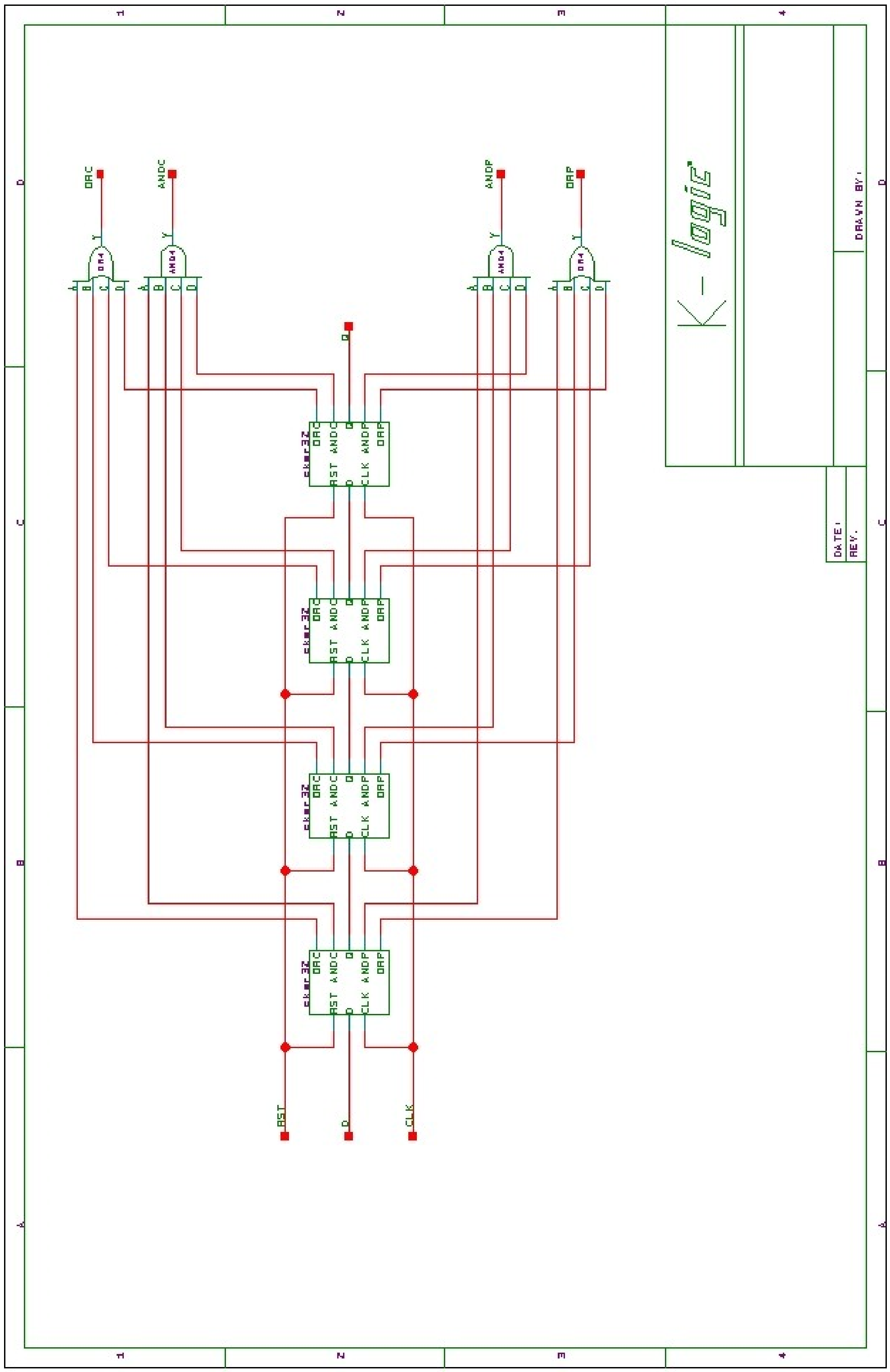

TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
Y00
Y01
Y02
Y03
Y04
Y05
Y06
Y07
RESETCNTA
ENCNTA
CNTALD
CNTCLR
CNTEN
CNTLD

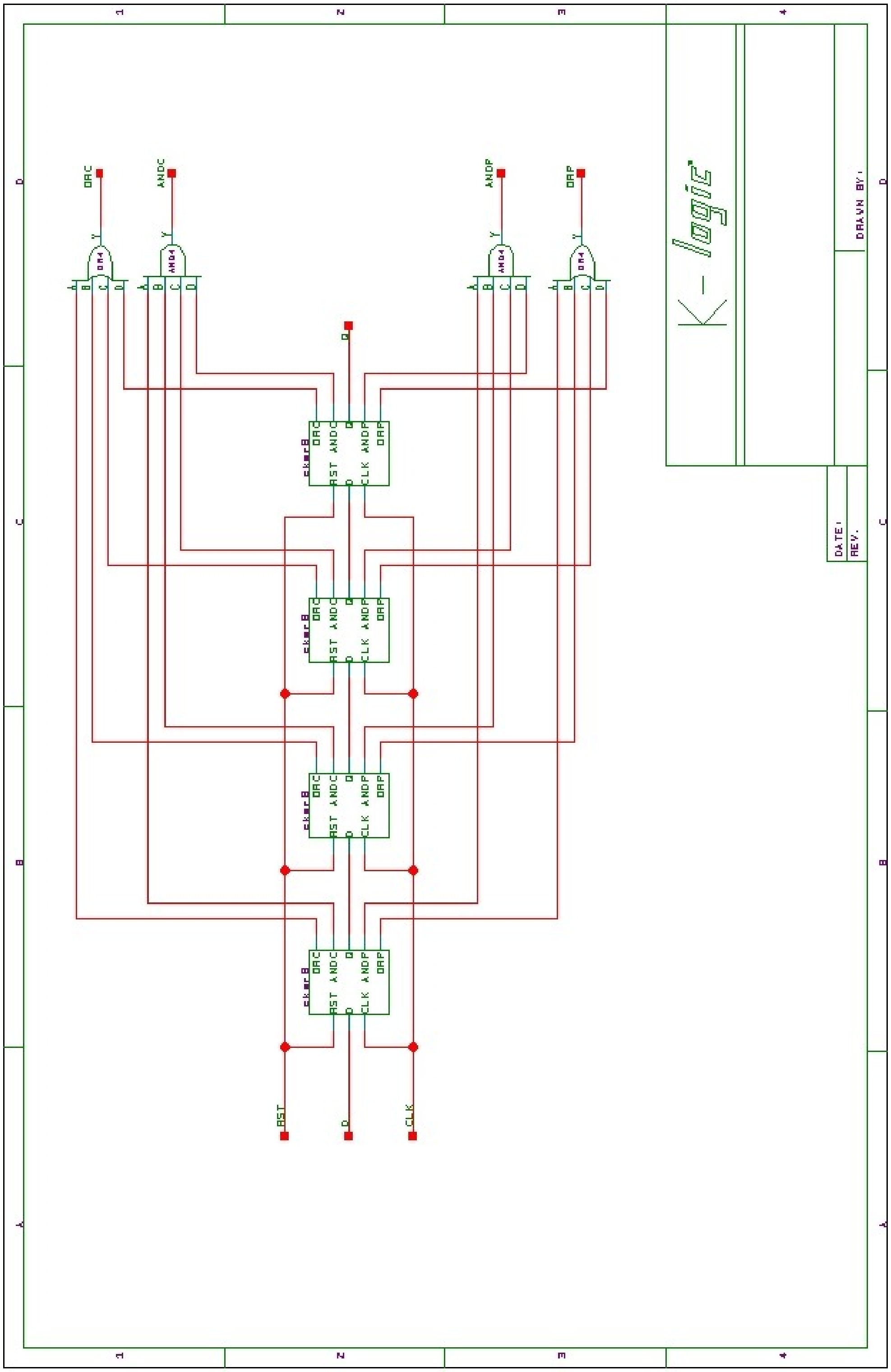

TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
INX1
INX2
INBUF
Y

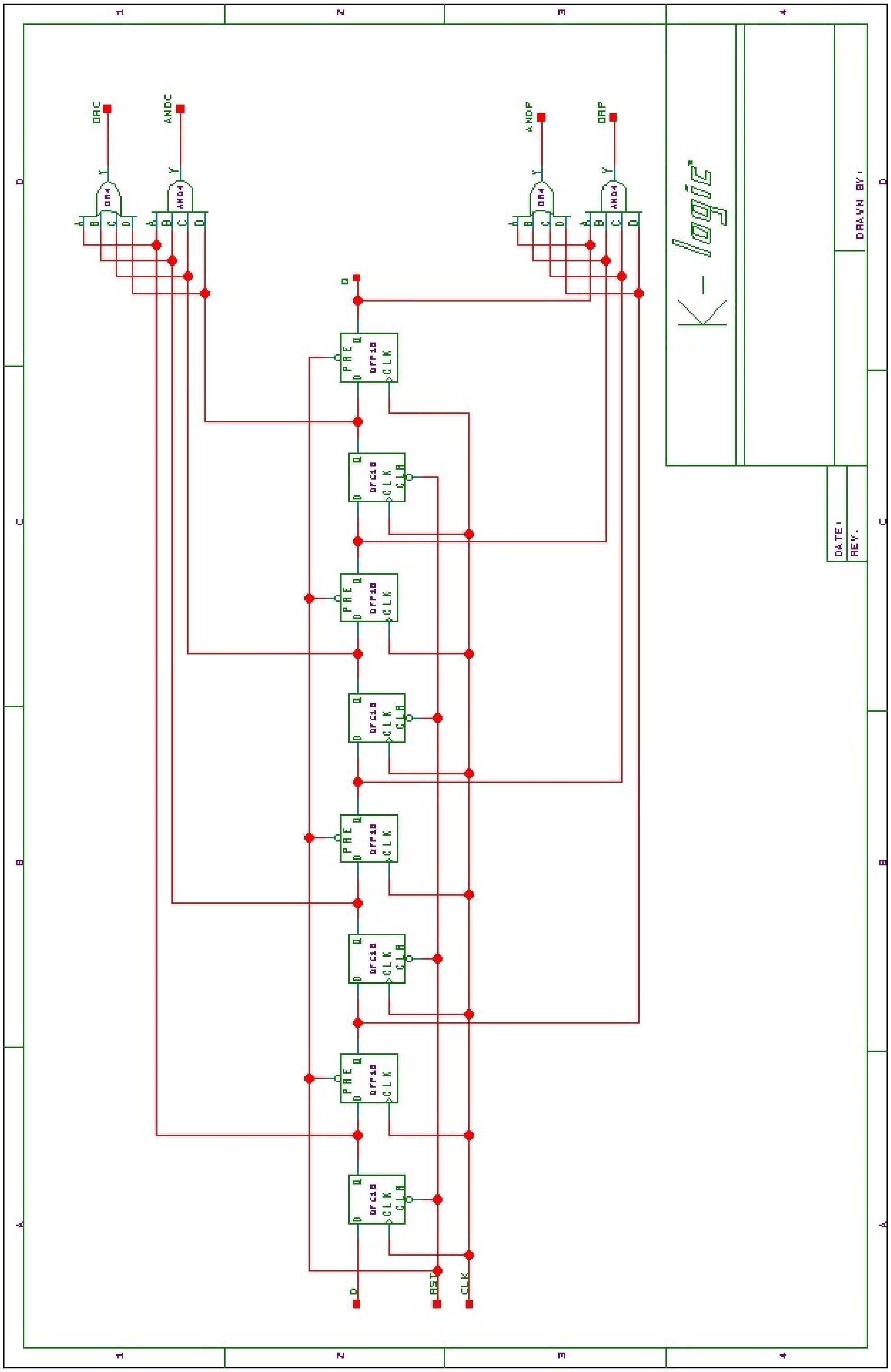

CHECK0
CHECK1
CHECKSHIFTOUT
FUNC_RST
CLK
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.

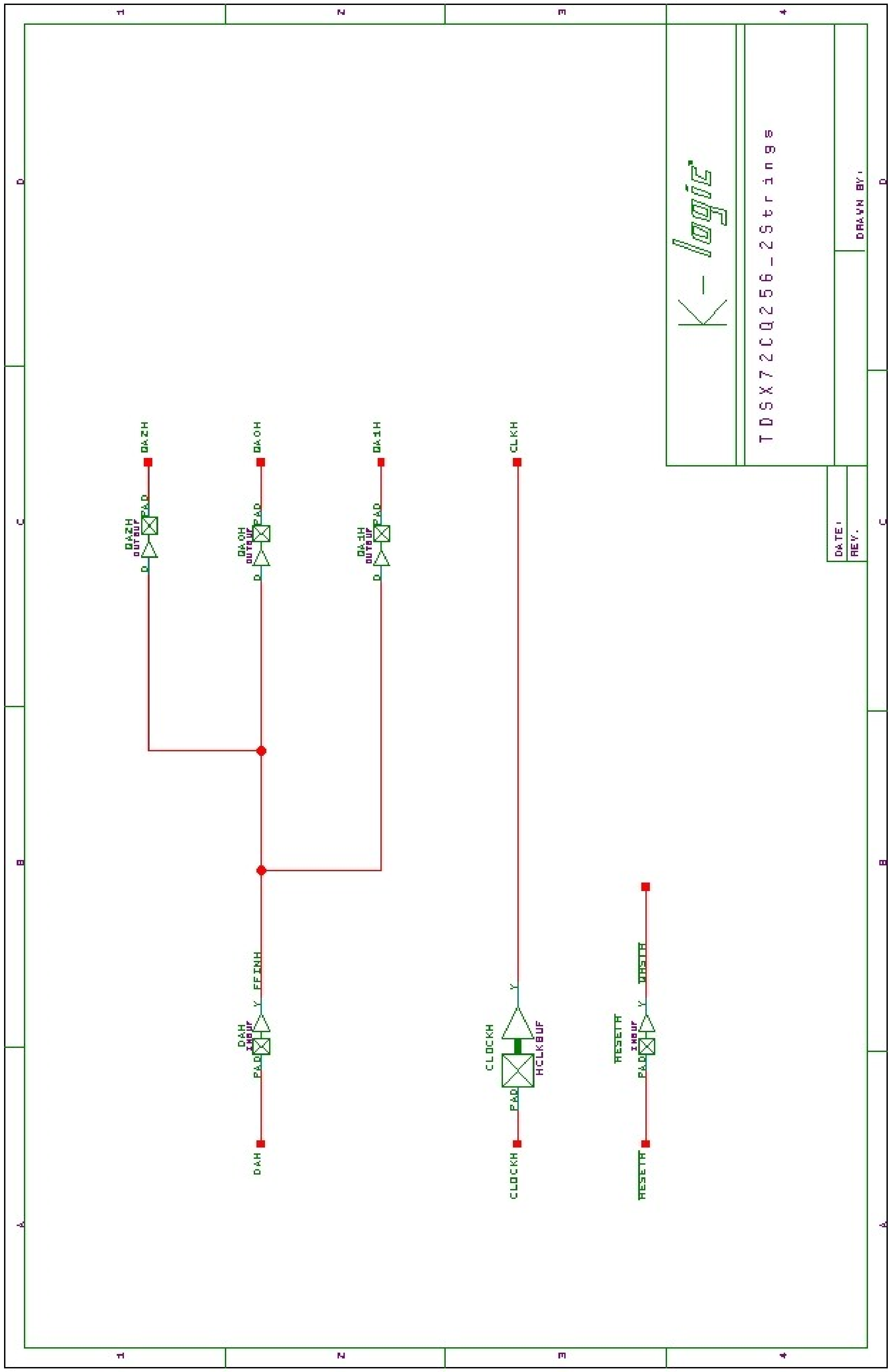


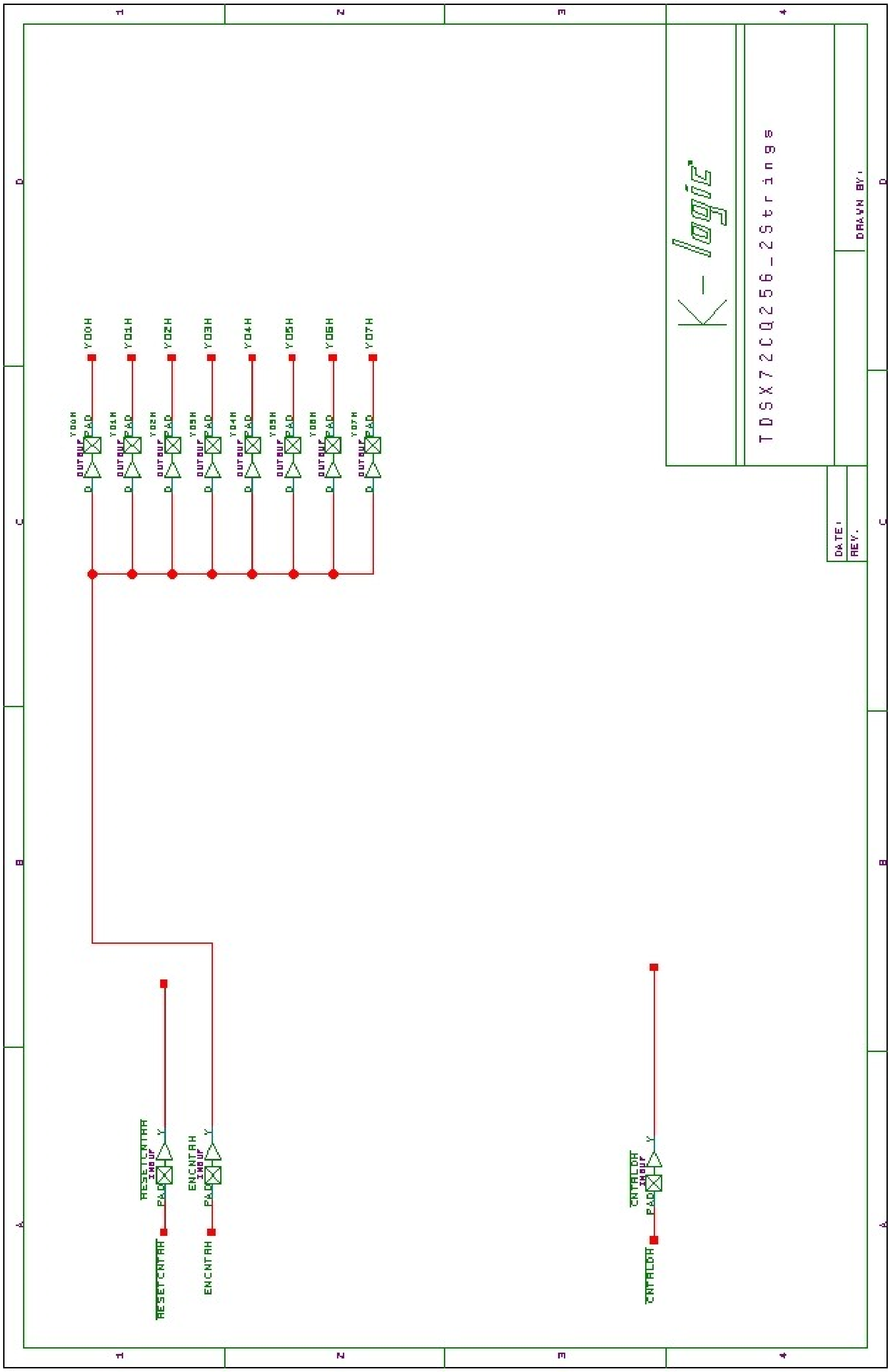
ORC
ANDC
ANDP
ORP
Q
ckmr128
RST
D
CLK
K-logic
DRAWN BY:
DATE:
REV.

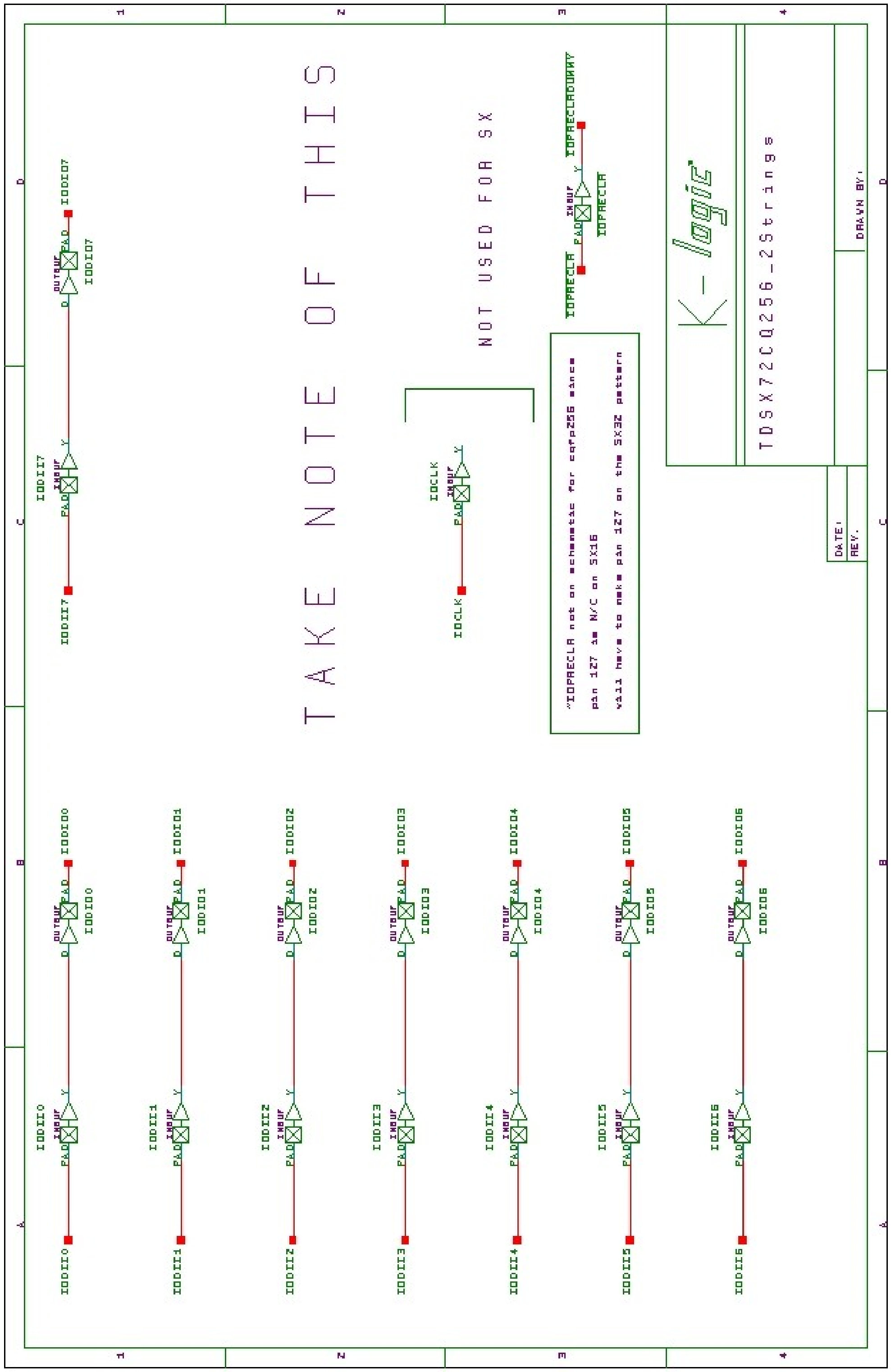

ORC
ANDC
ANDP
ORP
Q
ckmr32
RST
D
CLK
K-logic
DRAWN BY:
DATE:
REV.

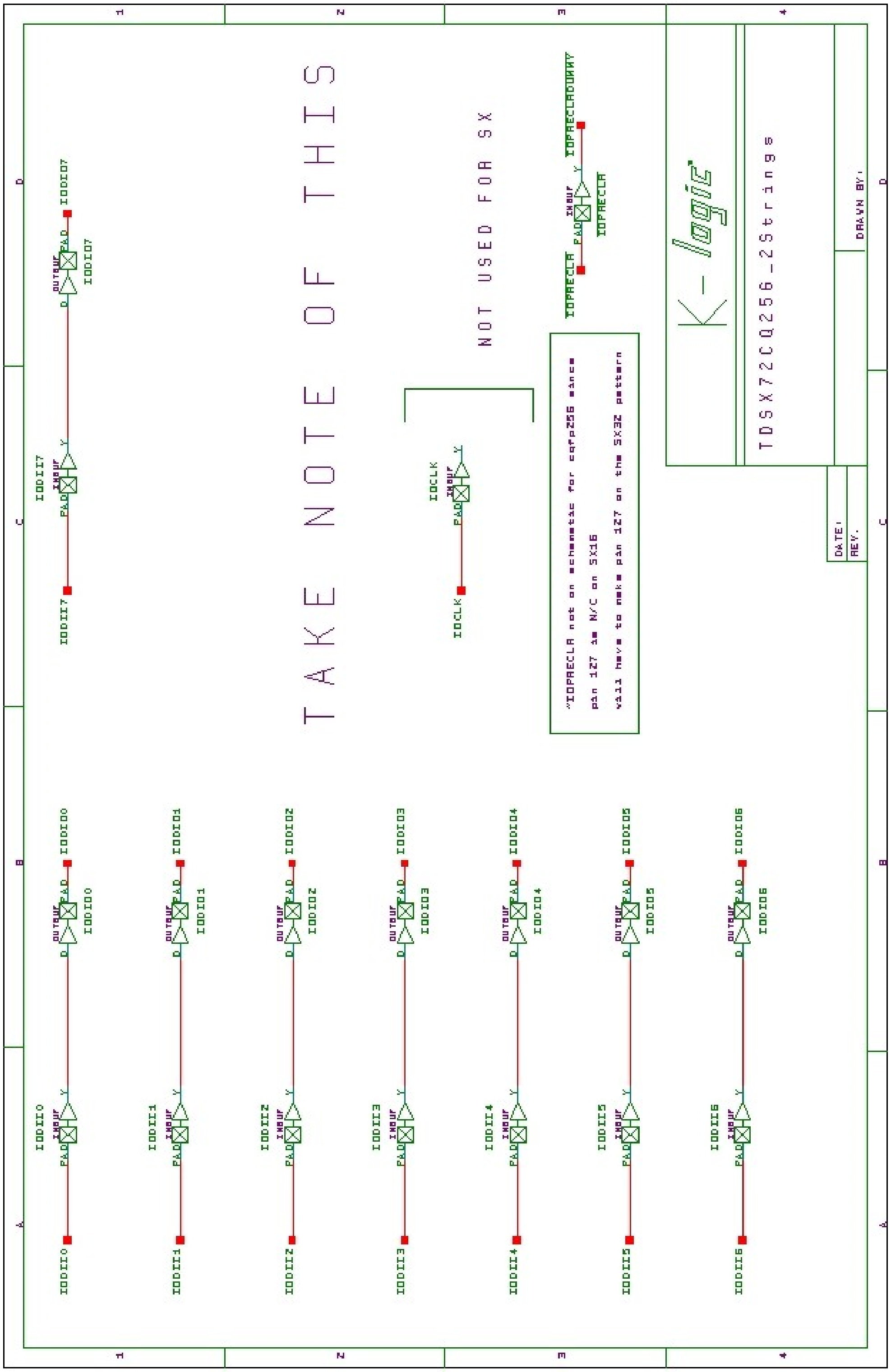

ORC
ANDC
ANDP
ORP
Q
RST
D
CLK
DATE:
REV.
DRAWN BY:

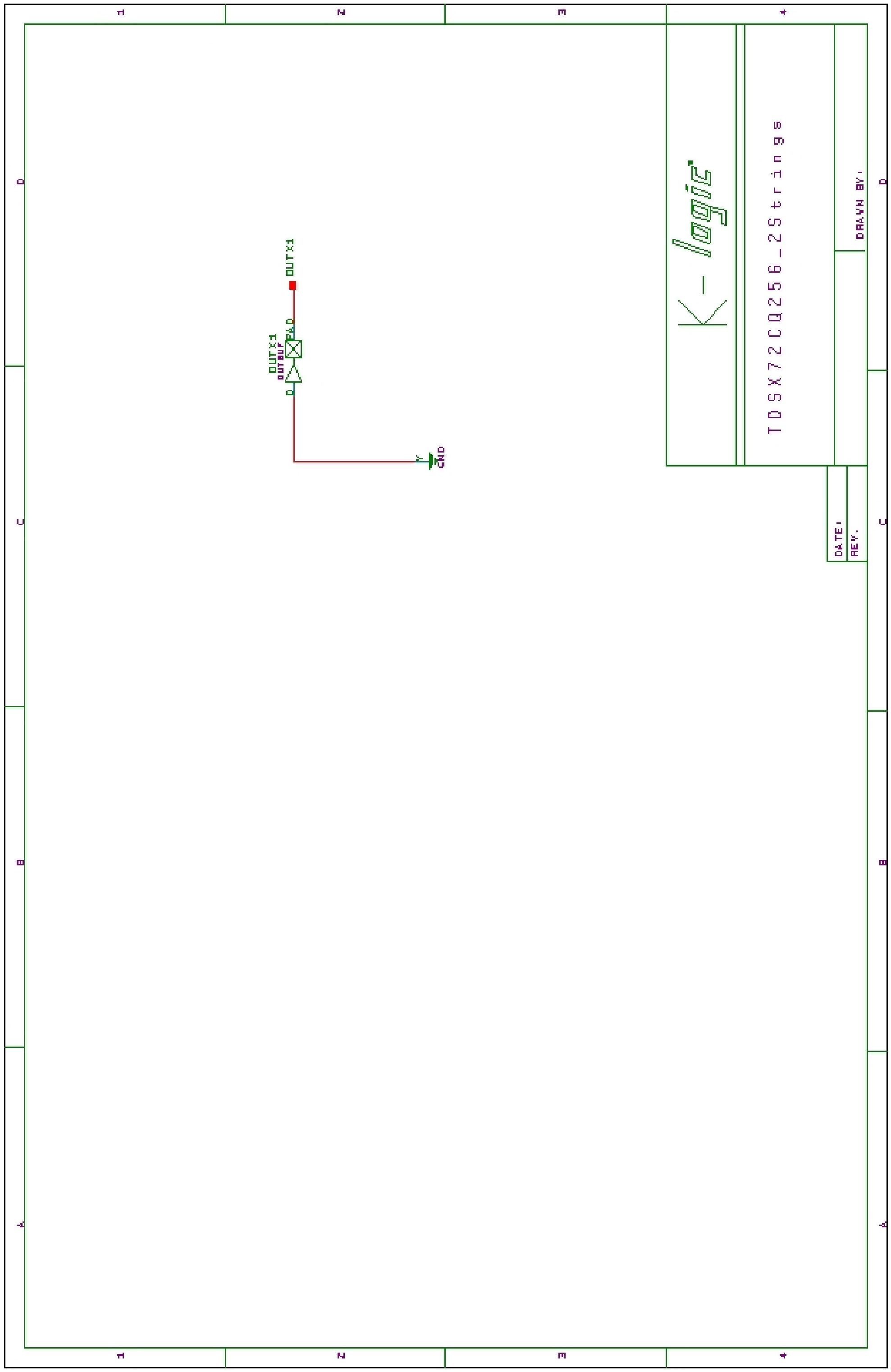

ORC
ANDC
ANDP
ORP
RST
CLK
DATE:
REV.
DRAWN BY:
K-logic


TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
DA2H
DA0H
DA1H
CLKH
OUTBUF
PAD
INBUF
DAH
CLOCKH
HCLKBUF
RESETH


Y00H
Y01H
Y02H
Y03H
Y04H
Y05H
Y06H
Y07H
RESETCNTAH
ENCNTAH
CNTALDH
K-logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.


TAKE NOTE OF THIS
NOT USED FOR SX
*IOPRECLR not on schematic for cqfp256 since pin 127 is N/C on SX16 will have to make pin 127 on the SX32 pattern
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.


TAKE NOTE OF THIS
NOT USED FOR SX
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
IOCLK
IOPRECLR
IOPRECLRDUMMY
IODII0
IODII1
IODII2
IODII3
IODII4
IODII5
IODII6
IODII7
IODIO0
IODIO1
IODIO2
IODIO3
IODIO4
IODIO5
IODIO6
IODIO7


TDSX72CQ256_2Strings
K - logic
DRAWN BY:
DATE:
REV.
OUTX1
OUTBUF
PAD
D
Y
GND

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