PolarFire Neutron Testing Report

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I. TEST OBJECTIVE

The second phase of Neutron testing was performed on Microsemi's new PolarFire family of devices MPF300T. The main objective of this test was to test the product for Single Event Latch up (SEL) behavior as well as to get soft error data on the Flip Flop, LSRAM, µSRAM, Math Block, PLL and DLL on final Silicon, RevF material.

II. DEVICE UNDER TEST

Five parts were irradiated during the test. The samples were prepared by removing packaging material to expose the dice. Resistive heaters were placed on the parts to heat the devices. Maximum achievable temperature was approximately 90°C.

Table 1. Testing Configuration

Part Serial Number	Revision/Lot ID	Patch	Board	Focus
113	F/K5949	Avionics	Daughterboard + Motherboard	Soft Error + SEL
114	F/K5949	Non Avionics	Daughterboard + Motherboard	Soft Error + SEL
115	F/K5949	Avionics	Daughterboard	SEL
116	F/K5949	Avionics	Daughterboard	SEL
118	F/K5949	Avionics	Daughterboard	SEL

1. Beam

Los Alamos WNR target ICE house was used for this experiment. The fluence was calculated based on neutron energies > 10MeV. The flight path length, as shown in Figure 1, is approximately 20 meters from the source to the fission chamber.

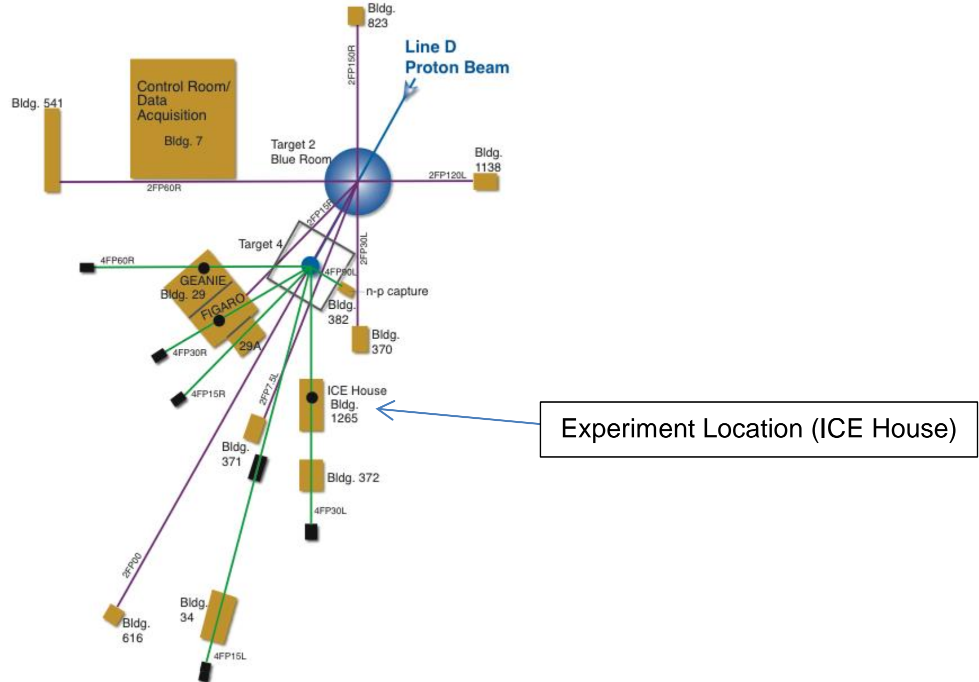

Figure 1: Flight Paths at LANSCE

2. Voltage Bias and Temperature

The five boards were placed one behind the other. Three of the boards are biased at maximum operating condition, the worst case for SEL testing. The biases are recorded in below. For soft errors we ran the devices at nominal voltages.

Table 2 – Voltage configurations (operating conditions)

Channel	Nominal Bias (Soft Errors)	Max recommended operating conditions (SEL)
1	1.05	1.08
2	1.8	1.89
3	2.5	2.575
4	3.3	3.465

The following table outlines which power domains are connected to the respective channels.

Table 3 – Power Domain configuration during testing setup

Channel	DUT Power Domain
1	VDD, VDDA
2	VDD18, VDDI0, VDDI1, VDDI6, VDDI7
3	VDD25, VDDA25, VDDSREF
4	VDDI3, VDDI2, VDDI4, VDDI5, VDDAUX2, VDDAUX4, VDDAUX5

The 2 boards running at temperature ranged between 87°C to 94°C. Refer to the run log below.

3. Testing Procedure

1) Program DUT and Master chips with respective designs and verify functionality

2) Place resistive heaters and sensors on the DUTs. Ramp the temperature up to 87-94°C.
3) Check the functionality of the test designs.
4) Open shutter to start irradiation and monitor outputs.
5) Record SEU/SEL data.

Table 4 - Run log (Entire Test Campaign)

Run	DUT	Irrad Bias	Time Start	Time End	Adjusted Fluence (n/cm^2)	Temperature (°C)
1	113	1.05/1.8/2.5/3.3	9:00AM	9:15AM	4.78+09	Room
1	114	1.05/1.8/2.5/3.3	9:00AM	9:15AM	4.66+09	Room
1	115	1.08/1.89/2.575/3.465	9:00AM	9:15AM	4.58+09	50-94
1	116	1.08/1.89/2.575/3.465	9:00AM	9:15AM	4.50+09	50-94
1	118	1.08/1.89/2.575/3.465	9:00AM	9:15AM	4.43+09	50-94
2	113	1.05/1.8/2.5/3.3	9:30AM	7:09PM	3.83E+10	Room
2	114	1.05/1.8/2.5/3.3	9:30AM	7:09PM	3.74E+10	Room
2	115	1.08/1.89/2.575/3.465	9:30AM	7:09PM	3.67E+10	88
2	116	1.08/1.89/2.575/3.465	9:30AM	7:09PM	3.61E+10	92
2	118	1.08/1.89/2.575/3.465	9:30AM	7:09PM	3.55E+10	Room
3	113	1.05/1.8/2.5/3.3	7:15PM	7:50AM	9.00E+10	Room
3	114	1.05/1.8/2.5/3.3	7:15PM	7:50AM	8.78E+10	Room
3	115	1.08/1.89/2.575/3.465	7:15PM	7:50AM	8.63E+10	88
3	116	1.08/1.89/2.575/3.465	7:15PM	7:50AM	8.49E+10	92
3	118	1.08/1.89/2.575/3.465	7:15PM	7:50AM	8.34E+10	Room
4	113	1.05/1.8/2.5/3.3	7:53AM	8:37AM	5.10E+09	Room
4	114	1.05/1.8/2.5/3.3	7:53AM	8:37AM	4.98E+09	Room
4	115	1.08/1.89/2.575/3.465	7:53AM	8:37AM	4.89E+09	91
4	116	1.08/1.89/2.575/3.465	7:53AM	8:37AM	4.81E+09	94
4	118	1.08/1.89/2.575/3.465	7:53AM	8:37AM	4.73E+09	Room
5	113	1.05/1.8/2.5/3.3	8:42AM	9:50AM	7.01E+09	Room
5	114	1.05/1.8/2.5/3.3	8:42AM	9:50AM	6.84E+09	Room
5	115	1.08/1.89/2.575/3.465	8:42AM	9:50AM	6.72E+09	88
5	116	1.08/1.89/2.575/3.465	8:42AM	9:50AM	6.61E+09	92
5	118	1.08/1.89/2.575/3.465	8:42AM	9:50AM	6.50E+09	Room
6	113	1.05/1.8/2.5/3.3	10:00AM	3:46PM	3.99E+10	Room
6	114	1.05/1.8/2.5/3.3	10:00AM	3:46PM	3.89E+10	Room
6	115	1.08/1.89/2.575/3.465	10:00AM	3:46PM	3.83E+10	88
6	116	1.08/1.89/2.575/3.465	10:00AM	3:46PM	3.76E+10	92
6	118	1.08/1.89/2.575/3.465	10:00AM	3:46PM	3.70E+10	Room
7	113	1.05/1.8/2.5/3.3	3:55PM	9:30PM	3.92E+10	Room

7	114	1.05/1.8/2.5/3.3	3:55PM	9:30PM	3.83E+10	Room
7	115	1.08/1.89/2.575/3.465	3:55PM	9:30PM	3.76E+10	87
7	116	1.08/1.89/2.575/3.465	3:55PM	9:30PM	3.70E+10	91
7	118	1.08/1.89/2.575/3.465	3:55PM	9:30PM	3.64E+10	Room
8	113	1.05/1.8/2.5/3.3	9:45PM	10:00AM	7.99E+10	Room
8	114	1.05/1.8/2.5/3.3	9:45PM	10:00AM	7.79E+10	Room
8	115	1.08/1.89/2.575/3.465	9:45PM	10:00AM	7.66E+10	93
8	116	1.08/1.89/2.575/3.465	9:45PM	10:00AM	7.53E+10	92
8	118	1.08/1.89/2.575/3.465	9:45PM	10:00AM	7.40E+10	Room
9	113	1.05/1.8/2.5/3.3	10:38AM	8:32PM	5.94E+10	Room
9	114	1.05/1.8/2.5/3.3	10:38AM	8:32PM	5.80E+10	Room
9	115	1.08/1.89/2.575/3.465	10:38AM	8:32PM	5.70E+10	92
9	116	1.08/1.89/2.575/3.465	10:38AM	8:32PM	5.60E+10	92
9	118	1.08/1.89/2.575/3.465	10:38AM	8:32PM	5.51E+10	Room
10	113	1.05/1.8/2.5/3.3	8:36PM	3:33AM	5.22E+10	Room
10	114	1.05/1.8/2.5/3.3	8:36PM	3:33AM	5.10E+10	Room
10	115	1.08/1.89/2.575/3.465	8:36PM	3:33AM	5.01E+10	92
10	116	1.08/1.89/2.575/3.465	8:36PM	3:33AM	4.92E+10	92
10	118	1.08/1.89/2.575/3.465	8:36PM	3:33AM	4.84E+10	Room

III. DUT DESIGN

Soft error data was collected on Flip Flops, uSRAM, LSRAM, Math blocks, PLL and DLL. The following is a brief description of the designs used to obtain preliminary data on each respective block.

1. Flip Flop Design

4 Shift register chains with 4000 stages per chain are tested and each flip flop chain used a different data input pattern.

- Chain 1 – input 0s with toggling clock at 10MHz
- Chain 2 – input 1s with toggling clock at 10MHz
- Chain 3 – input checkerboard with clock at 10MHz
- Chain 4 – Slowed down checkerboard with clock at 10MHz

2. LSRAM Design

69 Large SRAM blocks were instantiated, 64 words x 18 bits each word. The SRAM data is read continuously, and compared to a model on the master (expected data) to identify if there are any errors.

3. uSRAM Design

69 micro SRAM blocks were instantiated, 64 words x 12 bits each word. The SRAM data is read continuously, and compared to a model on the master (expected data) to identify if there are any errors.

4. Math Block Design

The design has 2 parallel math block chains with fixed coefficients A, B and C is equal to the input of the previous stage. 10 stages of Math blocks were used in each chain performing the operation P = A*B + C.

IV. RESULTS

1. SEL and Configuration cell

There were no observable SEL or configuration upset for the entirety of this test. The upper bound FIT is provided in Table 5.

Table 5 – SEL and Configuration upset Summary

Temp + Bias	Total	High Temp + Max bias	Room Temp + Max Bias	Room Temp + Nominal Bias
Cross section (cm^2/Device)	$<5.00\times10^{-13}$	$<1.26\times10^{-12}$	$<2.59\times10^{-12}$	$<1.21\times10^{-12}$
FIT/Device [NYC]	<0.007	<0.016	<0.034	<0.016
Fluence (n/cm^2)	2.00×10^{12}	7.90×10^{11}	3.85×10^{11}	8.21×10^{11}

2. Fabric Soft Errors

Both System Controller Suspend Enabled (Avionics) and Disabled (non-Avionics) modes were tested and the results are summarized in Table 6 and 7 respectively.

Table 6 – Fabric blocks FIT Rate Summary (Avionics or System Controller Suspend Enabled)

Block	Pattern	Fluence (n/cm^2)	Cross section (σ)	FIT [NYC]
FF	All 0s	4.15×10^{11}	7.21×10^{-15} (cm^2/bit)	98.33/Mb
	All 1s	4.15×10^{11}	1.08×10^{-14} (cm^2/bit)	147.50/Mb
	CKBD 10MHz	4.15×10^{11}	2.40×10^{-14} (cm^2/bit)	327.78/Mb
	CKBD 2.5MHz	4.15×10^{11}	1.26×10^{-14} (cm^2/bit)	172.08/Mb
LSRAM SBU	Data = Address	4.15×10^{11}	1.43×10^{-14} (cm^2/bit)	195.87/Mb
LSRAM MBU	Data = Address	4.15×10^{11}	$<5.44\times10^{-16}$ (cm^2/bit)	<7.42/Mb
µSRAM SBU	Data = Address	4.15×10^{11}	9.61×10^{-15} (cm^2/bit)	131.13/Mb
µSRAM MBU	Data = Address	4.15×10^{11}	3.81×10^{-15} (cm^2/bit)	51.95/Mb
Math Block	N/A	4.15×10^{11}	7.21×10^{-13} (cm^2/Mathblock)	0.0093/Mathblock
PLL	N/A	4.15×10^{11}	2.40×10^{-12} (cm^2/PLL)	0.031/PLL
DLL	N/A	4.15×10^{11}	2.40×10^{-12} (cm^2/DLL)	0.031/DLL

Table 7 – Fabric blocks FIT Rate Summary (Non-Avionics or System Controller Suspend Disabled)

Block	Pattern	Fluence (n/cm^2)	Cross section (σ)	FIT [NYC]
FF	All 0s	4.05×10^{11}	7.39×10^{-15} (cm^2/bit)	100.77/Mb
	All 1s	4.05×10^{11}	7.39×10^{-15} (cm^2/bit)	100.77/Mb
	CKBD 10MHz	4.05×10^{11}	2.09×10^{-14} (cm^2/bit)	285.53/Mb
	CKBD 2.5MHz	4.05×10^{11}	1.47×10^{-14} (cm^2/bit)	201.55/Mb
LSRAM SBU	Data = Address	4.05×10^{11}	1.42×10^{-14} (cm^2/bit)	194.82/Mb
LSRAM MBU	Data = Address	4.05×10^{11}	$<5.58\times10^{-16}$ (cm^2/bit)	<7.60/Mb
µSRAM SBU	Data = Address	4.05×10^{11}	8.55×10^{-15} (cm^2/bit)	116.63/Mb
µSRAM MBU	Data = Address	4.05×10^{11}	2.79×10^{-15} (cm^2/bit)	38.03/Mb
Math Block	N/A	4.05×10^{11}	1.23×10^{-13} (cm^2/Mathblock)	0.0016/Mathblock
PLL	N/A	4.05×10^{11}	2.46×10^{-12} (cm^2/PLL)	0.032/PLL
DLL	N/A	4.05×10^{11}	2.46×10^{-12} (cm^2/DLL)	0.032/DLL

All 0s and all 1s FF data patterns means shifting All 0s or All 1s and therefore are insensitive to clock glitches. Checkerboard means shifting alternating 0s and 1s in a shift register and thus sensitive to extra clock pulses. The PolarFire FF is a pulsed Latch FF with a clock generation circuit that is sensitive. The contribution of clock glitches in the Checkerboard (10MHz) and Checkerboard (2.5MHz) slow data patterns explains the different error rates calculated for the respective patterns.

3. SEFI Summary

One SEFI event was recorded for the duration of the test, a SEFI is defined as a Chip Level Reset where the chip experiences an unwanted reset with a momentarily loss of functionality during the Reset event. The SEFI self-recovers and no additional Reset of power cycle is required to regain functionality of the design. Table 8 shows the SEFI FIT rate.

Table 8 – SEFI cross section and FIT Rate

Fluence (n/cm^2)	Cross section (cm^2/Chip)	FIT/Chip
2.00×10^{12}	5.00×10^{-13}	0.007

FIT rate adjusted for NYC 40kft and North Pole 50kft are shown in Table 9 and 10. Table 11 shows the formulas for FIT rate calculations.

Table 9 – FIT rate adjusted for NYC 40kft and North Pole 50kft- Avionics or System Controller Suspend Enabled

Block	FIT/Mb[NYC–Sea level]	FIT/Mb[NYC – 40kft]	FIT/Mb[North Pole – 50kft]
FF All 0s	98.33	50690.14	97935.59

FF All 1s	147.50	76035.22	146903.38
FF CKBD10MHz	327.78	168967.15	326451.97
FF CKBD 2.5MHz	172.08	88707.75	171387.28
LSRAM	195.87	100970.45	195079.36
uSRAM	131.13	69306.29	130600.50
Mathblock	0.0093	4.83	9.34
PLL	0.031	16.11	31.13
DLL	0.031	16.11	31.13

Table 10 – FIT rate adjusted for NYC 40k and North Pole 50k- Non-Avionics or System Controller Suspend Disabled

Block	FIT [NYC–Sea level]	FIT [NYC – 40kft]	FIT [North Pole – 50kft]
FF All 0s	100.77/Mb	51948.28/Mb	100366.35
FF All 1s	100.77/Mb	51948.28	100366.35
FF CKBD10MHz	285.53/Mb	147186.79	284371.34
FF CKBD 2.5MHz	201.55/Mb	103896.56	200732.71
LSRAM	194.82/Mb	100426.71	194028.82
uSRAM	116.63/Mb	60125.32	116164.76
Mathblock	0.0016/Mathblock	0.83	1.60
PLL	0.032/PLL	16.51	31.91
DLL	0.032/DLL	16.51	31.91

Table 11 – Formulas used for FIT rate calculations

Formulas	σ(PerBit) = Total Bit Upsets/ Fluence/Total Num Bits σ(Mb) = σ(PerBit)* 2^{20} bits FIT/Mb[NYC] = σ(Mb)*f(NYC)* 10^9 (errors/ 10^9 hour); where f(NYC) = 13n/ cm^2 /hour FIT/Mb[NYC-40kft] = FIT/Mb[NYC] *515.48 FIT/Mb[North Pole- 50kft] = FIT/Mb[NYC]*995.93

V. CONCLUSION

1. There were no instances of SEL or Configuration upset observed for a total fluence of 2.00×10^{12} n/ cm^2 across varying biases (refer to Table 5).
2. One SEFI event with a FIT rate of 0.007/Chip was observed, where the chip experiences a reset and recovers on its own without the need of issuing a power cycle.
3. Cross sections and equivalent FIT rates for Flip Flops, Mathblock, LSRAM and uSRAM are reported in Table 6 and 7.
4. Cross sections and equivalent FIT rates for PLL and DLL blocks are also reported in Table 6 and 7.